

# SEE and TID of Emerging Non-Volatile Memories

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**Abstract** – We report on the SEE and TID tests of higher density flash memories. Stand-by currents and full functional tests were used to characterize the response of radiation effects. Both normal and irregular SEFI were observed indicating upsets from complex control circuitry. TID results are compared with tests from previous generations.

## INTRODUCTION

As non-volatile memories become the standard of today digital audio, video and camera equipment, manufacturers are struggling to supply low-cost high-density flash memories to fulfill the increasing demand [1]. Besides consumer electronics applications, flash memories have been used in solid-state recorders in space mission systems. Current solid-state recorders are designed around reliable, robust and radiation-hardened flash memories. Since most available parts are COTS (commercial-off-the-shelf), redundancy must be built into the system to ensure its data integrity during operating lifetime. Redundancy can be built around multi-chip-module (MCM), which contains duplicates of one die installed in a single package. MCM components that are packed with two or more flash memory die of a similar type can backup data among themselves and then can be directed into different modes. Newer flash memories add multi-block program, multi-block erase, and multi-level storage [2].

There are two types of flash architecture: NOR and NAND. While both architectures have the same basic storage element (consisting of a control gate stacked over an insulating oxide known as a floating gate, a source, and a drain), it is the interconnection of these memory cells that distinguishes the structure. The NOR cell architecture is shown in Figure 1 and in the NOR flash memory array, the bit line logic goes to "0" if any of the memory cell transistors is "ON".

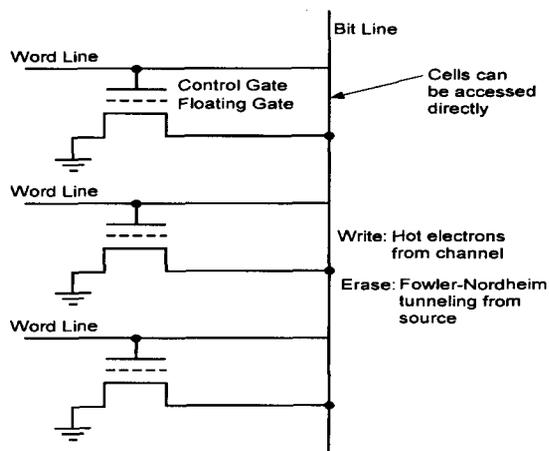


Figure 1: the NOR flash memory architecture

The research described in this paper was carried out at the Jet Propulsion Laboratory, California Institute of Technology, under contract with the National Aeronautics and Space Administration (NASA), under the NASA Electronics Parts and Packaging Program, Code AE.

The NAND cell structure is shown in Figure 2 and in the NAND flash memory array, the bit line logic goes to "0" if all of the memory cell transistors are "ON". Both architectures require charge pump circuits in order to provide the high internal voltages that are needed for erase and write operations.

The memory cells of NAND architecture require 20 volts for writing and erasing, while cells of NOR structure only need 12 volts for erase and program functions. NOR flash memories use Fowler-Nordheim (F-N) tunneling to pull electrons off the floating gate during erasure and inject hot electrons to the floating gate during programming. The NAND type structure inherited more uniform charge transfer between its floating gate and its body since only F-N tunneling is activated for both erasing and writing. The NOR memory structure has relatively fast random read speed, but it has slow erase and write speeds compared to its NAND counterpart.

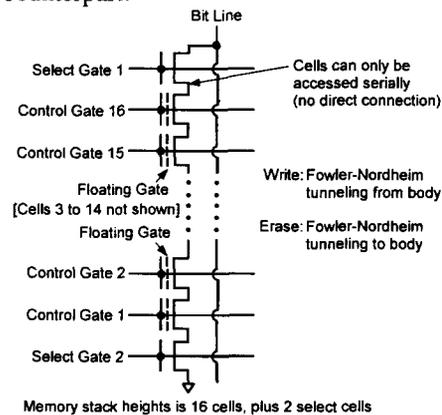


Figure 2: the NAND flash memory architecture

## DEVICE DESCRIPTIONS

The SanDisk SDTNF-512 is a 3.3-volt 512-Mbits NAND flash memory device, organized as 528 bytes X 32 pages X 4096 blocks. Operating modes include of multi-block program, multi-block erase, auto page program, auto block erase, read, status read, and reset.

The AeroFlex ACT-F2M32A has 4 AMD29F016B die in one MCM package. It is a 5.0volts 64Mbits NOR flash memory device, organized as 2M x 8-bit x 4 die. Modes of operation consist of any combination of sectors erasure, read or program data to a sector not being erased, auto die erase, and individual die reset.

	No. of Blocks	Block Size (bytes)	Block Erase Time	Max. E/W Cycles	Initial Bad Blocks
AeroFlex 2Mx32b	32	64K	1s	10 <sup>5</sup>	none
SanDisk 64Mx8b	4096	16.5K	10ms	10 <sup>6</sup>	=< 80

**Table 1: Comparison of AeroFlex and SanDisk device**

As shown in Table 1, the SanDisk flash device requires only 8 seconds to erase the whole part, but the AeroFlex MCM needs at least 32 seconds to perform the similar operation. The SanDisk devices operate with lower currents in all modes, up to 30mA compared to 160 mA (read) and 240 mA(erase/write) for the AeroFlex parts.

**SINGLE EVENT TESTING**

Testing was done at Texas A&M cyclotrons and the Brookhaven National Laboratory (BNL). Properties of the ions used to test AeroFlex MCM and SanDisk parts are listed in Table 2 and Table 3, respectively.

Species	Initial LET	Max. LET	Range $\mu\text{m}$	Angles used
Neon	1.74	9.65	799 – 790	0
Argon	5.41	20.1	500 – 491	0, 38
Krypton	19.2	41.4	336 – 315	0
Xenon	37.9	63.4	286 – 254	0

**Table 2: Ions (at TAM) used to test AeroFlex parts**

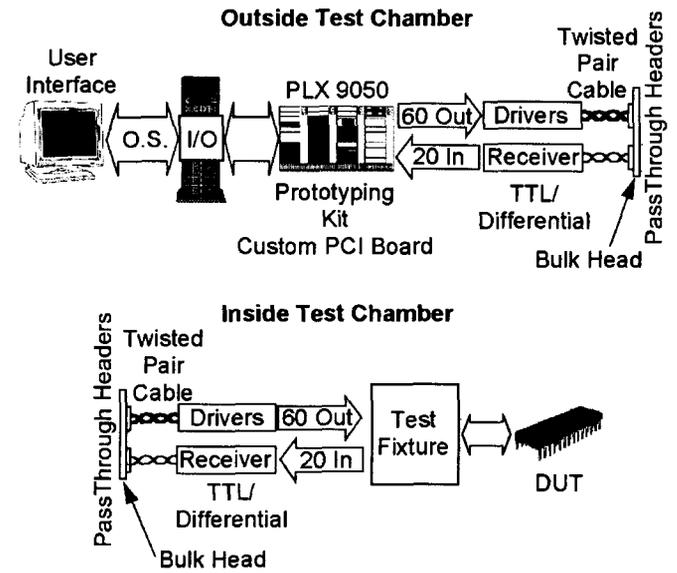
Species	Range $\mu\text{m}$	LET	Angles used
Lithium	113-389	0.371	0, 60, 70, 73
Fluorine	47-122	3.364	0, 45, 50, 60, 67
Silicon	38-75.76	7.901	0, 45, 55, 60
Chlorine	31.7-63.5	11.44	0, 45, 60

**Table 3: Ions used to test SanDisk parts at BNL**

The test equipment was comprised of two PCs, a power supply, and a FPGA-based test board. One PC controlled a HP6629A power supply. This allowed precision voltage control and latch-up detection and protection since the PC had millisecond control over the operation of the power supply. A second, dedicated PC controlled the test circuit board designed specifically to read errors and write commands/test patterns to the DUTs. Parts were programmed with a pseudo-random pattern to mimic real data. The algorithm generates a reproducible sequence of binary states. Two patterns are used to complement each other and to ensure that all bit locations are changed states. The address of any failure and the value at that address were recorded in a file for each run. The number of address and bit failures also was recorded in a separate log file. A depiction of the setup used is shown in Figure 3.

A read error is defined as incorrect data during a read out. During read out, upsets occur in the state machine controller, readout buffer, and registers. Each upset causes large number of errors, up to  $10^5$  with each upset. A write error is defined as the DUT would not be able to write to a specific address due to a time out error (inability to program data in less than one second). Erase errors are similar to write errors because either it takes too long to complete or its monitoring of complete block erase signal halts temporarily. Besides regular above errors, single event functional interrupt (SEFI) errors also occurred during irradiation and post static read. In the case of post read SEFI, the control register was

hit and stuck, consequently locked up the reading sequence. Reset the power to the DUT would re-initialize the register to its normal operational mode. SEFI block erase errors can



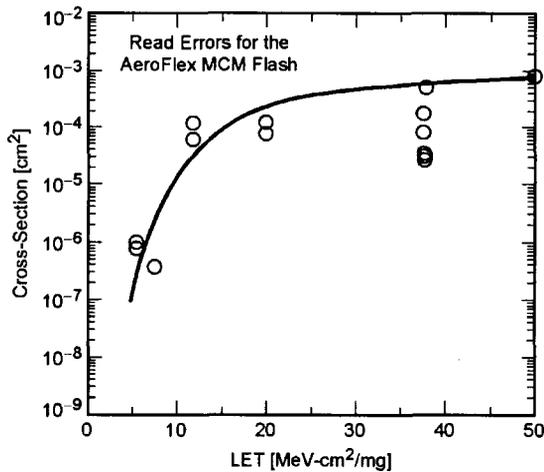
**Figure 3: SEE Test Setup**

produce either an infinite, never-ending operation, or a partial erasure, or a failure to erase the very first few blocks. The observed errors and solutions of recover SEFI locked-ups are described in Table 4.

Error type	Description	Solutions
Block-erase SEFI	Block-erase stuck and its logic never enter ready state.	Reset power only
Partial erase SEFI	Block-erase stopped at the first address. Few blocks were erased.	Repeat Erase/Write/Read
Slow Block-erase	Many passes were required to erase one or more blocks	Wait as long as time limit is within specs.
Write SEFI	Write operation complete status stuck.	Reset power only
Read SEFI	Sensing circuitry stuck due to charge built-up. Next read operation didn't clear errors.	Repeat Erase/Write/Read
Post-read SEFI	Read operation never ended.	Reset power only

**Table 4: Observed errors**

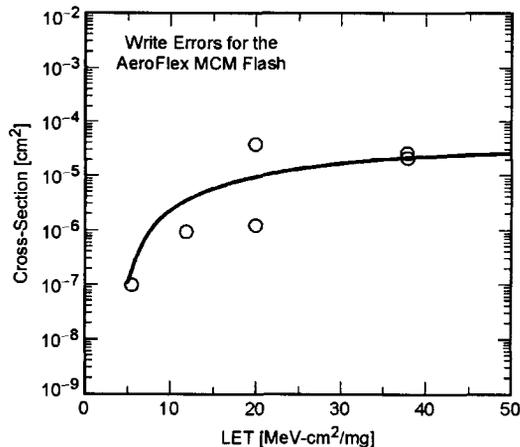
Three AeroFlex MCM parts were tested with negligible variation among them. Figures 4, 5, and 6 are statistically fit using a model by Edmonds [3]. Three operational modes were tested during irradiation: read, write and erase. Static read (post-irradiation) test is also conducted. Figure 4 shows the test results of the dynamic read errors. SEFI happens occasionally with the sudden increase of device supply current. Restarting the read function or cycling power reset SEFI errors. No hard errors or bit erasures were seen in  $10^{11}$  particles per centimeter.



**Figure 4: Cross-section of the dynamic read upsets (AeroFlex MCM)**

Figure 5 illustrates test results of write errors. This occurs due to state machine being upset resulting in the changing of the address it was reading for validation from the address that was being written. Block-erase errors are similar to write errors since the erase operation is aborted before completion. Figure 6 shows the results of the test of the block-erase mode of all three DUTs.

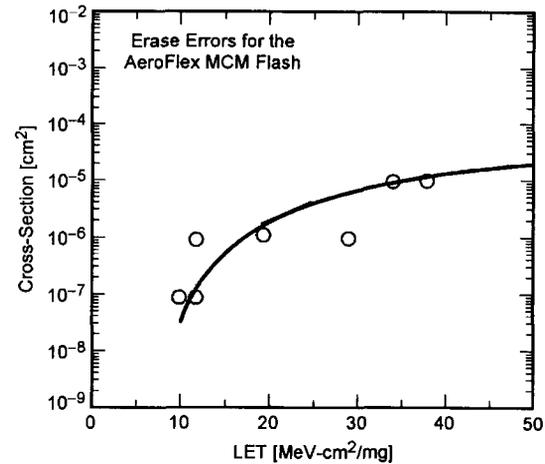
The AeroFlex device showed no Single Event Latchups at any LET. Different combinations of extreme angles and lower energy ions, which should have experienced end of range phenomenon in the sensitive volume of the latchup, did not trigger any latch up. LETs of 120 MeV-cm<sup>2</sup>/mg were used.



**Figure 5: Cross-section of write-upsets (AeroFlex MCM)**

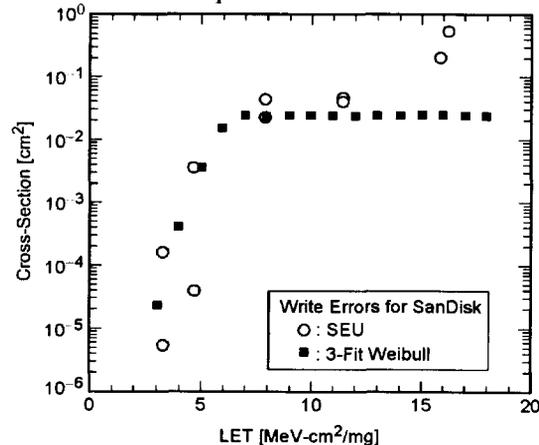
Two SanDisk devices were tested. The read and write modes were used during irradiation. The total time to erase a SanDisk device is less than 9 seconds. The short period of beam-run undoubtedly would not collect any meaningful data for interpretation. SEFI occurred at random and produced a surge in power supply current. After locked up, the SEFI current would stay at an unusual high value and would not re-initialize to idle state unless power was reset. Logic state

switching in the control circuit and registers may cause internal bus contention and probably created the sudden increase.



**Figure 6: Cross-section of erase upsets (AeroFlex MCM)**

One permanent bad block was observed after the lockup produced by a SEFI write upset. Figure 7 shows the cross-section of write upsets in SanDisk parts. Most SanDisk SEFI errors are write errors and similar to the AeroFlex SEFI lockups, they can be recovered with either power cycling or erase/write/read sequences.



**Figure 7: Cross-section of write-upsets (SanDisk)**

Test results for the read-upsets of the SanDisk devices were very similar to the test results observed during the read mode of the AeroFlex MCM components. However, SEFI post-read lockup never occurred for SanDisk parts. Figure 8 displays the SEE read upsets of SanDisk components. Based on Figure 4 and Figure 8, the cross-section of read-upsets of the SanDisk was qualitative similar to those of AeroFlex MCM parts.

#### TOTAL DOSE TESTING

Total dose tests were done using the JPL cobalt-60 facility at the dose rate of 25 rad(Si) per second with a series of 2 krad(Si) steps. DUTs were static biased during irradiation. Electrical parametric measurements were made after each irradiation step with an Advantest test system, while

functional tests were evaluated with the similar SEE setup without the vacuum chamber. Functional tests consist of the following sequences:

1. Erase, write pattern, read to validate stored data
2. Irradiate
3. Read pattern to ensure data retention
4. Erase, write complement data, read to validate
5. Go back to step 2.

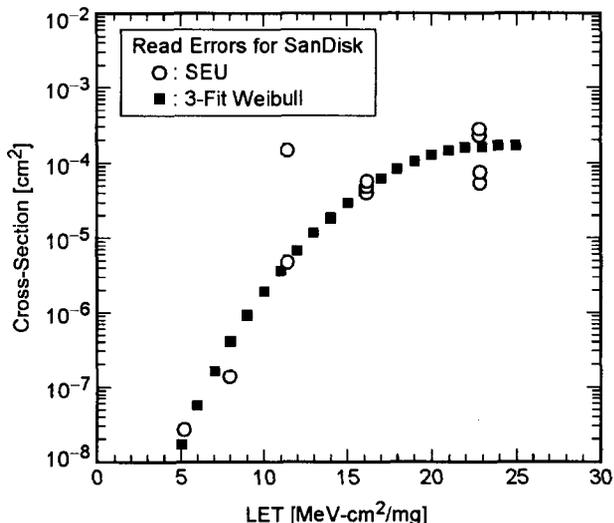


Figure 8: Cross-section of read upsets (SanDisk)

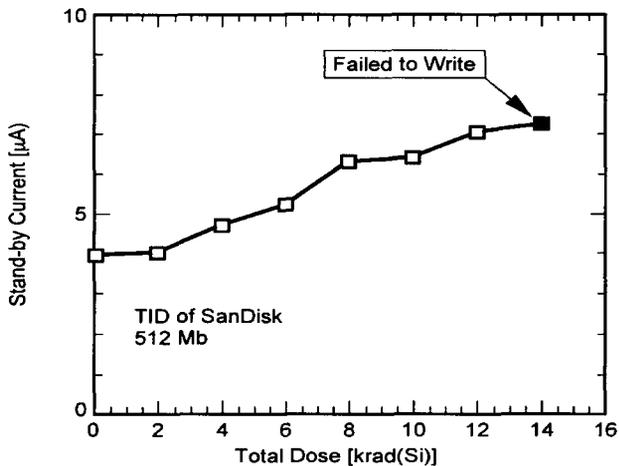


Figure 9: Total dose test results for the SanDisk 512Mb flash devices evaluated in full functional mode

The measured stand-by currents for SanDisk parts show no significant increase, a change of 3.26µA. The stand-by current of SanDisk devices went up to 7.22 µA at 14 krad(Si) at which functional failures occurred. Devices could be erased after 14 krad(Si). But the complement pattern could not be written to the DUTs and there were 5 million-bit read errors after 14 krad(Si). After 24 hours anneal at 3.3 volts and 25 degree C, one SanDisk part could be re-programmed. Previous generations of flash memory devices failed to erase at a lower level, around 8 krad(Si) with full functional tests including the erase/write/read sequence and could not recover

after 24 hours annealing [4]. Figure 9 displays the TID response of SanDisk parts.

The AeroFlex, two AMD29F016B parts, was evaluated in the similar setup as described in the previous paragraph. The AMD parts failed to erase after 8 krad(Si). The stand-by current went from less than 1 µA at the start of the test to 744 µA at 8 krad(Si). This implied that the oxide thickness of AeroFlex die is higher than those of the SanDisk devices. Figure 10 shows the total dose test results for the AeroFlex parts.

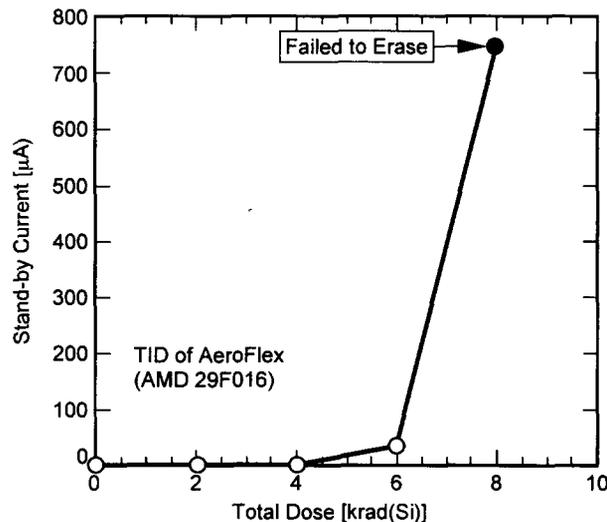


Figure 10: Total dose test results for AeroFlex MCM

## CONCLUSIONS

Both the NAND SanDisk 512Mb and the NOR AeroFlex 64Mb rely on the internal charge pump circuitry to provide high voltages for the erase/write operations. The results showed the component of AeroFlex MCM failed to erase at the total dose level of 8 krad(Si). The SanDisk part, a newer generation, performed better with TID evaluation, which could not be programmed at a higher dose level of 14 krad(Si). Single event upset in both device types appears to be similar with the exception that SanDisk parts did not experience the post-read SEFI while the AeroFlex MCM occasionally generated. A higher density with multi-level NAND flash technology device is currently final tested by Toshiba and hopefully will be ready for samples in the near future may pose a new challenge for space-based applications.

## References

- [1] R.M. Sherwin, "Memory on the move," *IEEE Spectrum*, pp. 55-60, May 2001.
- [2] B. Eitan, R. Kazerounian and A. Roy, "Multilevel flash cells and their trade-offs," *Digest of Papers from the 1996 IEDM*, p. 169.
- [3] L.D. Edmonds, "SEE cross sections derived from a diffusion analysis," *IEEE Trans. Nucl. Sci.*, vol 43, p. 3207 (1996).
- [4] D.N. Nguyen, C.I. Lee and A.H. Johnston, "Total ionizing dose effects on flash memories," *1998 IEEE Radiation Effects Data Workshop Record*, p. 100.