

1400-1900 GHz Membrane Based Schottky Diode Triplers

Alain Maestrini, Goutam Chattopadhyay,
Erich Schlecht, David Pukala and Imran Mehdi

Jet Propulsion Laboratory, MS 168-314, 4800 Oak Grove Drive, Pasadena, CA 91109

Abstract — The membrane based planar Schottky diode process has been utilized to design a family of triplers to cover the astronomically important 1400 to 1900 GHz range. The design process involves a systematic study of the various parameters such as anode size, diode doping, circuit configuration, and circuit topology to name a few. A successful design necessitates that tradeoff space is established and the most *practical* circuit is selected keeping in mind the rather unpredictable task of final assembly. Simulations show that the designs being fabricated will produce output power in the microwatt range which ought to be enough to pump hot electron bolometer (HEB) mixers.

I. Introduction

Recent progress in hot electron bolometer mixers has demonstrated very attractive sensitivities well into the THz regime. However, so far most if not all, of these mixers in the 1 THz range have been pumped with gas-based laser sources. For any flight applications it would be extremely important to develop solid-state sources that can pump these mixers. Fortunately, planar Schottky diodes have revolutionized the field of multiplied sources and in the last few years tremendous progress has been made towards implementing practical planar Schottky diode varactors in the THz range [1]-[6]. The present paper deals with the design of a family of triplers that cover the 1400 to 1900 GHz frequency range.

One possible approach based on a $x_2x_3x_3$ chain driven by power amplifiers in the 92-106 GHz range will cover the astronomically important lines at 1.6 and 1.9 THz. Similarly, a $x_2x_3x_3$ chain driven with a 80-92 GHz power amplifier will cover the 1.46 THz spectrum. The present paper deals with the design of the last stage triplers mentioned in the above scenarios. This paper will address some of the constraints that are placed on designs for the high frequency triplers and will address the methodology involved in designing circuits that can be implemented for robust LO chains.

II. Design Methodology

A common method employed to design and optimize diode multiplier circuits is to first optimize the diode parameters using non-linear codes (such as harmonic balance). The diode impedance is then properly matched to the input and output circuits utilizing linear circuit synthesis. This approach is relatively fast and has shown to work very well with balanced doublers in the sub-THz range [2,4,6], since the input and output circuits can be optimized independently. However, in our approach we have exclusively used non-linear codes to simultaneously optimize the input, output and the idler frequency for designing of the

triplers. Though, this places further burden on the computational hardware, it allows one to simultaneously optimize the diode physical structure along with the embedding circuitry for maximum advantage.

Diode model: A complete and accurate physical diode model that can predict device response at these frequencies is under development [7]. A practical approach is to use a simple model of the diode that can easily be described in commercial codes including significant efficiency limiting phenomena such as breakdown voltage and current saturation. Such an exercise has been carried out in [8] for doublers assuming very limited input power (0.1 mW). Based on this exercise doublers in the 1.9 THz range at room temperature should be designed according to:

$$R_s \times C_j(0) = 120 \Omega \cdot \text{fF} \quad (1)$$

Where, R_s is the series resistance and $C_j(0)$ is the zero bias junction capacitance. Note that depending of the doping of the epy-layer the value of $R_s \times C_j(0)$ can vary: a lower doping level brings more resistance.

For the 1.4THz to 1.9THz triplers a zero bias junction capacitance of 0.6 to 1.2fF is assumed based on the wafer doping ($5 \times 10^{17} \text{ cm}^{-3}$) and reasonable minimum dimensions consistent with the membrane fabrication process. Furthermore, the model was modified by introducing a linear frequency dependence of the RF series resistance. The series resistances of the high frequency triplers was chosen by extrapolating linearly the series resistances used to model an existing (and characterized) 1.2 THz balanced tripler [5] in accordance with (1).

Losses: At 1.9THz, losses in the circuitry are a major concern. Losses not only introduce a linear attenuation of the signals in a multiplier circuit, losses can also make the matching of the diode very inefficient. Simulations show that a diode with $C_j(0)=1\text{fF}$, pumped with 2.5mW at 633GHz, can transfer power to the third harmonic at 1.9 THz up to thirty times more efficiently when matched by an optimal and ideal circuit, than when matched by a circuit feasible with the state-of-the-art technology (with an ideal matching circuit the diode works in a true varactor mode, with a feasible matching circuit the same diode works mostly in a varistor mode). The losses must be included during the optimization of the circuit and not after. Matching circuits designed with no loss could be in practice “surprisingly” lossy and not fully optimum.

Topology limitation & accuracy: Another major difficulty encountered in the designing of terahertz multipliers is the limitation in the topology of the circuits. This limitation is mainly due to the RF losses that the metallic parts of the circuits can induce. Actually, to keep the losses acceptable, it is necessary to use matching elements made of sections of waveguides in which the currents flow with a low surface density. The rectangular waveguide, the coaxial waveguide or the suspended microstrip are usually good candidates for such a requirement. Unfortunately the topology of the circuits feasible with such

waveguides is pretty limited. In addition, the active devices are totally immersed in these waveguides, a fact that does not facilitate efficient modeling.

The accuracy of the fabricated circuits is also a concern when working at these frequencies. It is important to design the circuits to be as tolerant as possible to fabrication and assembly variations. To allow for machining tolerances in the waveguide blocks it is recommended to integrate on chip the critical matching elements in order to take advantage of the tighter tolerances associated with micro-photolithographic techniques. Circuits fabricated on thin dielectric membrane combine low loss and accuracy providing for a more stable and robust implementation.

Input power: Another practical constraint that must be acknowledged for any high frequency multiplier design is the fact that only limited amount of RF power will be available to drive the multiplier. When the pump power of a multiplier is small, the diode cannot be properly modulated. At the limit, the power conversion from the fundamental to the n^{th} harmonic follows a law that asymptotically tends to:

$$P_n \xrightarrow{P_1 \rightarrow 0} \alpha(f) \times P_1^n \quad (2)$$

or in the logarithmic form :

$$\text{Log}(P_n) \xrightarrow{P_1 \rightarrow 0} \alpha'(f) + n \times \text{Log}(P_1) \quad (3)$$

where P_n is the power produced at n^{th} harmonic, P_1 is the pump power, $\alpha(f)$ is coefficient that depends on the diode and the frequency. Equation (2) shows that for a tripler ($n=3$), dividing the pump power by two can divide the output power delivered by the diode by eight (and the conversion efficiency by four). This relationship is confirmed by simulating various multipliers with varying input power (see Figure 1).

Circuit configuration: When one has to choose between designing a balanced multiplier that requires at least two diodes, or an unbalanced multiplier that requires only one, the relation between the pump power and the efficiency of a diode has to be taken into account. The single diode of an unbalanced multiplier will receive twice the power that each diode of the simplest balanced multiplier will receive. In addition, the higher the order of multiplication, the bigger the difference in the conversion efficiency of the diode. On the other hand, balancing a multiplier considerably simplifies the matching circuit. In addition, there is the possibility to reduce the size of the anode to compensate the decrease of pump power (a smaller diode will be easier to modulate than a bigger one). In practice, this possibility is limited at high frequencies by the fact that a smaller anode presents a higher series resistance, and also by the fact that there is a minimum size for the anode.

Thus, for the 1.4 THz to 1.9 THz tripler designs both a balanced and an unbalanced approach was attempted. A generic block diagram of an unbalanced and balanced tripler are shown in Figure 2. An E-plane probe located in the input rectangular-waveguide couples the signal at the fundamental frequency to a suspended-microstrip waveguide that can propagate only the TEM mode. In order to keep this waveguide monomode, the dimensions of the channel in which the circuit is inserted have to be chosen with care. The diode(s) is (are) connected to an E-filed probe that couples the third harmonic of the funda-

mental to the output waveguide (the second harmonics is kept below cutoff). The matching of the diode is performed, both, by a succession of high and low impedance sections printed on chip and by the input and the output probes, with their respective backshort and waveguide step.

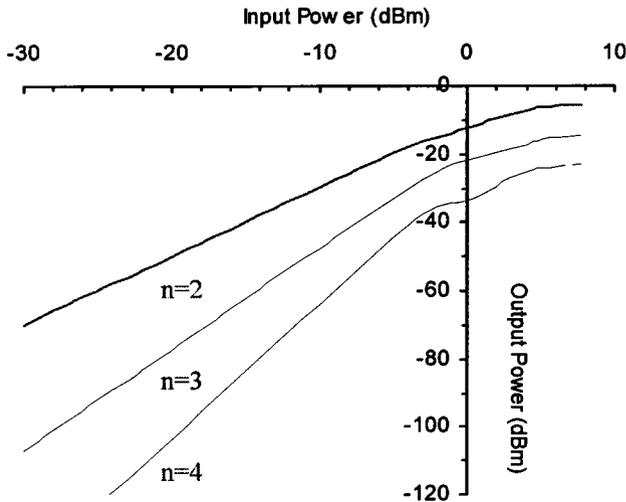


Figure 1: The calculated output power versus input power of an ideal frequency doubler (top), tripler (middle) and quadrupler (bottom) fits perfectly equation 3. The multipliers are optimized for an input frequency of 500GHz and an input power of 3.5mW. The diode is the same for all the multipliers – $C_j(0)=1\text{fF}$, bias fixed to zero volts.

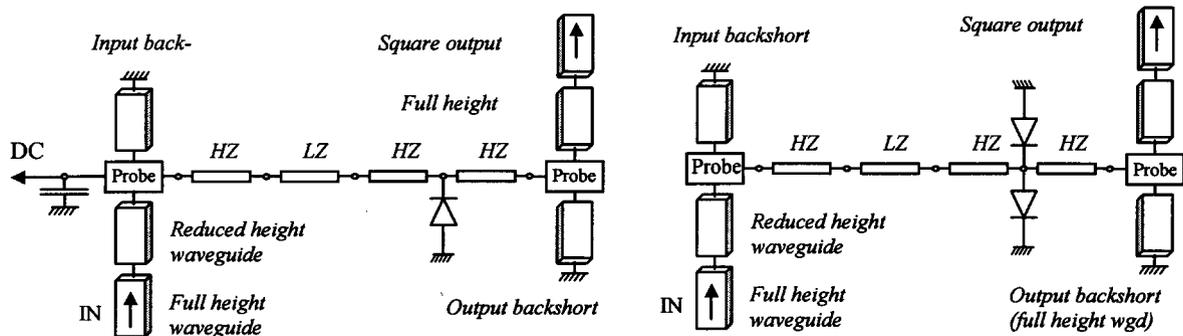


Figure 2: Generic block diagram of the unbalanced (left) and balanced (right) triplers. *HZ* stands for high impedance line, *LZ* stands for low impedance line.

III. A 1400 GHz tripler

The technology involved in fabricating these circuits has been discussed in [9]. The circuits are mounted in a gold-plated waveguide structure split into two precision-machined halves. Figure 3 shows the unbalanced and balanced designs inside the waveguide blocks. The diode of the unbalanced design has a very small mesa with a symmetrical anode that is grounded on both sides of the channel by two beam-leads. Each side of the mesa is connected to a high impedance line. One of them continues to the output probe. This structure is very compact. This design provides compactness but does slightly increase the parasitic capacitance.

The balanced tripler (Figure 3, bottom) has two diodes positioned on each side of the high impedance line. The diodes are connected in series at DC. One has its anode grounded at one side of the channel by a first beam-lead, the other has its cathode grounded to the other side of the channel by a second beam-lead. Due to the symmetry of the field at the fundamental frequency (TEM mode), the diodes appear in an anti-parallel configuration at RF. The second harmonic is trapped in a virtual loop [3] and cannot propagate in other parts of the circuit. This topology offers the advantage of a very small phase shift between the two anodes and the possibility to tune the matching at the idler frequency by adjusting the length of the beam-leads that ground the diodes. By reducing the mesa size from $10 \times 10 \mu\text{m}$ (minimum size used up to now at JPL) to $7 \times 7 \mu\text{m}$, we could implement the two diodes in a channel of $64 \times 25 \mu\text{m}$.

For these circuits the bias scheme is not a trivial problem. The unbalanced tripler can be biased through the input probe (that crosses the entire waveguide height) and the suspended microstrip line. A DC capacitor is implanted on chip to ground the RF signal. This solution can also work for the balanced designs but it is much more difficult to implement. Actually, two independent and opposite polarities have to be brought to the diodes. This can be done by implementing a small capacitor between the two mesas. The suspended microstrip has also to be divided into two insulated lines as shown in Figure 4. It is also possible to design the balanced circuit so that it is pretty much optimized for zero bias. We have included both designs in the current fabrication run.

We can compare the calculated performances of these multipliers with the performances of a diode that would be matched by an ideal circuit : at 1.46THz the balanced circuit is only about two times worse in terms of efficiency than an ideal circuit. Calculations show that 75% of the fundamental is coupled to the diodes. The remaining losses (another 25%) are shared between the second and the third harmonic. Simulated output power from the triplers is shown in Figure 5. For a given input power of 3.5 mW the balanced approach certainly seems to be the preferred approach. Considering that over 8 mW has already been demonstrated at 440 GHz it is possible that more input power will be available. Even with the limited input power a 3dB bandwidth of about 20% is achievable. Moreover, considering that the HEB mixers might only require LO power levels at the one microwatt range the existing design ought to cover even a larger bandwidth.

IV. A 1900 GHz Tripler

The unbalanced and balanced designs for the 1.9 THz tripler are shown in Figure 6. At a first glance they would seem to be 'scaled' copies of the designs for the 1.4 THz tripler. Even though the basic topology of the two designs looks similar, a detailed design was done for both triplers because simple scaling from one design to the other does not work.

Compare to the 1.4THz triplers, the 1.9THz triplers have a narrower channel. The mesas have the same size but their spacing is reduced. Another difference: the anode of the un-

balanced design at 1.9THz is grounded on both sides of the channel by two wide beam-leads that come very close to the mesa.

For the balanced circuit, implementing the two diodes was very difficult due to space limitation, even with a mesa as small as 7x7 micron. The chip was designed using the tightest tolerances available with the current technology.

Biasing of the unbalanced design is not difficult. However, a biasing scheme for the balanced design is not trivial. The solution suggested for the 1.4 THz design will not work due to space restrictions. The current circuit has been designed with zero bias. This sacrifices some of the potential bandwidth but seems to be the only practical approach given the restrictions on technology.

An input power of 2.5mW at 633 GHz is assumed. This amount of power has not been demonstrated yet but certainly looks plausible given the recent results up to 400 GHz. Optimized simulations of both the balanced and unbalanced circuits are shown in Figure 7. The balanced configuration can provide twice as much power as the unbalanced design but only for a limited bandwidth. At the band edges both designs provide similar amounts of output power. The inability to further reduce the length of the beam-leads that ground the diodes of the balanced tripler is believed to be the main reason for this limitation.

We can compare the calculated performances of these multipliers with the performance of a diode that is matched by an ideal circuit. The balanced tripler design has one-eighth the efficiency as an ideal tripler using the same diode. Only 70% of the fundamental is coupled to the diodes. The low performance of this circuit is believed to be mainly due to a non-optimized idler forced by the current technology.

An interesting simulation is to see what happens to the performance of the multipliers as input power is reduced. As the input power drops below 1 mW the unbalanced circuit tends to outperform its balanced counterpart. One could argue that the designs have not been optimized for low power but in reality the anodes cannot be shrunk any more to offset the reduced input power level.

V. Conclusion

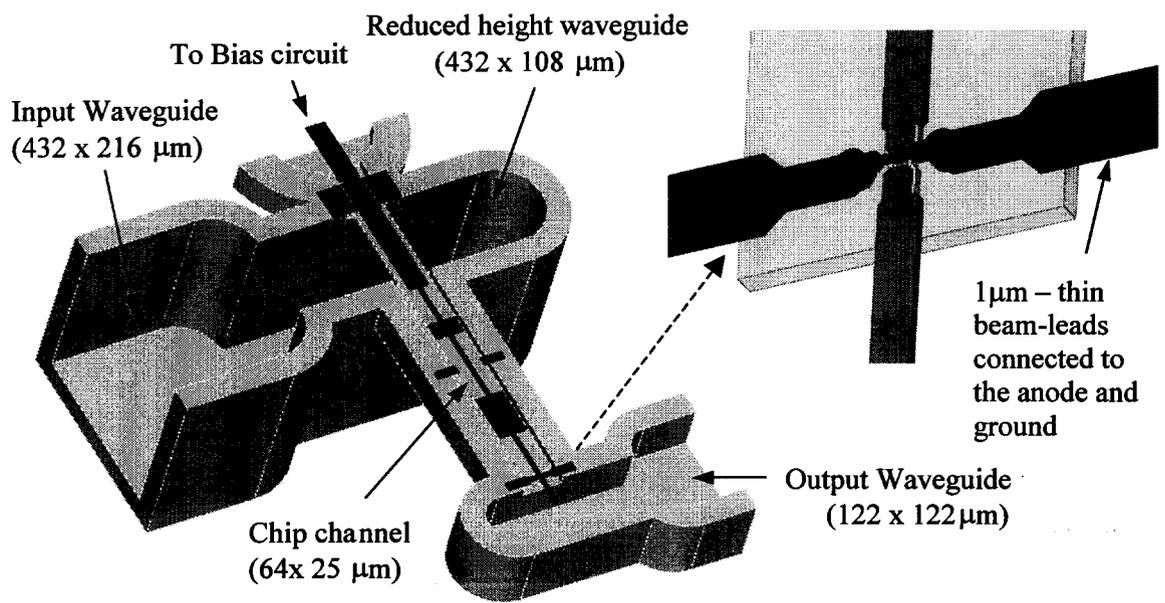
Triplers that work in the 1400 to 1900 GHz range have been designed and described. These circuits are based on the GaAs membrane process and are currently under fabrication. Simulations indicate that if the final stage triplers can be pumped with 2-4 mW of input power it will be possible to get sufficient output power to pump HEB mixers.

ACKNOWLEDGMENTS

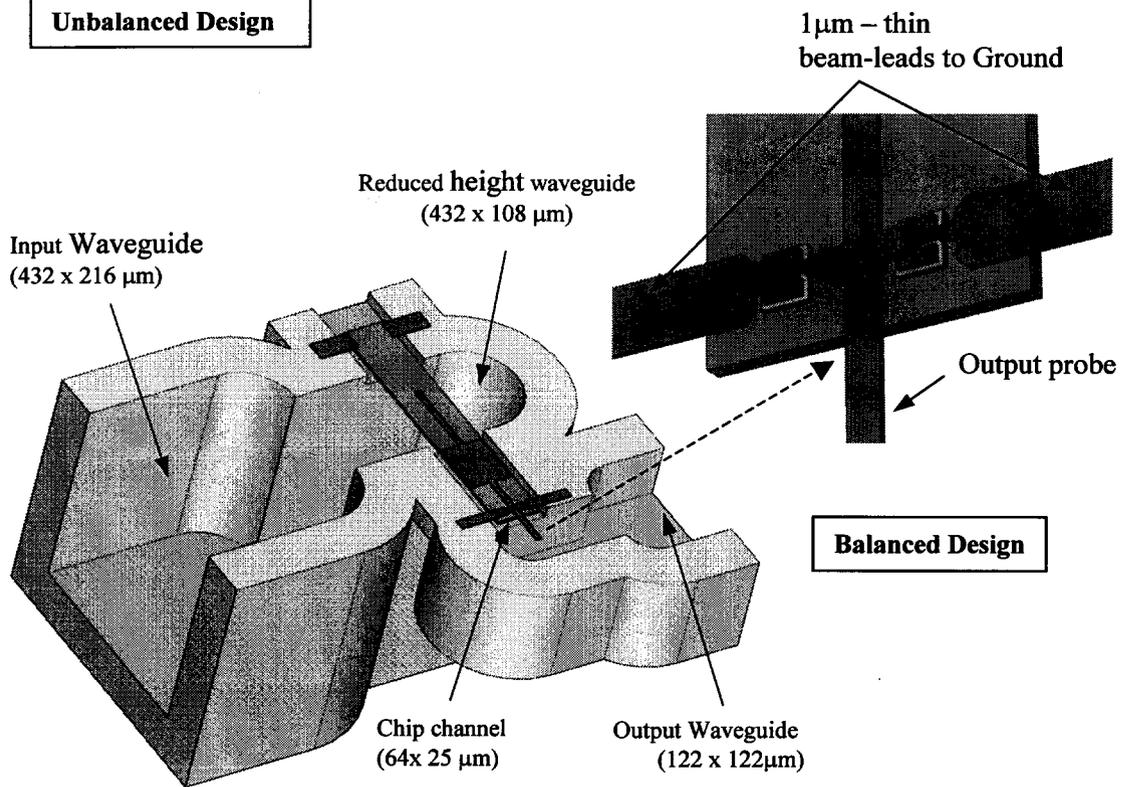
The authors wish to acknowledge many helpful discussions with Neal Erickson, Peter Siegel, Suzi Martin, and John Gill. The research described in this publication was carried out at the Jet Propulsion Laboratory California Institute of Technology, under a contract with the National Aeronautics and Space Administration.

REFERENCES

1. N. Erickson, R. P. Smith, S. C. Martin, B. Nakamura, and I. Mehdi, "High Efficiency MMIC Frequency Triplers for Millimeter and Submillimeter Wavelengths," *IEEE MTT Symposium*, Boston, June 2000.
2. E. Schlecht, G. Chattopadhyay, A. Maestrini, A. Fung, S. Martin, D. Pukala, J. Bruston and I. Mehdi, "200, 400 and 800 GHz Schottky diode substrateless multipliers: Design and results," in 2001 IEEE MTT-S Int. Microwave Symp. Dig., Phoenix, AZ, May 2001, pp. 1649-1652.
3. J. Bruston, A. Maestrini, D. Pukala, S. Martin, B. Nakamura and I. Mehdi, "a 1.2 THz planar tripler using GaAs membrane based chips," *proceeding of the 12th International Space Terahertz Technology Symposium*, San Diego, February 2001.
4. N. R. Erickson, G. Narayanan, R. M. Grosslein, S. Martin, P. Smith, I. Mehdi, M. Coulomb, G. DeMartinez, "Monolithic THz frequency multipliers," Proc. of the 12th Intl. Space Terahertz Technology Symp., San Diego, Feb. 2001, pp. 297-309.
5. A. Maestrini, J. Bruston, D. Pukala, S. Martin, I. Mehdi, "Performance of a 1.2 THz Frequency Tripler using a GaAs Frameless Membrane Monolithic Circuit," *IEEE MTT-S International Microwave Symposium*, Phoenix, Arizona, May 20-25, 2001.
6. G. Chattopadhyay, E. Schlecht, J. Gill, S. Martin, A. Maestrini, D. Pukala, F. Maiwald, and I. Mehdi, "A Broadband 800 GHz Schottky Balanced Doubler," *IEEE Microwave and Wireless Components Letters*, Vol. 12, no. 4, April 2002.
7. E. Schlecht, F. Maiwald, G. Chattopadhyay, S. Martin, and I. Mehdi, "Design considerations for heavily-doped cryogenic Schottky diode varactor multipliers," in Proc. 12th Intl. Space Terahertz Technology Symp., San Diego, CA Feb 2001, pp. 485-494.
8. Neal Erickson, private communications, 2000-2001.
9. Suzanne Martin, Barbara Nakamura, Andy Fung, Peter Smith, Jean Bruston, Alain Maestrini, Frank Maiwald, Peter Siegel, Erich Schlecht and Imran Mehdi, "Fabrication of 200GHz to 2700GHz Multiplier Devices using GaAs and Metal Membranes," *IEEE MTT-S International Microwave Symposium*, Phoenix, Arizona, May 20-25, 2001.



Unbalanced Design



Balanced Design

Figure 3: Unbalanced and balanced design of the 1400 GHz tripler.

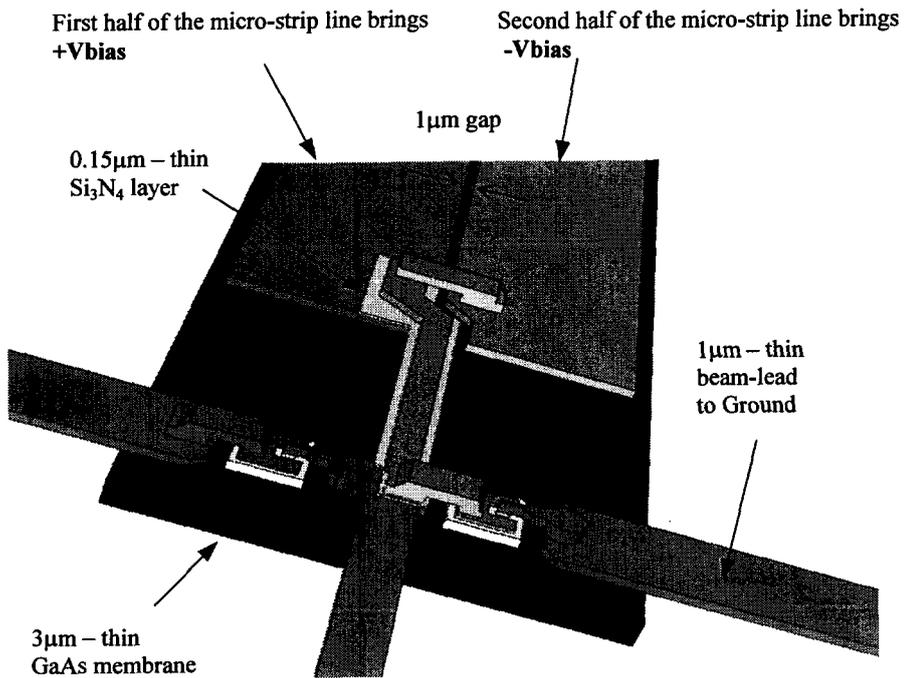


Figure 4: A possible approach for providing appropriate bias to a balanced tripler design.

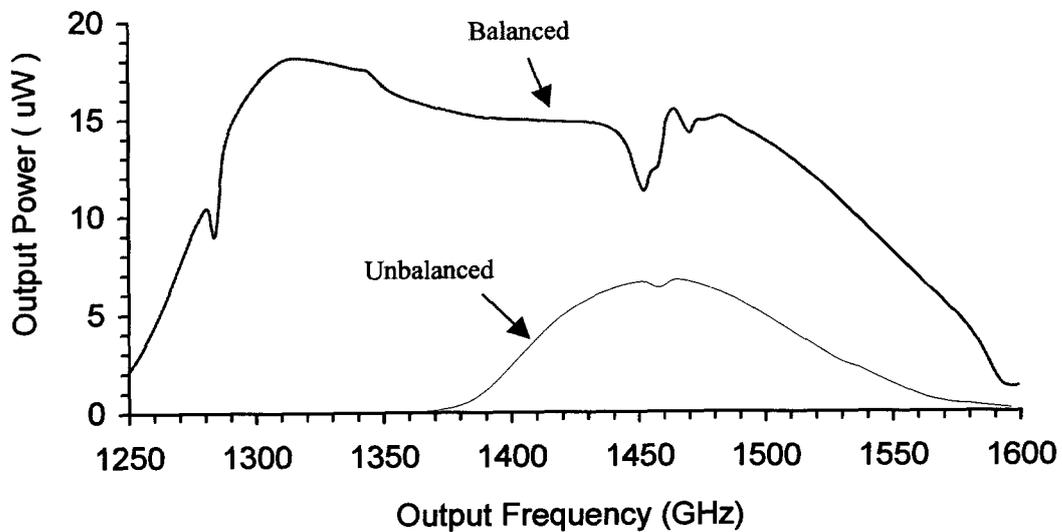


Figure 5: Calculated output power of the 1.4 THz balanced and unbalanced tripler. Input power of 3.5 mW is assumed in each case

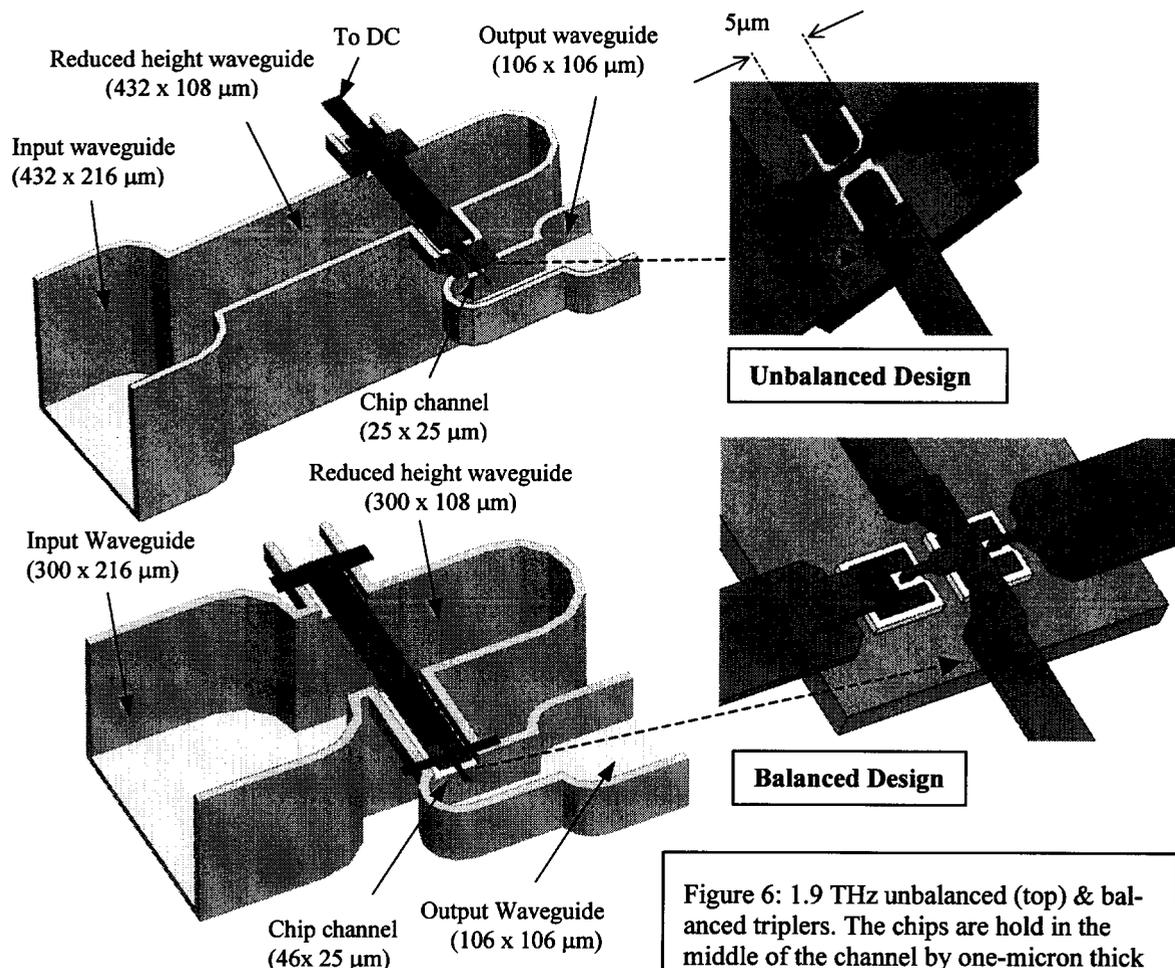


Figure 6: 1.9 THz unbalanced (top) & balanced triplers. The chips are hold in the middle of the channel by one-micron thick beam-leads. The balanced circuit does not allow to bias the diodes.

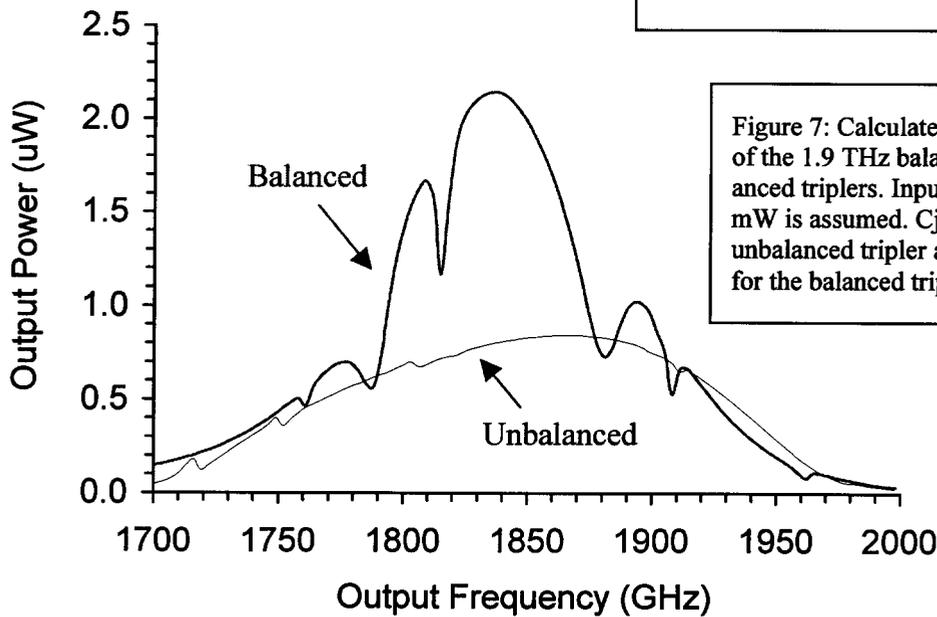


Figure 7: Calculated output power of the 1.9 THz balanced and unbalanced triplers. Input power of 2.5 mW is assumed. $C_j(0)=1\text{fF}$ for the unbalanced tripler and $C_j(0)=0.8\text{fF}$ for the balanced tripler.