

INTEGRATED IMAGING SENSOR SYSTEMS WITH CMOS ACTIVE PIXEL SENSOR TECHNOLOGY

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ABSTRACT

The availability of mature sub-micron CMOS technology has enabled the development of high performance active pixel sensor (APS) imagers and made possible the realization of drawing electronic imager technology into the mainstream of CMOS system-on-a-chip technology. The primary advantages of this CMOS APS imager technology are low-cost, low-power, simple digital interface, random access, simplicity of operation, high speed, miniaturization through system integration and improved functionality by incorporating on-chip signal processing circuits. This paper discusses common approaches to CMOS APS technology, as well as specific results on the five-wire programmable digital camera-on-a-chip developed at JPL. The paper also reports recent research in the design, operation, and performance of APS imagers for several imager applications.

1. INTRODUCTION

Today there are many kinds of electronic imagers with very different characteristics for consumer, commercial, scientific, military, and space applications. For example, camcorders are the most well known electronic imager. They capture images with television resolution at 30 frames per second. Other examples range from digital still cameras, computer peripherals, mobile robots, unmanned vehicles – including self-navigating cars and search-and-rescue vehicles, automatic assembly and product inspection systems to surveillance and military applications involving smart weapons and missile defense systems. Electronic imagers are also of great interest in existing and future space applications involving space communications, space navigation, robotic exploration of planets, and autonomous rovers.

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Despite the wide variety of applications, all electronic imagers have the same basic functions. These are (1) detector array for converting the incoming photons to photoelectrons, (2) a method to readout the collected electrons in the detector array, (3) timing, control and driver electronics to enable the readout, (4) signal processing electronics, (5) analog to digital conversion, and (6) interface electronics. Low-power, low-cost, miniature and integrated imaging systems are desired for most imager applications, especially in consumer electronics.

While CMOS technology has been responsible for the phenomenal growth in consumer electronics, micro-processors, memory, audio systems, and radio-frequency circuits (e.g. cellular phones), until recently, video technology remained outside this mainstream with charge-coupled-devices (CCD) as the incumbent technology for electronic imaging. First reported in 1970^[1], the development on CCD technology makes CCD imagers represent a matured technology in electronic imaging due to their superior sensitivity, dynamic range, uniformity, low noise, and small pixel size. However in order to achieve low charge transfer loss (typically $< 10^{-7}$), CCDs require specialized silicon processing (e.g. special implants, 2 or 3 layers of gate poly) that is not compatible with CMOS technology. Furthermore, CCDs are high capacitance devices, requiring multiple non-standard and high voltage clocks and biases, while providing only serial analog output (no random access and no digital output is provided). High device capacitance, large clock swing, need for DC-DC converters, and inability to integrate control and processing electronics on the imager chip make the CCD-based imaging system bulky and power-hungry (camcorder CCD power dissipation is around 10 Watts). Incompatibility with CMOS technology is a major barrier to realizing low-power, low-cost, miniature and integrated system-on-a-chip using CCDs.

Despite several earlier attempts, CMOS imaging performance lagged behind that of CCDs. The availability of mature near or sub-micron CMOS technology, in conjunction with the advent of new low noise active pixel sensor (APS) concepts altered this situation in the 1990's^[2, 3, 4]. The APS approach enables high quality CMOS imagers with performance rivaling those of CCDs, drawing electronic imager technology into the mainstream of CMOS system-on-a-chip development. The primary advantages of CMOS APS are low-cost, low-power (100 - 1000× lower than CCDs), simple digital interface, random access, simplicity of operation (single CMOS compatible power supply), high speed (> 1000 frames per second), miniaturization (10 - 100× smaller) through system integration, and smartness by incorporating on-chip signal processing circuits.

In this paper, we first give an overview on common approaches of CMOS APS technology in Section 2. The simple interface, programmable digital camera-on-a-chip using CMOS APS technology developed at JPL is described in Section 3. We conclude with a report on recent research developments at JPL,

including design, operation, and performance of APS imagers for different camera system applications in Section 4.

2. CMOS ACTIVE PIXEL SENSOR TECHNOLOGY

As mentioned in the previous section, an electronic imager has several function blocks. Since CCDs employ specialized silicon processing that is not compatible with CMOS technology, a CCD imager requires multiple chips for imager realization, multiple high and non-standard voltages for operation. However, since APS imager using standard CMOS process, the integration of all of the function blocks along with CMOS pixel array enables the realization of a single-chip imager. Figure 1 shows the schematic block diagram of a general CMOS APS architecture. The imager chip contains the pixel array (see Section 2.1) and a sample and hold block (see Section 2.2). It also contains some or all of the following function blocks: analog output signal chain (see Section 2.3), analog to digital converter (ADC) block (see Section 2.4), digital to analog converter (DAC), digital I/O interface, and timing and control.

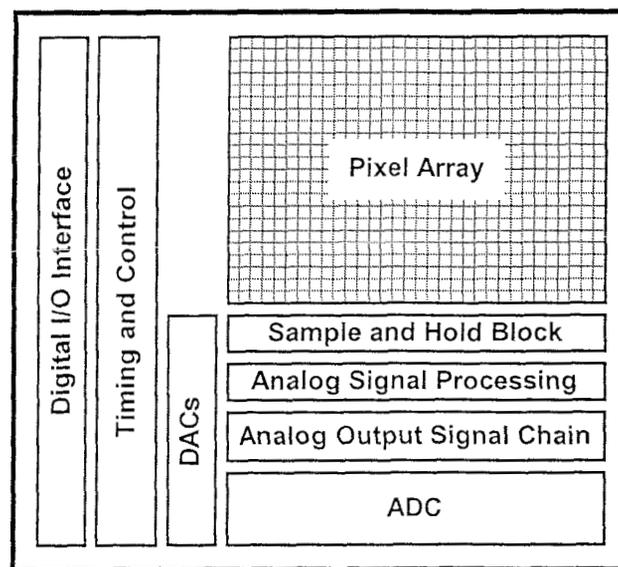


Figure 1. Schematic block diagram of general CMOS APS architecture.

2.1 CMOS Active Pixel Approach

The detector is composed of an M -row \times N -column pixel array. A sensor with an active amplifier within each pixel is referred to as an active pixel sensor or APS. There are two predominant approaches to pixel implementation in CMOS APS, photodiode-type active pixel and photogate-type active pixel.

The photodiode-type APS was described by P. Noble in 1968 [5] and has been under investigation by F. Andoh since the late 1980's [6, 7]. Figure 2(a) shows the schematic and potential diagram of the photodiode-type APS pixel, and Figure 2(b) shows a typical layout of the pixel. JPL as well as many other companies use this pixel structure in the CMOS imager design. The pixel consists of a reverse-biased p-n junction where the photons are converted into photoelectrons and are collected. The reversed p-n junction can be formed by either n+ implant to p-substrate (or p-well) or n-well implant to p-substrate. The photodiode-type APS use three transistors per pixel. A reset transistor (M_{RST}) that is used to periodically reset the photodiode, a source-follower input transistor (M_{SF}) is employed to buffer the photodiode, and a select transistor (M_{SEL}) with its gate commonly connected to an entire row of pixels. Not shown in Figure 1 is the load of the source-follower that is located at the bottom of each column of pixels and shared by the pixels in the column. Double sampling scheme is employed for readout. Photodiode is charged by photoelectrons and its resultant voltage measured by the source follower. After that, pulsing the RST gate resets the photodiode. Then the reset voltage is sensed. The difference between the signal level and the reset level is the output of the sensor. This double sampling fixed pattern noise (FPN) due to threshold voltage variations. Unlike a CCD pixel which produces a charge output, an APS pixel produces a voltage output over the column bus, and hence provides random-access.

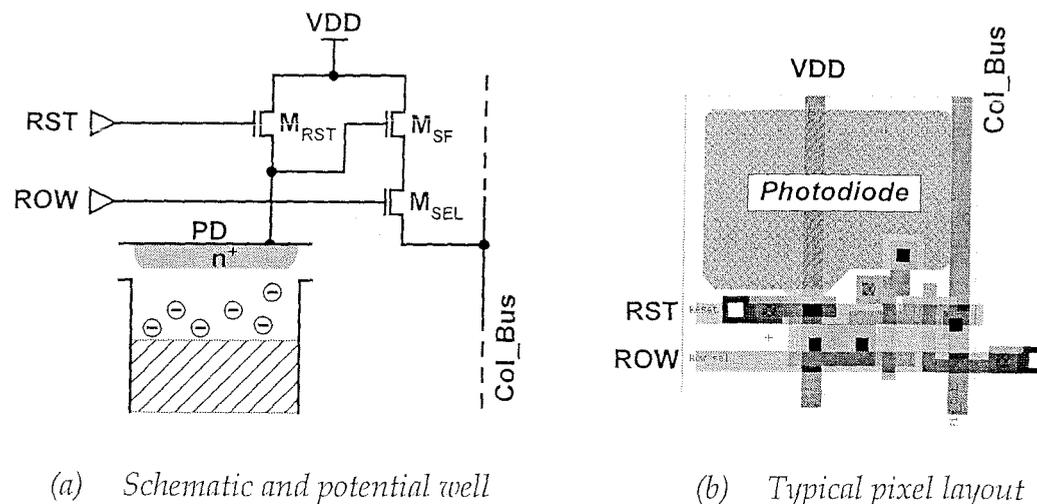


Figure 2. Photodiode-type APS pixel.

Photodiode-type APS pixel has high quantum efficiency ($\sim 50\%$ at 500 nm wavelength) as it has high fill factor (35 % to 55 %) and there is no overlaying polysilicon. The read noise is limited by the reset noise on the photodiode since correlated double sampling (CDS) is not easily implemented, and is typically 35 to 60 electrons, r.m.s. The fill factor (i.e. detector area to pixel area ratio) of photodiode-type APS pixel is typically 35 to 55 %. Comparing to photogate APS, photodiode APS has higher full-well capacity ($\sim 500,000$ electrons) and lower conversion gain, it is suitable for high-light level detector.

2.2 Readout of the Pixel Array

Readout of the pixel array is performed in a row-at-a-time mode. Figure 4 shows the schematic of pixel output voltage sample-and-hold circuit that is located at the bottom of each column of pixels. The load transistor (M_{LOAD}) of the pixel source-follower is biased at a DC voltage V_{LN} . Each pixel source follower feeds into two capacitors C_{SIG} and C_{RST} through the switches M_{SWS} and M_{SWR} , respectively.

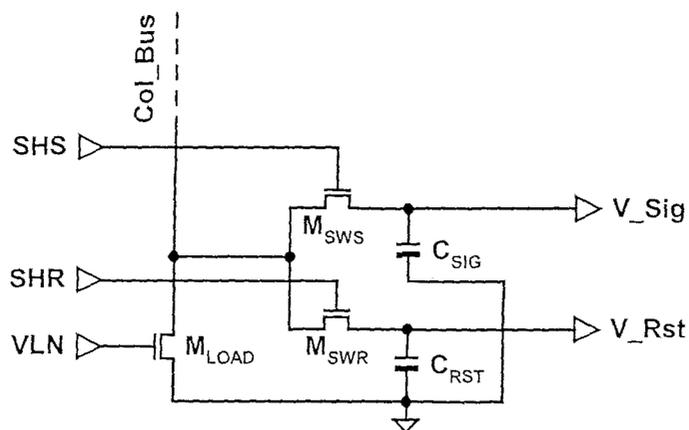
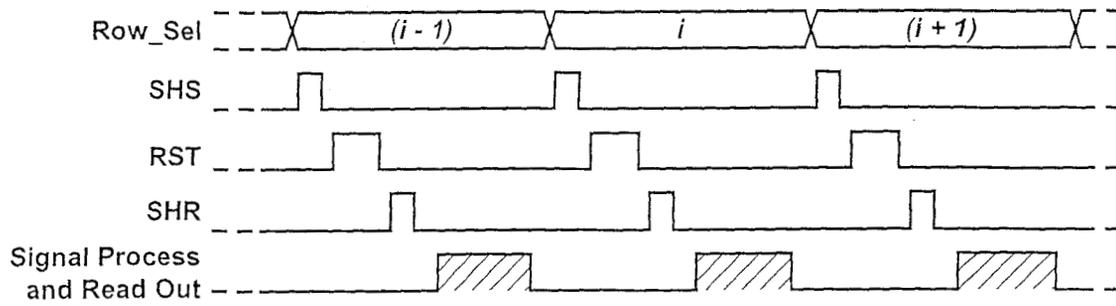


Figure 4. Schematic of column based pixel sample-and-holding circuit.

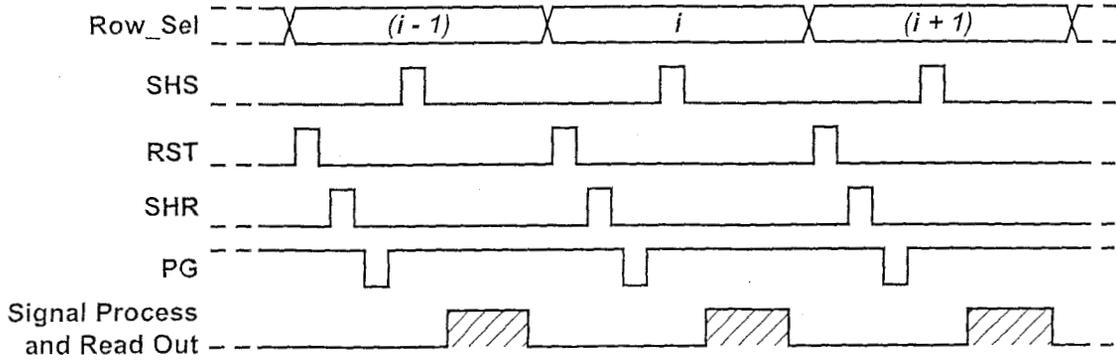
The signal voltage (V_Sig) and reset voltage (V_Rst) from each pixel are sampled to capacitors C_{SIG} and C_{RST} , before they are processed and read out. Figures 5(a) and 5(b) show the timing diagram of the pixel array readout operation of photodiode-type APS and photogate-type APS, respectively. After one row of pixel signals has been processed in column parallel mode (an entire row at a time) and read out in column-at-a-time mode, the row pointer moves to the next row. This process continues until the whole pixel array has been read out.

2.3 Analog Signal Output

The typical dynamic range of a CMOS APS imager pixel is 13 to 14 bits. However, considering the power dissipation and silicon real estate, integration of an ADC with greater than 12-bit resolution with APS sensor is very difficult. Therefore, applications requiring the full dynamic range of an APS imager (e.g. scientific imager) use imagers with analog output with off-chip digitization. Nevertheless, the signal dynamic range is determined in part by the analog signal chain. There are several analog circuit approaches such as source follower readout, capacitive-trans-impedance-amplifier (CTIA) readout, etc. Additionally, on-chip analog signal processing can be used to improve the performance of the CMOS APS.



(a) Photodiode-type APS



(b) Photogate-type APS

Figure 5. Timing diagram of the pixel array readout operation.

JPL has developed a delta-difference sampling (DDS) approach to remove offsets due to the column drives, and hence reduces column-to-column FPN. In combining with source follower output, this approach can suppress FPN peak-to-peak to 0.1 % of saturation level [11]. Figure 6 gives the schematic of source follower analog output signal chain with DDS approach. The DDS circuit calculates the difference between the voltages from two consecutive reads per channel. During the first read, the voltage on one of the column capacitors (C_{SIG} for instance) is read out, and stored on the coupling capacitor (C_{COS}). Following this, the DDS switch is enable to short the two capacitors C_{SIG} and C_{RST} . The output of the DDS circuit is the difference between the voltage on the capacitor before and after the short. If V_{Sig} and V_{Rst} are the voltages on the capacitors C_{SIG} and C_{RST} respectively before the DDS short, then the output of the chip is given by,

$$VS_Out = \gamma \left\{ V_{CL} + \beta \left[\alpha \cdot \frac{(V_{Sig} - V_{Rst})}{2} \right] - V_{TS} \right\} \quad (1)$$

$$VR_Out = \gamma \left\{ V_{CL} + \beta \left[\alpha \cdot \frac{(V_{Rst} - V_{Sig})}{2} \right] - V_{TR} \right\} \quad (2)$$

where, γ is the gain of the p-channel output driver, β is the gain of the p-channel column drivers, α is the gain of the pixel source follower. V_{CL} is the clamp potential, and V_{TS} and V_{TR} are the threshold voltages of output source followers. It can be seen from equation (1) and (2) that the resultant output signals are free from any dependence of the individual threshold of the p-channel column drivers, and hence free from column FPN.

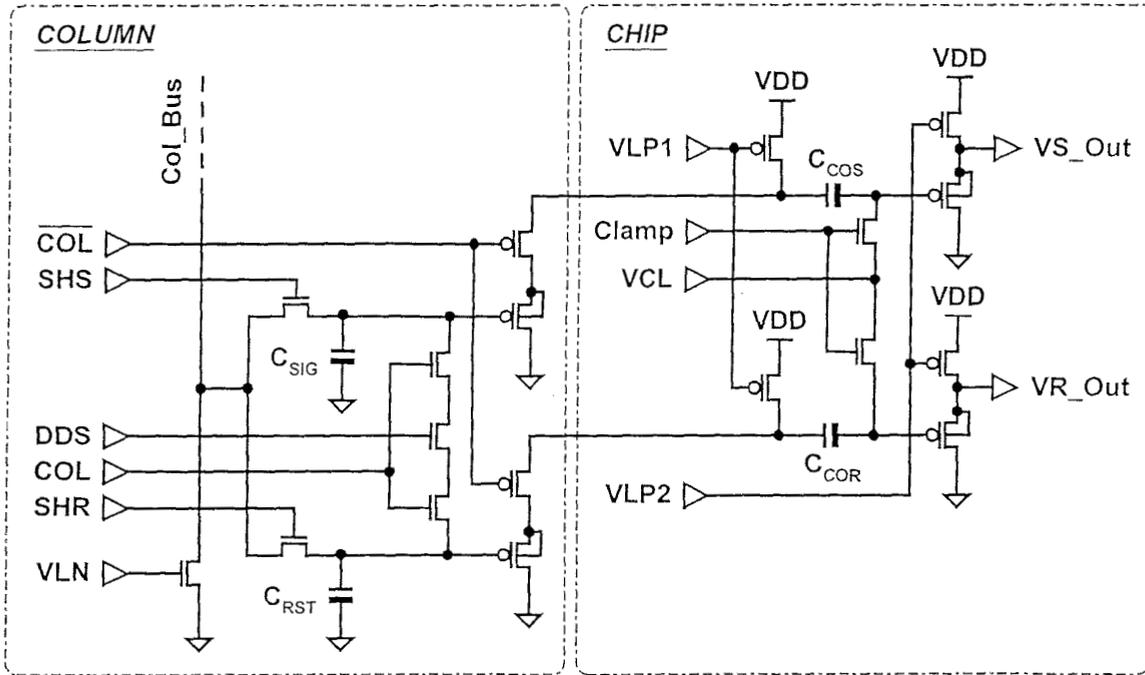


Figure 6. Schematic of source follower analog output signal chain with DDS approach.

A source follower analog output approach has low power dissipation and excellent linearity. However, its output data rate is ~ 1 Megapixel/sec, relatively slow for large format image sensor applications. On the other hand, a CTIA readout approach, using operational amplifier (OPAMP), can increase the data rate in a factor of about 10 with the cost of the amplifier power dissipation.

Figure 7 shows the schematic of a CTIA readout approach. To complete the readout of one row of pixels, the signals stored on the capacitors C_{SIG} and C_{RST} are scanned out by successively enabling the column select switch (COL). Once a particular column is selected, capacitors in that column are connected to the global switched capacitor amplifier, providing differential imager outputs. The global switched-capacitor amplifier consists of two differential OPAMPs, feedback capacitors (C_{OS} and C_{OR}). The feedback capacitors are reset to a common mode bias V_{CM0} before the readout of each column of data. If V_{Sig} and V_{Rst} are the voltages on the capacitors C_{SIG} and C_{RST} respectively before the column select switch turns on, then the output of the chip is given by,

$$VS_Out = V_{CM0} - \frac{C_{SIG}}{C_{OS}}(V_Sig - V_{CM0}) + V_{OFF_S} \quad (3)$$

$$VR_Out = V_{CM0} - \frac{C_{RST}}{C_{OS}}(V_Rst - V_{CM0}) + V_{OFF_R} \quad (4)$$

where, V_{OFF_S} and V_{OFF_R} are offsets due to threshold mismatches in signal branch and reset branch, respectively. The gain of the output stage can be controlled by changing the ratio of feedback capacitors to sample/holding capacitors (i.e. C_{SIG}/C_{OS} and C_{RST}/C_{OR}).

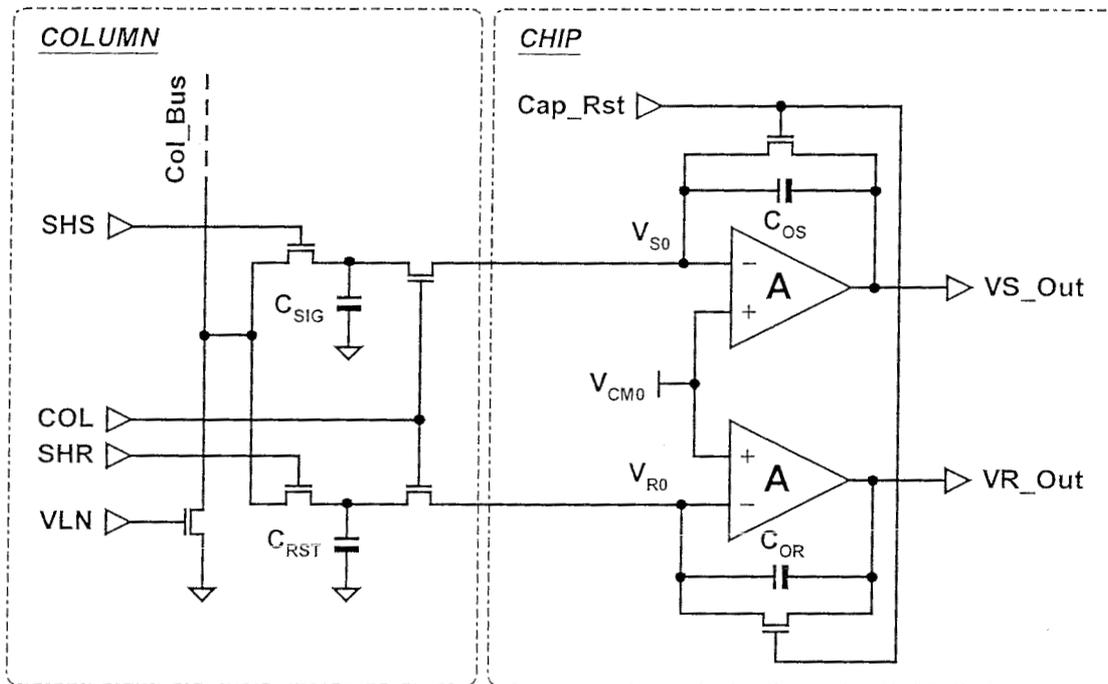


Figure 7. Schematic of a CTIA readout approach.

2.4 On-Chip Analog to Digital Converter

On-chip analog to digital converter (ADC) is desired for image sensors to achieve a single chip imaging system. One of the most significant benefits of a CMOS-based image sensor is its easy integration of such features. The ADC is desired to have low power dissipation, not occupy too much chip area, and achieve at least 8-bit resolution at 10 Megapixel/sec data rate. Many different architectures are possible as the design trade space is relatively flat [12]. It is possible to have a single ADC for the entire array operating at high conversion rate (such as pipeline ADC), an ADC for each pixel operating at frame rate (such as single-slope ADC), or an ADC for each column of the array (such as single-slope ADC, successive approximation ADC). The latter architecture is referred to as column-parallel and represents a good trade off between parallelism and chip

area for low power. JPL has demonstrated both a column parallel 8-bit single-slope ADC integrated with a small CMOS APS imager [13], and a large array with the same ADC architecture and 10-bit dynamic range [14]. A column parallel successive approximation ADC architecture has been integrated with CMOS APS and demonstrated by JPL [15] and Photobit Corporation [16].

For low-power digitization, an all-capacitor successive approximation ADC algorithm is commonly used. To be compatible with layout constraints of the column-parallel architecture, the resolution of this type ADC implementation is usually in the range from 8 to 10 bits. Some of the design also features built-in offset correction providing low FPN. An n-bit column-ADC circuit schematic along with the bit cell [B(i)] circuit is shown in Figure 8. The ADC consists of two branches of capacitors on which the reset and signal levels from the pixels are sampled. The capacitor (C_{SIG}) on the signal side is comprised of n (number of bits, equal to ADC resolution) binary-scaled capacitors (C_i). If C_{MSB} is the largest sized capacitor used, each capacitor in the bank follows the relation,

$$C_i = \frac{C_{MSB}}{2^i}, \quad \rightarrow \quad C_{SIG} = \left[2 - \frac{1}{2^{(n-1)}} \right] \cdot C_{MSB} \quad (5)$$

Each bit cell consists of a latch that controls the potential at the bottom-plate of the capacitor connected to it. Pulsing the bottom plate of a capacitor C_i to V_{REF} raises the voltage on C_{SIG} by the capacitive divider ratio or equal to $V_{REF} / 2^i$. The capacitors are buffered by two source-followers before being fed to the comparator circuit.

The ADC operates as follows. First, the reset (V_{Rst}) and signal (V_{Sig}) values are sampled with respect to ground on C_{REF} and C_{SIG} , respectively. The ADC operation consists of successively adding binary-scaled voltages to the signal side (V_{Sig}) while comparing the result to the reset side voltage (V_{Rst}), and registering the digital codes necessary to generate the voltage pattern. If at the i-th cycle, voltage on C_{SIG} is greater than that on C_{RST} , the i-th bit cell output is latched to a logic level "1" by pulsing set, and the voltage on C_{SIG} is returned to its original value. Otherwise, the bit cell logic latches the output to logic "0". The comparator output is also stored in the appropriate data latch [i.e. D(0) to D(n-1)] at the bottom of the column. Digitization is completed after n repetitions, with bit cells representing digital code. Since the ADC digitizes the difference of V_{Rst} and V_{Sig} , it is inherently immune to pixel threshold mismatches.

In order to cancel the offset generated by the buffer source followers and the comparator, a calibration phase can be used. During this phase, the same signal is sampled on both capacitors, and then digitized. Ideally the digital code is "0". Thus, the ADC output in the calibration phase is the digital representation of the

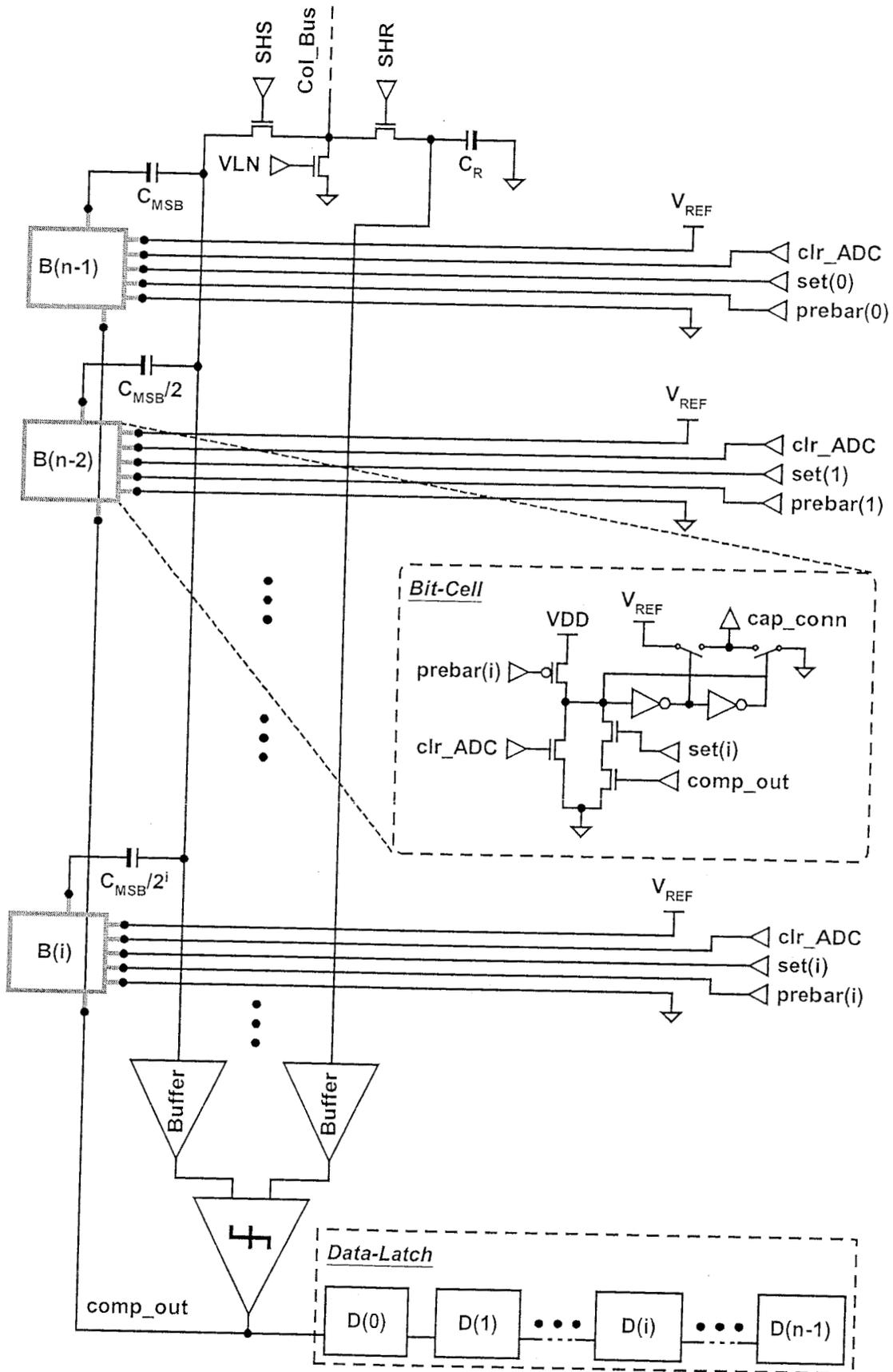


Figure 8. All-capacitor successive approximation ADC implementation with the bit-cell circuit.

offset between the two branches. The ADC outputs are stored in offset latches at the bottom of the column. By subtracting the offset code from the pixel ADC code during data readout, offset free digitization is realized, and FPN is minimized.

2.5 Other On-Chip Analog and Digital Circuits

Compatibility of CMOS APS with standard CMOS process enables the integration of timing and control circuit with imager array that greatly reduces the complexity of off-chip control. As a result a control FPGA is not required in many cases. Furthermore, while the CMOS imager uses a single power supply (typically 3.3 V or 5 V in CMOS process), other required bias and reference voltages can be generated on chip by on-chip DACs. Additionally, on-chip analog signal processing implementations are also used to improve the CMOS APS imager functionality. Examples of signal processing demonstrated in CMOS image sensors include amplification [17], multi-resolution imaging [18], Gamma correction, gain Control [19] and on-chip centroiding [20].

3. SINGLE-CHIP, PROGRAMMABLE DIGITAL CMOS IMAGER

JPL has been developing large format, low-power, single-chip CMOS digital imagers capable of reproducing high quality images since 1995 [21, 22]. The 512×512 single-chip programmable digital CMOS imager reported in this section requires a single power supply (3.3 V), consumes only 6 mW of power at video rates, is capable of operation with read noise < 40 electrons in photodiode-type pixel approach. This chip has a simple digital interface and requires a minimum of 5 wires (i.e. VDD, Ground, Digital-In, Digital-Out, and Clock). The one-chip digital imager will find ready use in a number of commercial portable applications where low-power and the availability of a simple, digital interface is of great importance.

3.1 Imager Architecture and Operation

The single-chip imager integrates the CMOS pixel array with timing and control functions, programming functions, reference generation functions (using DACs), ADC, and the analog signal chain. Figure 9 shows the schematic block diagram of the CMOS APS imager, consisting of the above mentioned function blocks. A set of input registers enables the user to select between different modes of operation such as analog or digital (serial or parallel) output, video or snapshot imaging mode, and while also allowing the user to dynamically program the exposure time, electronic pan and zoom setting, speed and bias control.

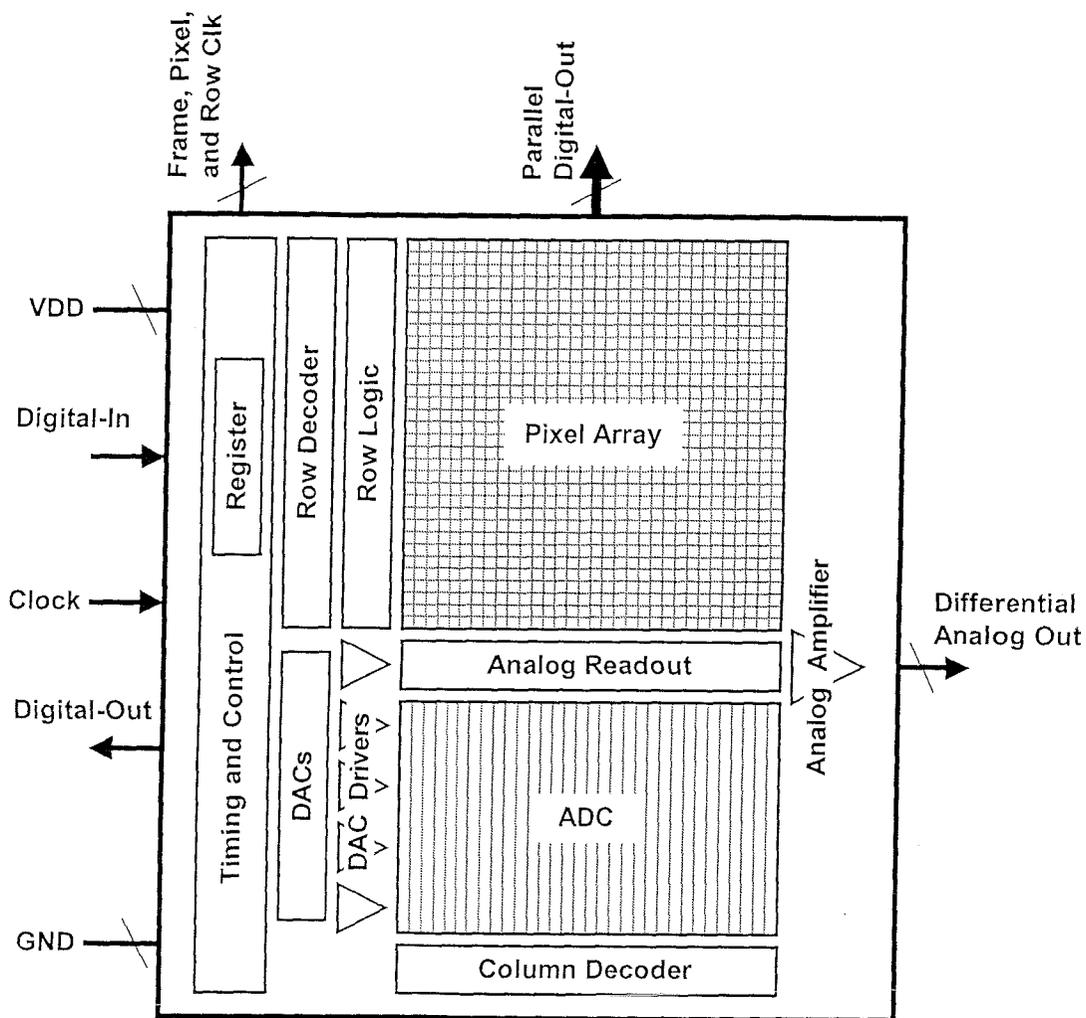


Figure 9. Schematic block diagram of the single-chip imager.

This chip uses the photodiode pixel approach described in Section 2.1 with pixel size of $12\text{-}\mu\text{m}\times 12\text{-}\mu\text{m}$, combined with the source follower analog signal chain described in Section 2.3, and is designed for high-resolution applications. A 10-bit column parallel successive approximation ADC discussed in Section 2.4 has also been implemented on-chip. The bias and reference generation block consists of six 5-bit multiplying DACs to provide the required reference voltages and bias currents. In addition, a new hard-to-soft (HTS) reset scheme that allows imager operation high linearity at low light levels without any observable image lag and extends the operational dynamic range, has been implemented on this chip^[23]. The schematics of the column based HTS reset scheme circuit implementation with photodiode pixel and column signal chain is shown in Figure 10.

The exposure time in digital still imaging or in slow-scan imaging can vary over a large scale from 100 msec to > 10 sec. In order to set the exposure time and the frame-read time independently, and to achieve variable exposure time, the imager is designed to operate with a two-pointer addressing scheme, a pointer

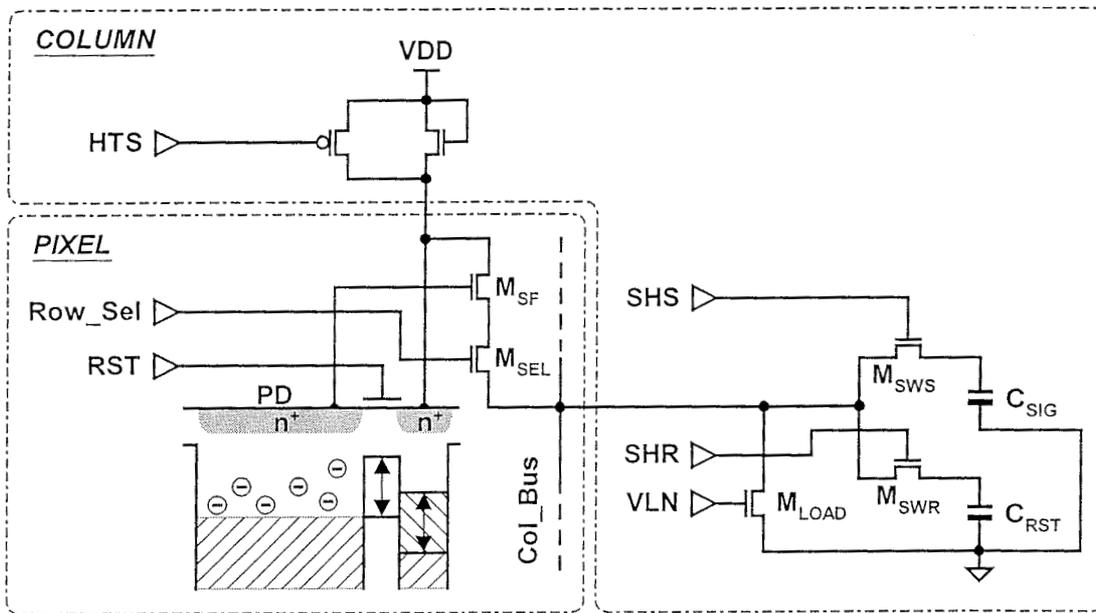


Figure 10. Schematics of the column based HTS reset scheme circuit implementation with photodiode pixel and column signal chain.

being a decoded row address. The first pointer causes a row of pixels to begin integration, and the second pointer causes it to end integration, and execute a row-read sequence. Thus, the exposure time (T_{INT}) is determined by the temporal spacing of the integration and read pointers for the same row. Since integration and readout of different rows are interleaved, a typical row phase consists of four sub-phases: (1) initiation of integration for row m , (2) pixel readout for row $m-k$, (3) parallel digitization of the row of pixels, and (4) digital data out, as shown in Figure 11.

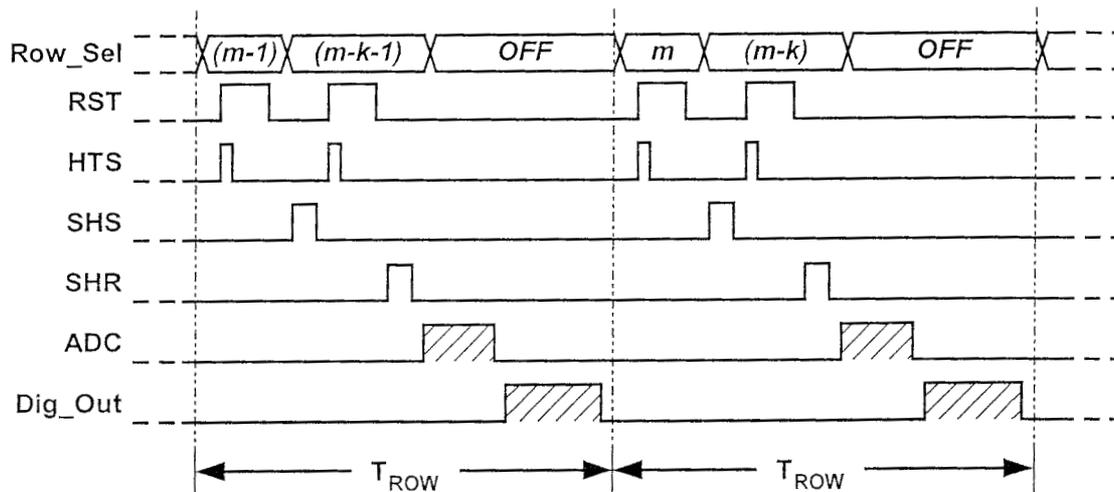


Figure 11. Pixel and row timing diagram.

Frame time of the imager is primarily determined by the output clocking speed (t_{READ}), with t_{SH} (sample and hold time) and t_{ADC} (ADC time) being a small

fraction of T_{ROW} (one row operation time), especially if the digital imager is read out in serial mode.

3.2 Imager Performance

Figure 12 shows the die microphotograph of the 512×512 digital camera-on-a-chip. The chip occupies an area of 10-mm×15-mm, with the imager area being 6-mm×6-mm, and the ADC area is 6-mm×5-mm. The pixel pitch is 12- μm ×12- μm , with drawn optical fill-factor of 38 %. The ADC array takes up a large amount of area since accurate capacitance matching is desired. The chip provides digital video data (8 Megapixel/sec) at an ultra-low power of 6 mW, while producing high quality image. Figure 13 is a reproduction of the digital image captured with the one-chip imager.

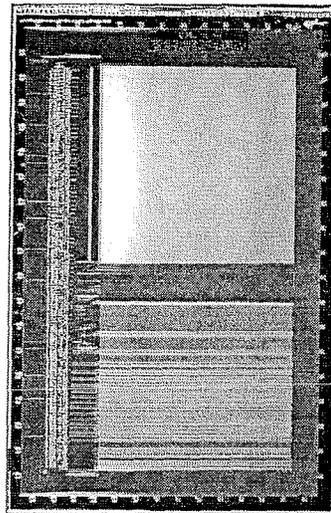


Figure 12. Microphotograph of the 512×512 digital camera-on-a-chip.

Unlike other CMOS imagers, no image artifacts such as column-to-column FPN are visible, and the pixel response non-uniformity is less than 1 % (typical of a camcorder-type imager). The column-to-column FPN, measured from a flat field, is less than 1.0 LSB across the array at low-light levels. By employing HTS reset scheme, good optical response with excellent low-light-level response linearity is achieved. The peak quantum efficiency at 550 nm wavelength is 42 %, indicating good optical collection. The measured ADC is highly linear, with most of the non-linearity shows up at major transition codes, but is less than 0.5 LSB over the entire input range. The CMOS imager performance, summarized in Table 1, is commensurate with high quality imaging requirements.

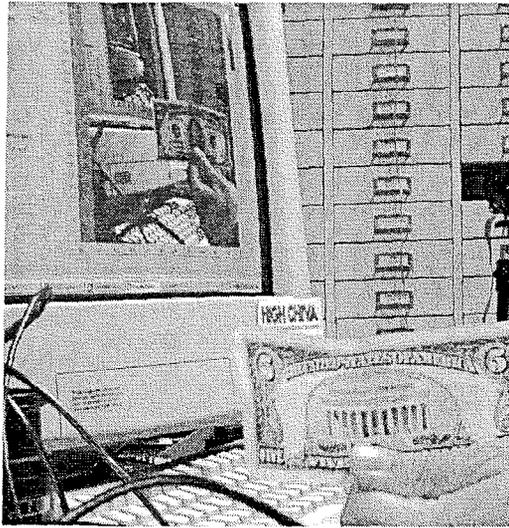


Figure 13. Digital image captured with the one-chip imager.

Table 1. 512×512 APS camera-on-a-chip performance summary

| Imager Characteristics | Values | Comments |
|---------------------------|----------------------------------|---------------------|
| <i>Technology</i> | CMOS, 0.5- μ m, 1P3M | |
| <i>Outputs</i> | analog and digital | |
| <i>Array format</i> | 512×512 | |
| <i>Pixel size</i> | 12- μ m×12- μ m | |
| <i>Responsivity</i> | 4 μ V/photon | @ 550 nm wavelength |
| <i>Quantum efficiency</i> | 42 % | for the total pixel |
| <i>Dark current</i> | 500 pA/cm ² for PD | @ room temperature |
| <i>Noise</i> | 40 e ⁻ for photodiode | |
| <i>Full well</i> | 250,000 e ⁻ for PD | |
| <i>ADC resolution</i> | 10 bits | 9.3 effective bits |
| <i>ADC DNL max.</i> | 0.46 LSB | |
| <i>Power</i> | 6 mW | @ 8 Megapixel/sec |
| <i>Power supply</i> | 3.3 V | single power supply |
| <i>Timing and control</i> | on-chip | |

A digital micro-miniature camera implemented using this CMOS one-chip digital imager is shown in Figure 14. The total volume of the camera including optics is 5 cm³ and is comprised mostly of optics. The optics size can be further reduced, allowing “wrist-watch” type cameras. The micro-miniature programmable camera consists of a miniature lens glued to a single digital imager chip that interfaces with only 5 wires (VDD, Ground, Clock, and serial Digital-In, Digital-Out). The camera requires only one power supply to operate and dissipates less than 10 mW of power driving a standard RS232 interface.

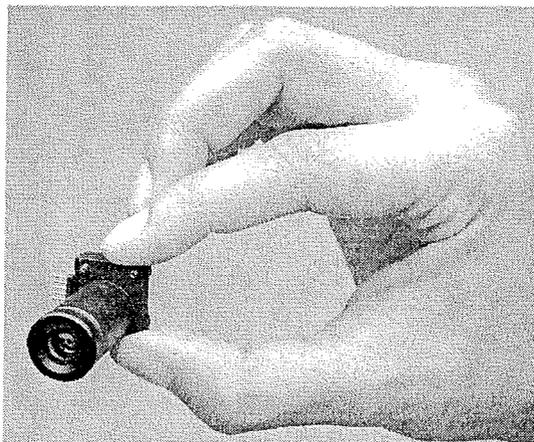


Figure 14. Miniature digital one-chip camera.

4. DEVELOPMENT AND CUSTOM DESIGNED CMOS APS

Since the early 1990's, JPL has been working on the development of CMOS APS technology with the integration of various on-chip data processing circuits with CMOS APS array for an expanding array of applications. Some of these developments are reported in this section.

4.1 Snapshot APS for High Speed Imaging

Until recently, most CMOS imagers operated following the timing diagram shown in Figure 11. For an imager operation with an integration time of $k \times T_{\text{ROW}}$, the row operation of $(m-k)^{\text{th}}$ row includes the reset of pixels in m^{th} row and data process (i.e. sample/holding, ADC, and readout) of pixels in $(m-k)^{\text{th}}$ row. For an imager with N -row and M -column pixel array, the row integration and row operation period as a function of time is illustrated in Figure 15. This figure indicates that although all pixels in the imager have the same integration time, their integration start and end time are row dependent. In other words, the imager does not support simultaneous integration of all pixels in the imager, and the imager is said to be operating in a "rolling shutter" mode. The effect of non-simultaneous exposure is image distortion whenever there is relative motion between the imager and elements in the scene being imaged. Snapshot mode of operation overcomes this limitation by simultaneously integrating all pixels and storing that data in-pixel for readout.

A snapshot imager using a photodiode-type pixel has been demonstrated by incorporating a switched storage node inside the pixel [24, 25]. However, incomplete charge transfer leads to image lag and increased noise in these imagers. Snapshot mode of operation is also possible with pinned photodiode

pixels [26], however, requiring non-trivial modification of the standard CMOS process.

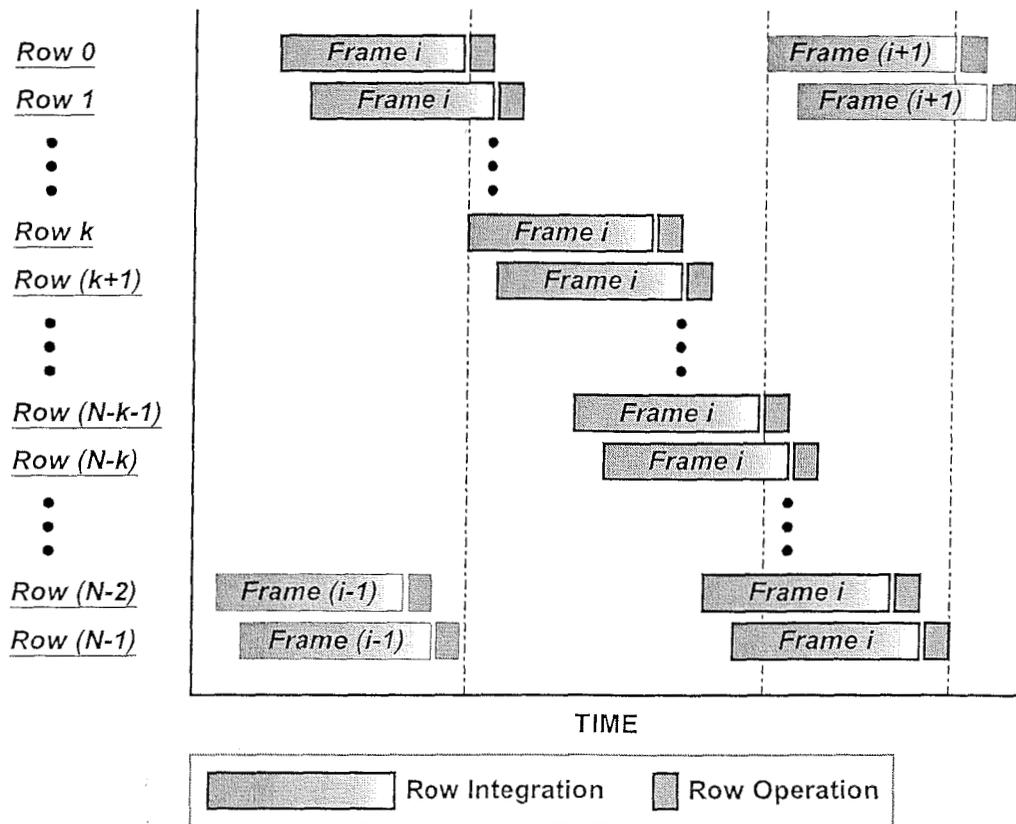


Figure 15. Row integration and row operation period as a function of time for imager with N -row and M -column pixel array.

The first photogate-type snapshot APS imager was developed at JPL and reported in 1998 [27]. The photogate pixel overcomes the above limitations by enabling complete CCD-like charge transfer to the storage node at the expense of fill factor loss due to an extra in-pixel transistor and QE loss due to the polysilicon gate. The proof-of-concept 128×128 snapshot imager has been implemented in a standard single-poly, three-metal, and n-well CMOS technology. A new pixel design and clocking scheme allow the imager to provide high-quality images without motion artifacts at high shutter speeds. Figure 16(a) shows the schematic of the snapshot imager pixel, along with the potential well diagram, and Figure 16(b) shows the layout of a snapshot pixel of $14.4\text{-}\mu\text{m}$ pitch and 27 % fill factor.

The pixel consists of a photogate (PG), two transfer gates (TG1 and TG2), a reset gate (RST), a metal-shielded sense node (FD), source follower input transistor (M_{SF}), and the row-select transistor (M_{SEL}). TG1 and TG2 are common to the entire chip and are pulsed. Snapshot imaging (or concurrent exposure of all pixels) is achieved by simultaneously transferring the integrated charges

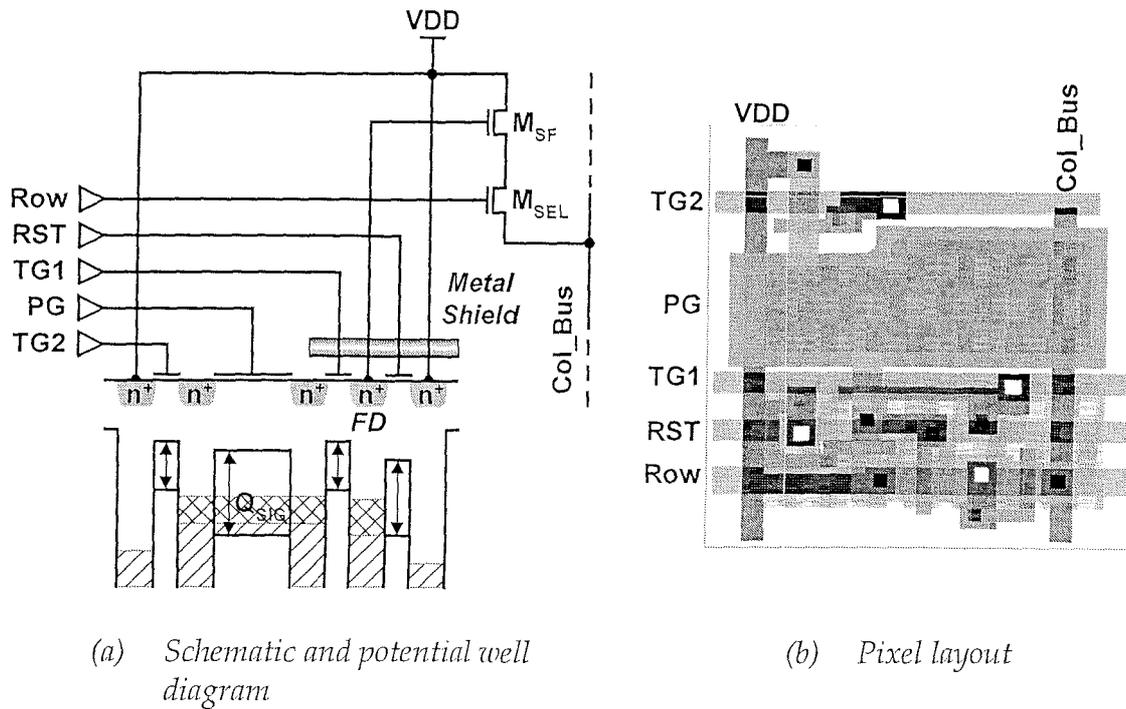
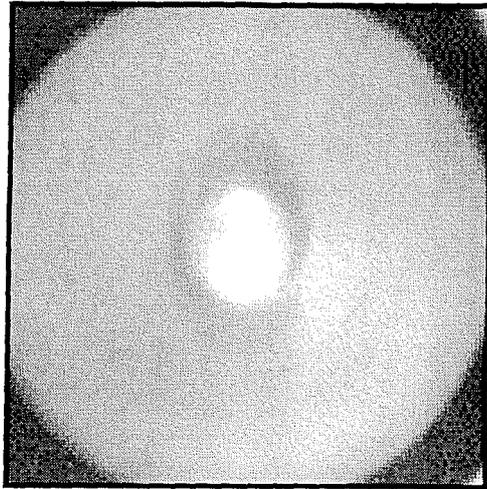


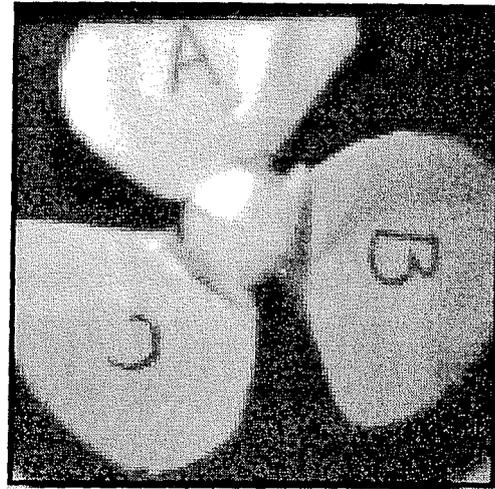
Figure 16. Snapshot pixel design of $14.4\text{-}\mu\text{m}$ pitch and 27 % fill factor.

under PG to the sense node (FD) within each pixel by momentarily pulsing TG1. The sense node provides intermediate storage for the time taken by the array complete readout in row-at-a-time manner. Thus, the imager can operate with simultaneous high-speed exposure independent of the frame read time. Since FD is isolated following a charge transfer, an additional gate (TG2) is added for controlling the integration time and providing lateral anti-blooming. Momentarily pulsing TG2 simultaneously to clear the charge under PG at anytime sets the start of integration. The resultant pixel architecture preserves the row-wise random access feature. In order to obtain the highest signal dynamic range for data analysis, source follower analog output with DDS approach is employed for readout the signal.

Figure 17 shows the snapshot mode image of a three-blade fan rotating at a high speed of 1800 r.p.m. with a long exposure time of 30 msec in (a) and a short exposure of $75\ \mu\text{sec}$ in (b). With the long exposure, the captured image is a uniformly blurred image. However, with the short exposure, the captured image virtually freezes the rotation of the fan, clearly showing the three blades. Compared to imager operation in “rolling shutter” mode, snapshot mode of imaging has eliminated row-wise distortion due to motion. The performance of the snapshot CMOS APS is summarized in Table 2.



(a) 30 msec exposure time



(b) 75 μsec exposure time

Figure 17. Snapshot mode image of a three-blade fan rotating at a high speed of 1800 r.p.m.

Table 2. Snapshot CMOS APS performance summary

| Imager Characteristics | Values | Comments |
|------------------------|------------------------------|--------------------------|
| Technology | CMOS, 0.5-μm, 1P3M | |
| Array format | 128×128 | |
| Pixel size | 14.4-μm×14.4-μm | 27 % fill factor |
| Pixel type | photogate | 6 transistors per pixel |
| Power | < 3 mW | @ 1 Megapixel/sec |
| Max. frame rate | 400 Frames/sec | |
| Minimum exposure time | 75 μsec | measured |
| Conversion gain | 25 μV/e ⁻ | |
| Linearity | 99.3 % over 90% range | |
| Fixed pattern noise | 0.1% | after DDS correction |
| Read noise | 4.5 electrons | |
| Full well | 37,000 electrons | |
| Dynamic range | 78.3 dB | |
| Quantum efficiency | 19 % | @ 550 nm wavelength |
| Dark rate | 30 - 77 pA/cm ² . | @ room temperature |
| Image lag | Immeasurable | |
| Blooming | None observed | @ 40 dB above saturation |
| Light leakage to FD | 5 % | |

4.2 CMOS Imager with On-Chip High-Speed Windowed Centroiding Capability

For many years, JPL has been working on integrating analog signal processing with CMOS APS to improve the functionality of the imager for different applications. One of the works reported in 1999 is CMOS imager with on-chip high-speed windowed centroiding capability^[20]. Low-power, high-speed, accurate computation of centroid from a pre-defined window in the image plane is important for a number of space-based and commercial applications. These include object tracking in robotic systems^[28], space guidance and navigation systems^[29], and deep-space optical communication systems that require accurate and stable beam pointing for high speed data transfer^[30].

In this work, we developed an APS with an integrated centroid-computation circuit that allows accurate X and Y centroid computation from a user-selectable window of interest. Such an imager offers real-time centroid computation while dissipating low-power and realizing a miniature tracking system. The architecture of the windowed-centroiding APS is shown in Figure 18. It consists of a 2-D imager array, a switching network, inner-product (IP) computation circuits, and an analog divider. On-chip 2-D centroid computation is carried out by first computing the relevant inner-products (weighted sums) for a given row. Upon completion of all row-wise IPs, these values are used to generate the final X and Y IP as shown in Figure 18. A single divider circuit is then used to generate the X and Y centroids.

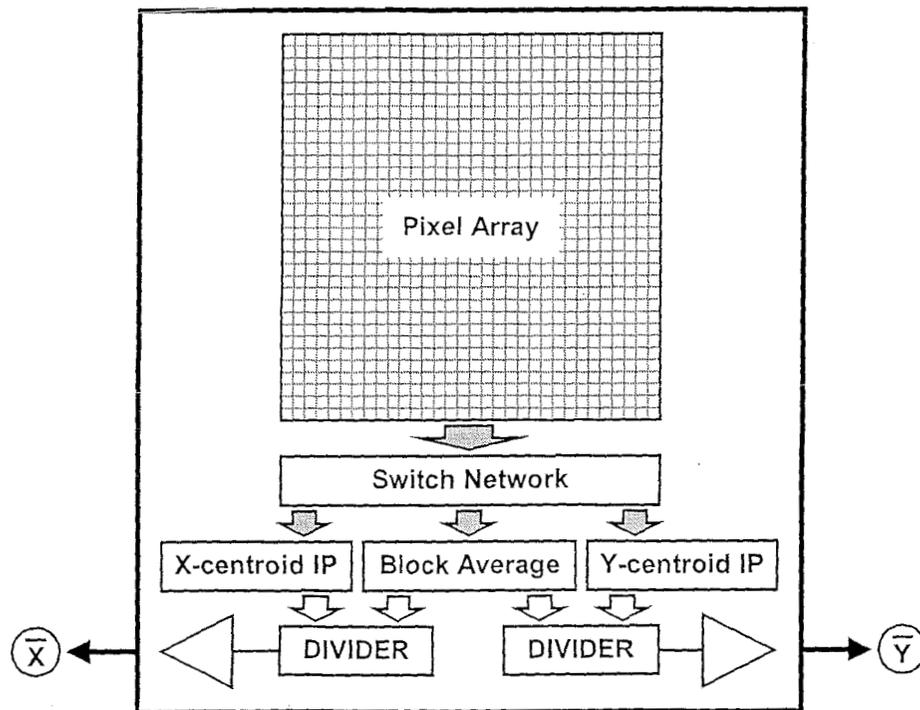


Figure 18. Block diagram of windowed-centroiding APS

The X- and the Y-centroids computed by the on-focal-plane circuits are given by:

$$\overline{X}_{n \times n} = \frac{2 \cdot (n+1)}{[n(n-1)+2]} \cdot \frac{\sum_{i=1}^n \sum_{j=1}^n x_{j-1} v_{ij}}{\sum_{i=1}^n \sum_{j=1}^n v_{ij}} \quad (6)$$

$$\overline{Y}_{n \times n} = \frac{2}{(n-1)} \cdot \frac{\sum_{i=1}^n y_{i-1} \sum_{j=1}^n v_{ij}}{\sum_{i=1}^n \sum_{j=1}^n v_{ij}} \quad (7)$$

where x_i , and $y_j = 1, 2, 3, \dots, n-1$, respectively, v_{ij} is the voltage of each pixel. Apart from a scaling pre-factor, both computations yield the correct value of the respective centroids.

For low-power operation, only capacitors and switches are used to perform the computation of X-centroid IP and Y-centroid-IP [18], with different sized capacitors representing different weights. A switching network consisting of $N \times 9$ (N is the imager format) switching array connects 9 consecutive columns of the imager array with user selected column start address into the computation circuit. This allows centroid computation for blocks of size 3×3 to 9×9 . Thus, the computation is performed in parallel with the imager readout, leading to a high computation speed and minimal computational overhead.

Figure 19 shows the chip photograph of the prototype imager of 128×128 format. Computation circuits take up only a small area of $1.7\text{-mm} \times 0.9\text{-mm}$, irrespective of the imager format. The imager was fabricated using $0.5\text{-}\mu\text{m}$ one-poly three-metal CMOS technology with a $12\text{-}\mu\text{m}$ pixel pitch, and has two ports: one for centroid output and the other for imager output. Use of passive components and only one OPAMP (for the divider circuit) enable low power ($< 2\text{ mW}$) operation.

In order measure the centroiding accuracy, image centroid was computed separately by acquiring the raw data from the imager port. The computed centroid was then compared against the value obtained from the centroid port, and relative error (in pixels) was computed. The measurements were repeated for different window sizes, centroid values, mean signal strengths, and from different regions of the imager. It was found that a typical centroid error of 0.02 pixel was achieved over most of the array, the worst case error being around 0.07

pixel for the smallest sized (3x3) window, as shown in Figure 20. Figure 20 shows the smallest and the largest centroid error measured from the array. The error dependence on the window size was not large, although in general, the error was found to be lower for larger sized windows. The window centroiding update rate is about 20-50 kHz that makes the chip suitable for use in real-time image-based control systems.

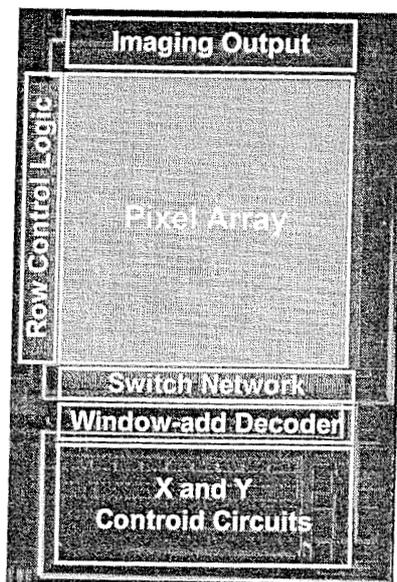


Figure 19. Chip Photograph of the 128x128 CMOS APS centroid chip.

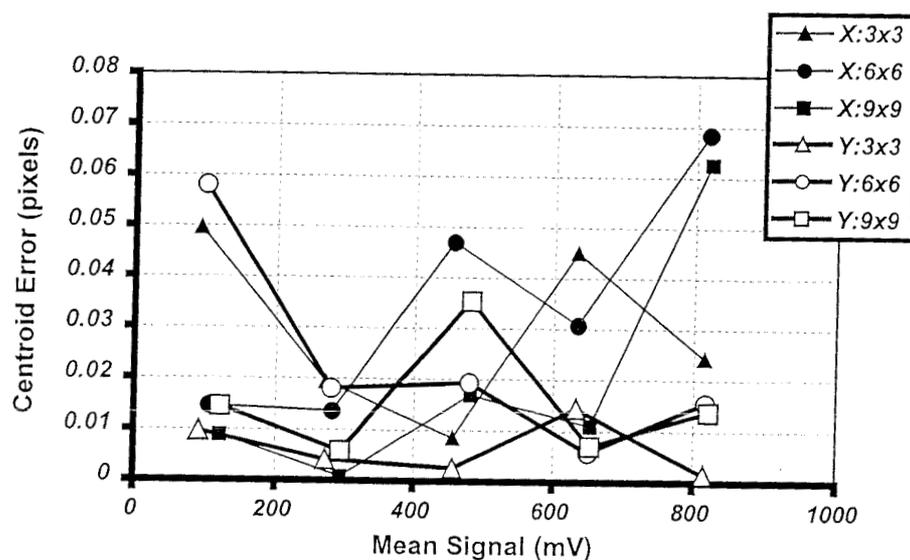


Figure 20. Centroid error as a function of average signal strength. (for selected window sizes).

4.3 Dynamically Reconfigurable Vision CMOS APS Imager

Another work on integrating analog signal processing with CMOS APS developed at JPL reported in 2001 is dynamically reconfigurable vision (DRV) CMOS APS imager for real-time staring vision systems [31]. Active vision systems are of great interest in realizing autonomous systems ranging from commercial to surveillance, military, and future space applications. The complexity of an active vision system arises from the fact that it concurrently carries out a number of diverse visual tasks, such as search, detection, recognition, and multi-target tracking. Search requires wide field-of-view (FOV), tracking requires fast frame rate data output from regions of interest (ROI), recognition requires high spatial resolution, while multi-target cueing requires all three of them concurrently. These cannot be easily handled by imaging systems with conventional image sensors due to the serial nature of pixel access and the enormity of the data volume. For example, a large FOV system consisting of a million pixels, operating with an update rate of 1 kHz digitized to 10 bits will require a data output rate at a prohibitively high data rate of 10 Gigabits per second, not to mention the enormity of data storage needed. Moreover, data processing complexity grows as a function of n^M , where n is the number of pixels output to the off-chip processor, and $M > 1$. Thus, the elimination of data-redundancy is critical for realization of real-time, miniature active vision systems with low-power dissipation.

The multi-acuity, multi-window DRV CMOS imager developed at JPL is suitable for reconfigurable vision system applications. The imager is capable of simultaneously providing data from three partially overlapping ROIs, with the locations and resolutions of the ROIs being dynamically reconfigurable by the user. The imager is capable of operation in tracking mode at > 1 kHz update rates. By allowing placement of the high resolution "fovea" anywhere within the FOV, the imager enables a low-power staring active vision system that meets the diverse and conflicting requirement of search, identify and track modes.

The prototype DRV imager has been implemented in a 0.5- μm n-well one-poly three-metal process. The schematic block diagram of the imager is shown in Figure 21. It consists of a CMOS pixel array, integrated column-parallel signal processing circuits at the top and bottom of the imagers, column and row control circuits, digital I/O interface, and a minimum amount of required operation control logic. Two of the ROIs (window-2 and window-3) are controlled by the control blocks located at the bottom of the pixel array and are output from port-2, while window-1 is controlled by the control blocks located at the top of the pixel array and is output from port-1. The architecture does not require any modification of the pixel array, since variable ROI resolution is accomplished through column-parallel circuits. This permits multi-resolution output without sacrificing imaging performance. Variable resolution ROI or a super-pixel (SP) is

implemented by averaging a block of $n \times n$ neighboring of pixels, using a column-parallel switched capacitor array to carry out passive averaging [18].

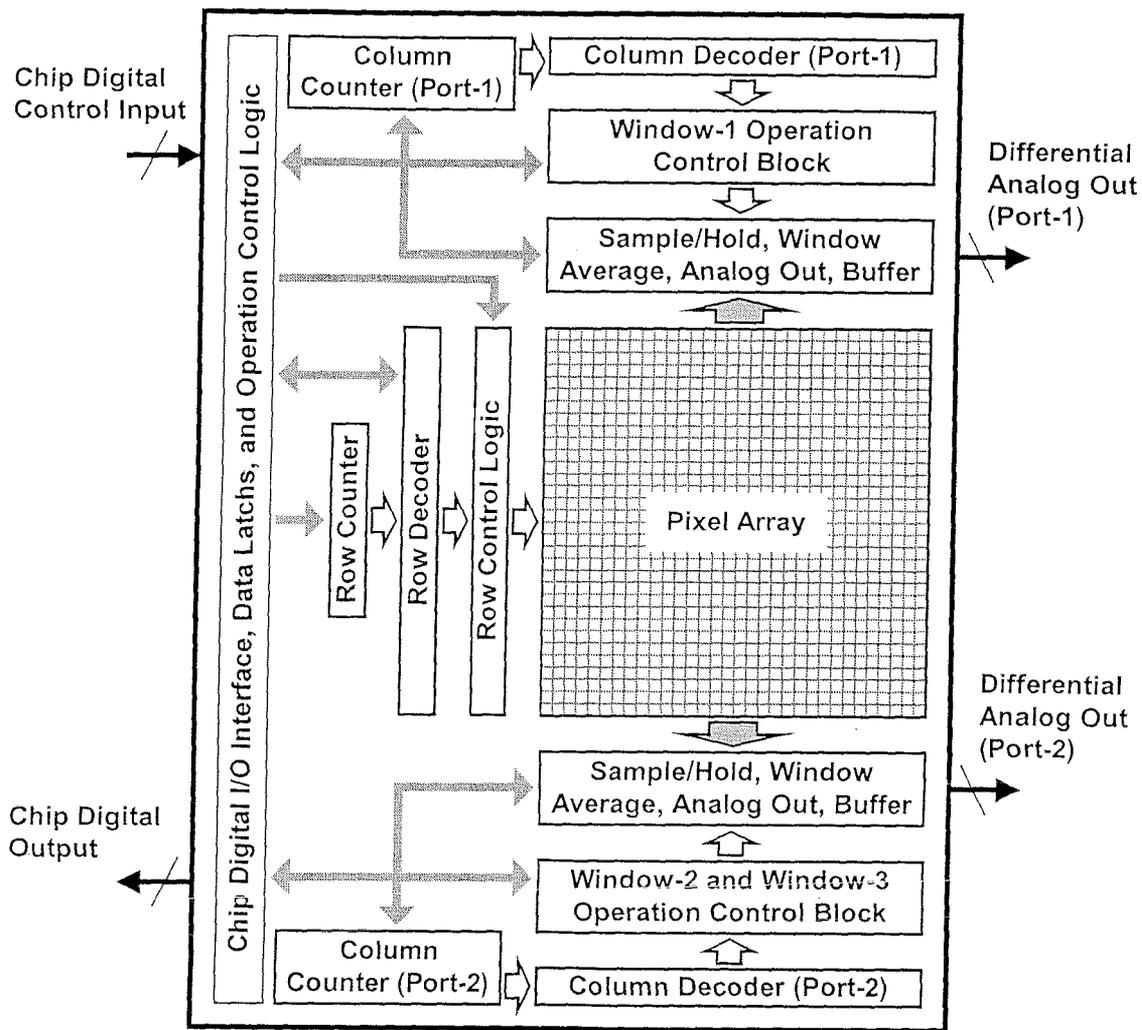


Figure 21. Schematic block diagram of the DRV imager.

The imager is designed to support only a set of binary selectable ROI resolutions, with the resolutions scaled in a binary fashion from 1×1 to 32×32 . Thus, there are six different super-pixel resolution settings, multiple adjoining super-pixels can be grouped together to create arbitrarily large ROIs. The ROI-1 (window-1) can overlap with ROI-2 (window-2) and ROI-3 (window-3).

Unlike a conventional imager, the DRV imager requires special column control logic signals in order to configure the ROIs and generate super-pixel data. Six control bits per column are needed for each ROI to control the row-averaging, column-averaging and readout functions. Since the ROIs can have arbitrary starting positions and sizes, as well as different resolutions (i.e. super-pixel depths), the control bit pattern for each ROI is different. Individual ROI bit-

patterns are separately generated, followed by multiplexing and latching on column-latches for simultaneous control of the ROIs.

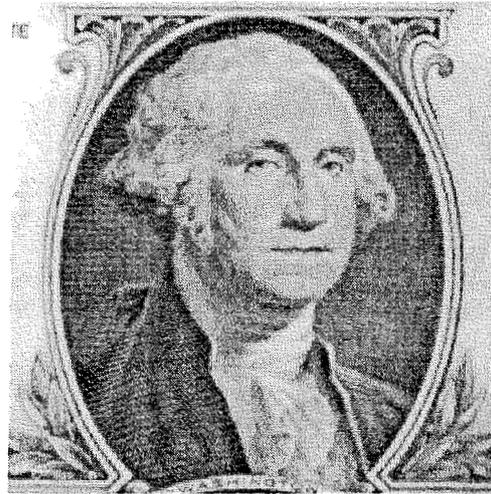


Figure 22. 256×256 image captured by DRV imager in snapshot mode of operation.

Table 3. DRV imager performance characteristics and important experimental results

| Characteristics | Values | Comments |
|--------------------------|--------------------------------------|---------------------------|
| Technology | CMOS, 0.5- μm , 1P3M | |
| Imager format | 256×256 | |
| Pixel type | photogate | snapshot operation |
| Pixel size | 15- μm ×15- μm | |
| No. of simultaneous ROIs | 3 | |
| Max. update rate | 100 kHz | |
| Super-pixel sizes | 1×1, 2×2, 4×4, 8×8, 16×16, and 32×32 | 6 super-pixel resolutions |
| Averaging error | < 0.7% | |
| Quantum efficiency | 22 % | @ 550 nm |
| Full well | 45,000 e ⁻ | |
| Noise | < 7 electrons | @ 2MHz data output rate |
| Dynamic range | > 75 dB | for short-exposure time |
| Imager FPN | ~ 0.1% of imager saturation level | not visible |
| Dark current | 100 pA/cm ² | @ room temperature |

More than 100Hz frame rate has been achieved at all window sizes and super-pixel resolutions. A very high update rate of 10 kHz was reached for an ROI consisting of 10×10 super-pixels, with each super-pixel consisting of block-

averaged 4×4 pixels. Averaging error was found to be less than 0.7 %, and to depend only slightly on the super-pixel size. Figure 22 shows the image captured in snapshot mode. Table 3 summarizes the performance characteristics and important experimental results of the DRV imager.

A prototype DRV unit was built around the DRV imager. It consists of the DRV camera, a host laptop, and an ethernet data link. The host displays video from 3 concurrent DRV windows over a fast Ethernet (100 Mbps) data link. Overall timing and control signals are provided by an embedded programmable logic device (PLD). Figure 23 shows the picture of the camera unit, and Figure 24 demonstrates the operation of the unit with simultaneous display of lower-resolution wide FOV and high-resolution narrow ROI imagery. A template-based external tracking scheme was used to continuously track the two persons in the FOV at 25 frames per second [32].

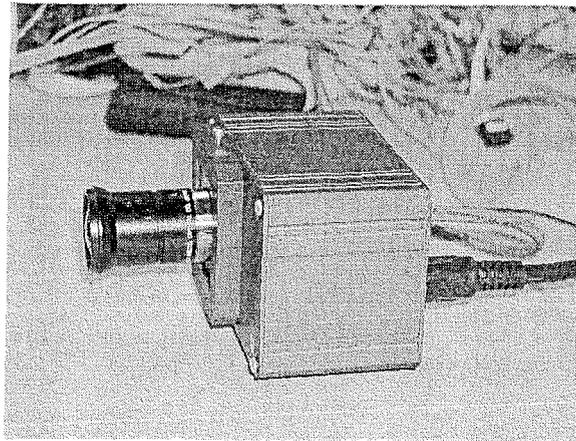


Figure 23. Photograph of the DRV demonstration unit.



Figure 24. Three frames of DRV image data from windows. One window operates at low-resolution wide FOV, and the other two embedded within the FOV operates at higher resolution narrow ROI.

4.4 Large Format CMOS APS

Low power, simple interface, large format APS with high image quality has widely applications, especially in consumer electronics for HDTV camcorders and large format digital still cameras. JPL developed a 1K×1K CMOS APS with analog and digital outputs that has been reported in 1997 [14]. Recently, a 1K×1K APS has been implemented in a 0.5- μm two-poly three-metal twin-well CMOS process. This imager integrated digital interface, control logic with n-well based photodiode pixel array, using conventional source follower output as well as high speed CTIA output. Both output schemes has been discussed in Section 2.3. Figure 25 shows the schematic block diagram of the 1K×1K APS imager.

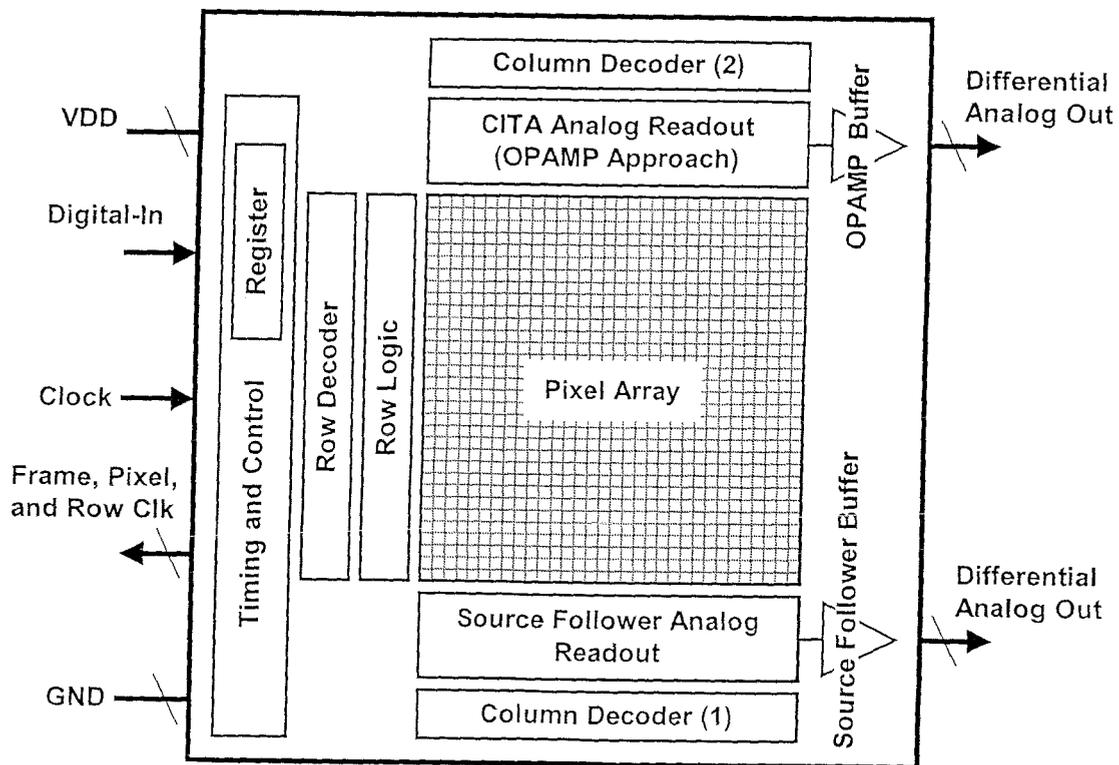


Figure 25. Schematic block diagram of 1K×1K CMOS APS.

The performance and characteristic of imager chip is still under testing. Primary experimental results indicate that, by carefully implement the power and ground connection to the pixel array and output signal chain, the imager has a very uniform photon response. The measured FPN are 0.24 % and 0.31 % through CITA signal chain and source follower signal chain, respectively. Full resolution image captured by 1K×1K APS through CTIA signal chain is shown in Figure 26.

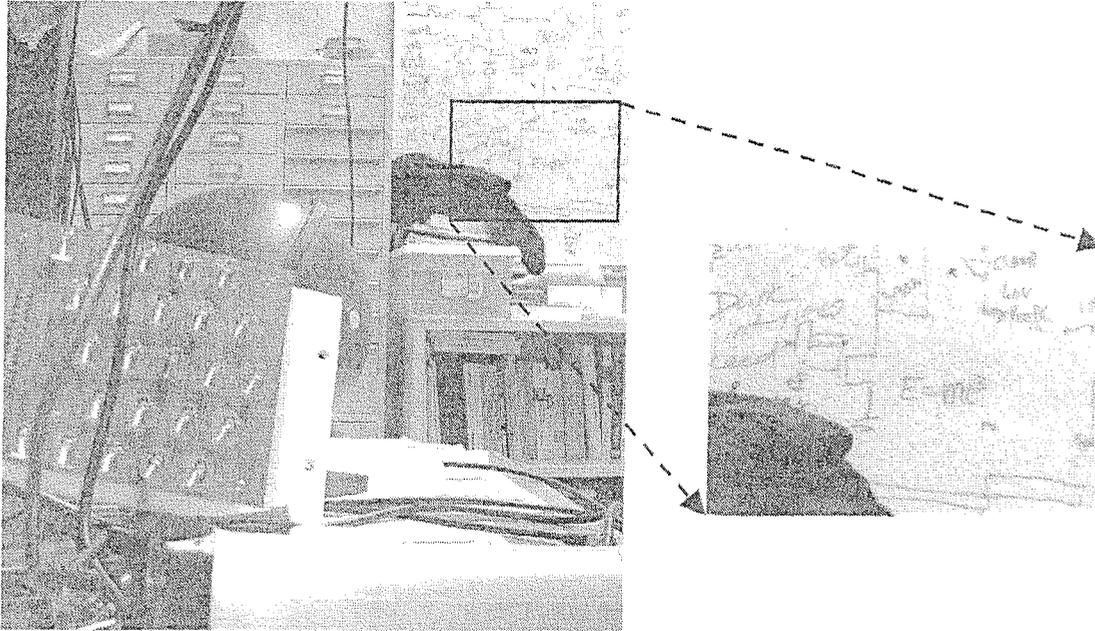


Figure 26. Full resolution image captured by 1K×1K APS through CTIA signal chain.

5. CONCLUSIONS

A highly miniaturized imaging system with low-power, simple interface, large format, and high image quality based on CMOS active pixel sensor (APS) technology has wide applications in consumer electronics, industry, military, scientific, and space applications. Recent development of CMOS APS technology has demonstrated noise, quantum efficiency, and dynamic range performance comparable to CCDs with greatly increased functionality. In this paper, we have discussed general approaches of CMOS APS technology. We have reported design and experimental results on a recent large format 5-wire CMOS APS camera-on-a-chip as well as other recent CMOS APS imager development at JPL for several applications.

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