Latent Damage From Single-Event Latchup

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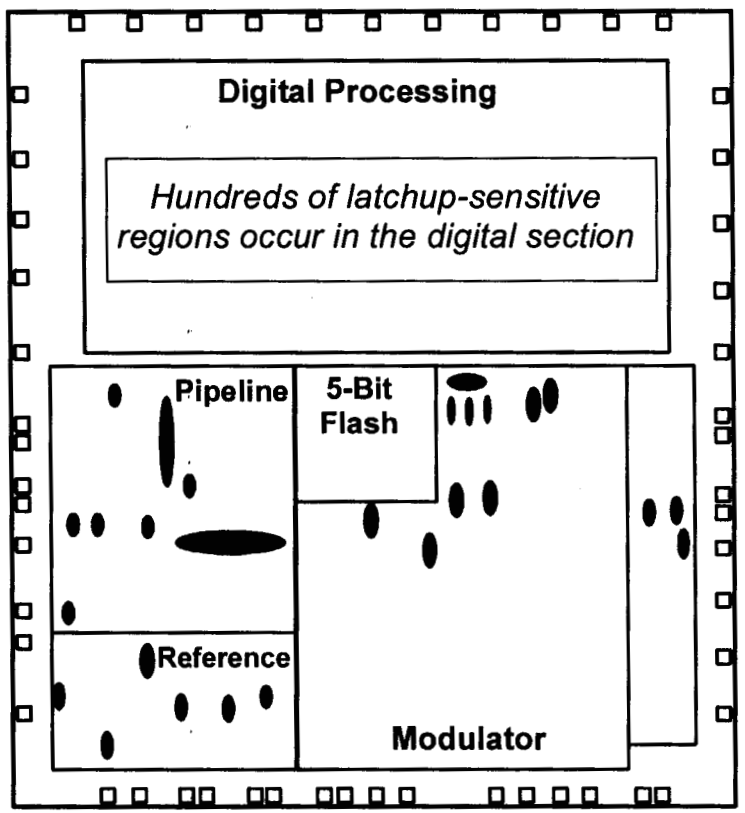
Identification of Latchup-Sensitive Regions on AD9260

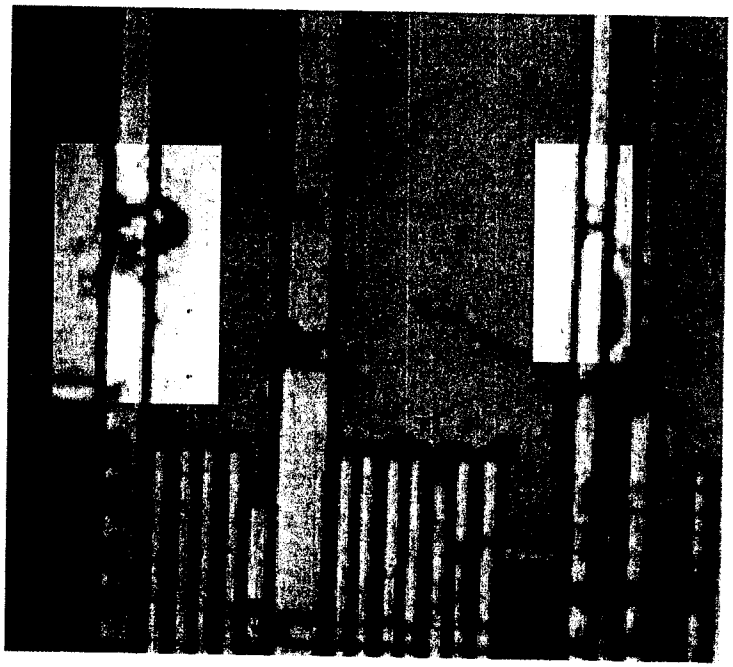
Laser-induced SEL testing at the Aerospace Corporation

- Synchronization of power supply to DUT and laser pulse
- Power clamped 1ms after arrival of pulse
- Observation of voltage through DUT during SEL on digital oscilloscope
- Laser spot position on DUT monitored with CCD camera and CRT



28 latchup-sensitive regions with distinct geometries and equilibrium currents were located in analog section of the AD9260

An Unexpected Observation



- A structurally damaging SEL was observed in real-time
- The DUT was observed to still be functional after holding a 200mA current for 1ms before the power supply was shut down

Follow-up to AD9260

- Structural damage was repeatable
  - irradiating different devices produced nearly identical SEL-induced damage
  - not due to local defects from fabrication process
  - only 50% of events were catastrophic
- Microscopy revealed erupted aluminum spheres and nearby voiding of interconnect
- Do other devices exhibit this failure mode?

CMOS Devices Studied for SEL-Induced Metallization Damage

CMOS Device	Device Type	Manufacturer	Latent Damage
AD9260	ADC	Analog Devices	Yes
AD9240	ADC	Analog Devices	No
ADC10321	ADC	NSC	Yes
CAR/CPPX1T-A7BR	Oscillator	Cardinal/Cypress Hybrid	Yes
LTC1799	Oscillator	Linear Technology	No
ADSP2100	DSP	Analog Devices	No

Five additional CMOS device types were found to be sensitive to this SEL-induced failure mode

Key Features of Latent Damage

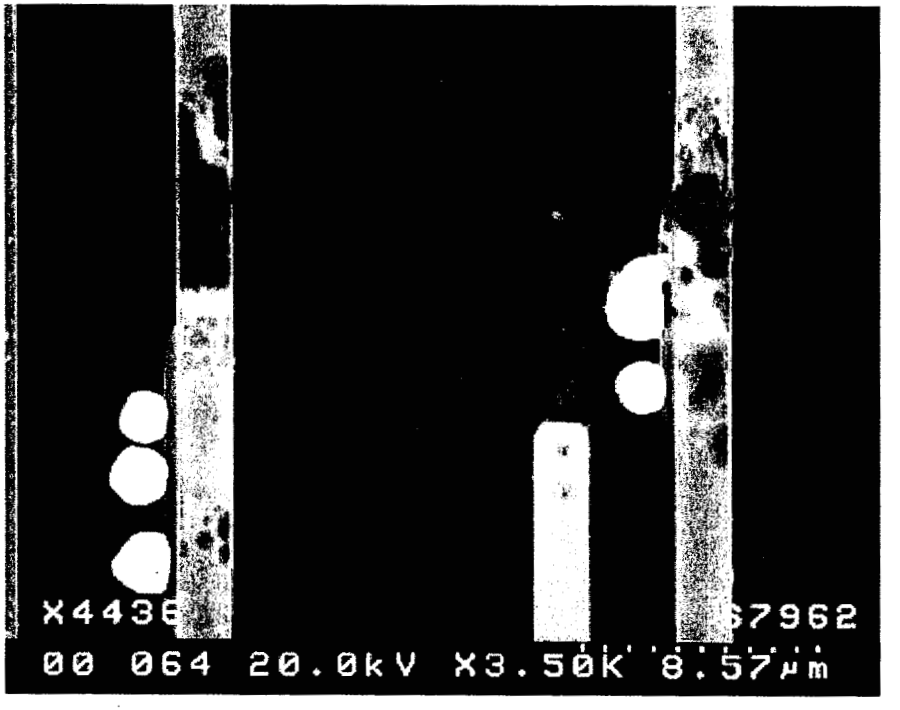
- Top level metal
- Current Density $>10^7 A/cm^2$
- More extreme/violent than electromigration ($5x10^5 A/cm^2$)

Diagnostic Approaches

- Laser Testing
  - -Allows observation of this failure mode in real time
  - -Damage site is immediately known
- Optical microscopy
  - -Die is scanned for shiny potential damage sites
  - -Often difficult due to the complexity of many CMOS circuits
- Scanning Electron Microscopy (SEM)
  - -Bright regions revealed to be spheres of erupted metal
  - -Energy Dispersive Spectroscopy (EDS) confirms that spheres are Al and not packaging remnants left from delidding process

Latent Damage Signatures

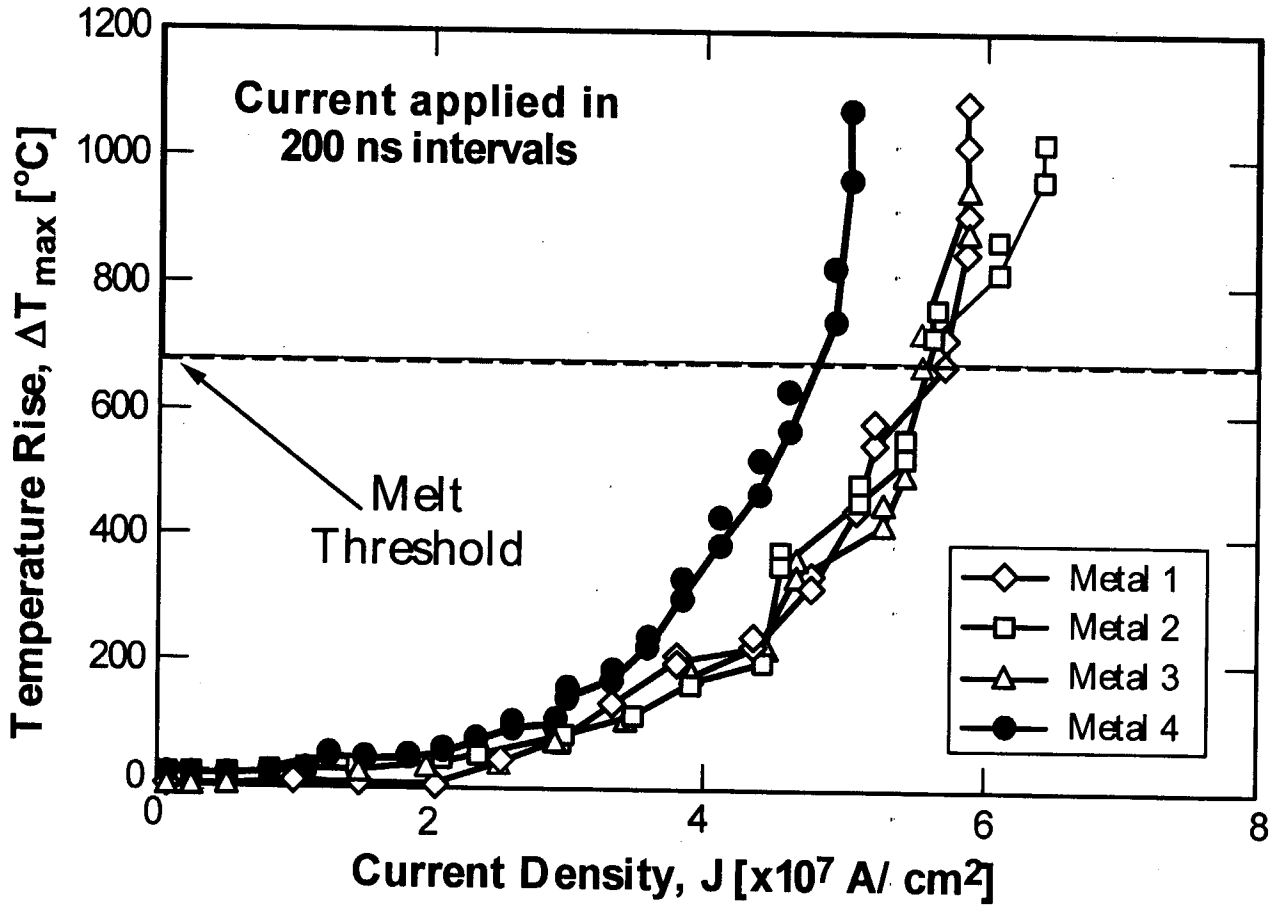
- Erupted aluminum spheres
- Cracking of insulator material (silicon nitride/oxide)
- Fracturing and lifting of insulator to release metal
- Significant voiding of interconnect metal
- Most often occurs in top level metal



Previous Studies of Interconnect Failures from Current Pulses

- **"Critical" current density of 10^7A/cm^2 for pulses over 1μs** for fracture-type failures (Murguia & Bernstein)
- Modeling shows **top level metal experiences highest temperature increase** at high current densities; effect intensifies as more levels of metal are used (Shen; Gui)
- **Stress caused by mismatch between thermal expansion coefficients** of metal & insulator material (Kim & Sache)

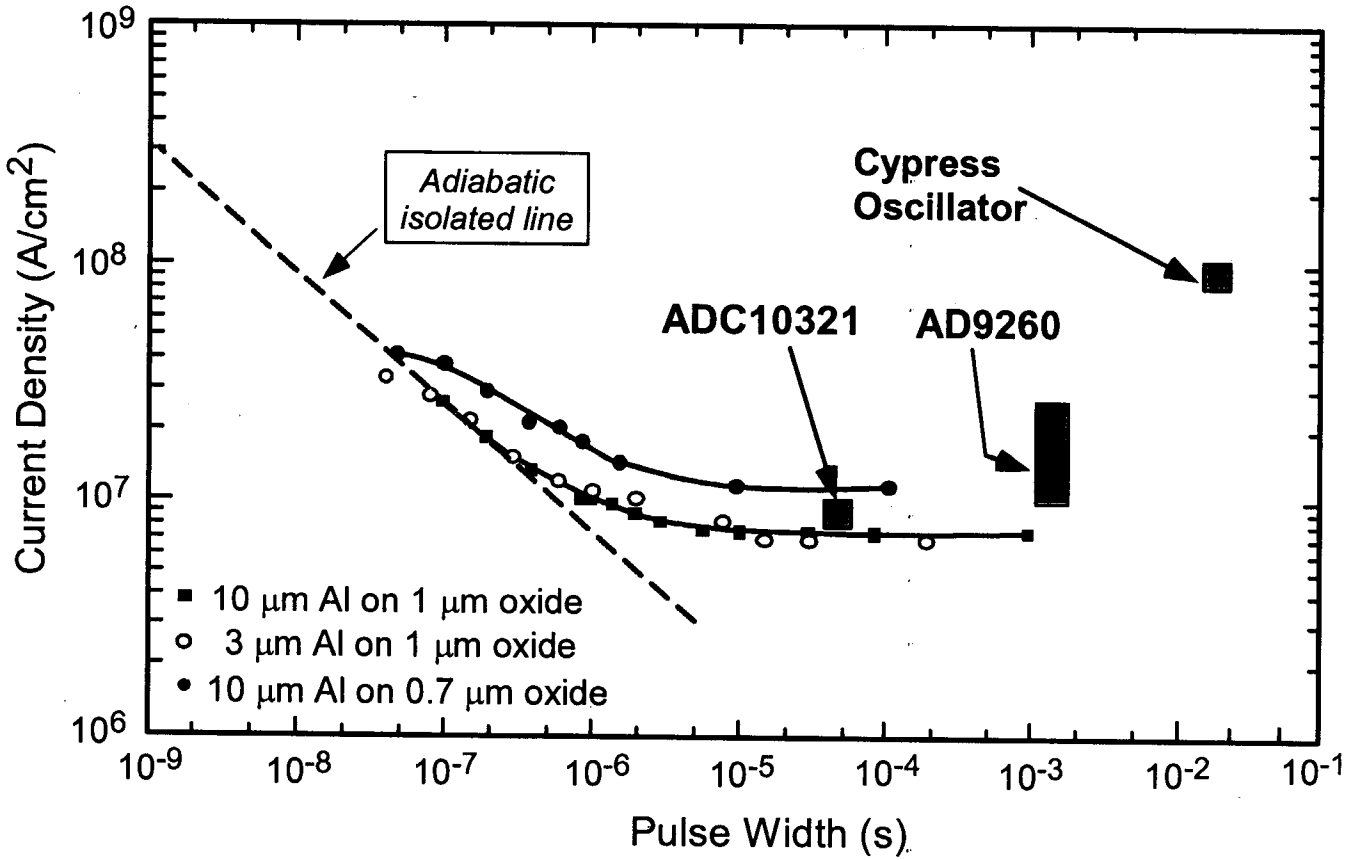
Previous Studies of Interconnect Failures from Current Pulses



After Banerjee, et al., Elect. Dev. Lett., 18(9), 1997

Open circuit failure/melting of Al previously predicted at current densities of 5-6 x 10^7 A/cm^2 and pulses as short as 200ns (Banerjee, et al)

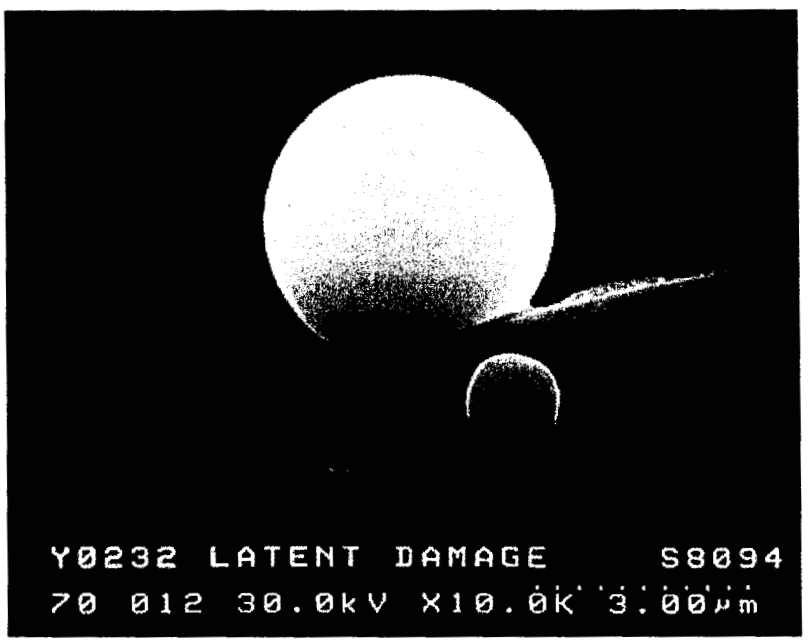
SEL-Induced Latent Damage Data



After Murguia and Bernstein, Elect. Dev. Lett., **14**(10), 1993

With our current densities of 10^7-10^8 A/cm^2 & durations of 60μs or more => MELTING

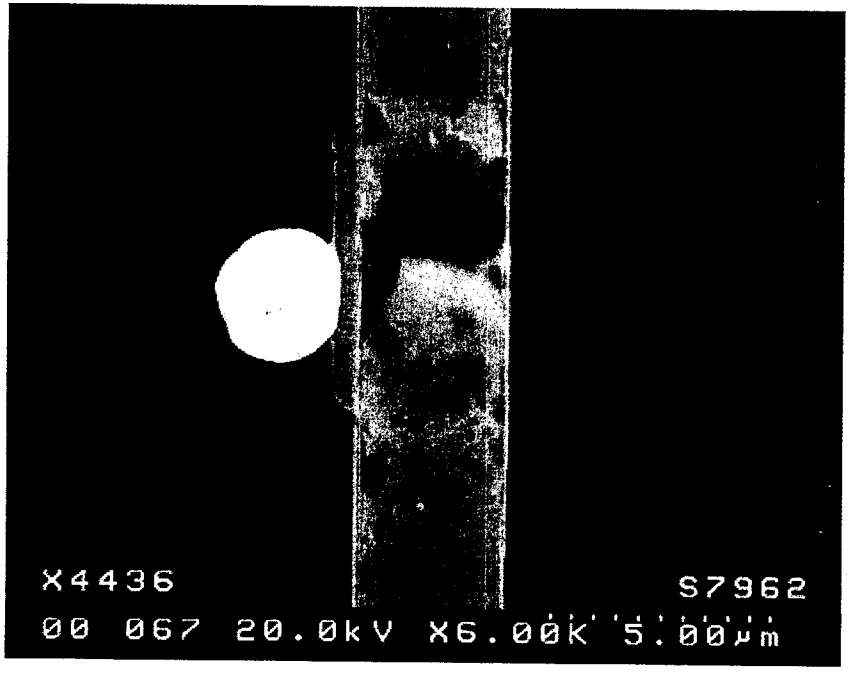
A Physical Interpretation



- Critical current density is held long enough to melt interconnect
- Differences in thermal coefficients of expansion of metal and insulator puts mechanical stress on insulator
- Cracking of insulator and eruption of metal occur, often to the point of catastrophic voiding
- As extruded metal cools it forms most efficient spherical shape
- ***Not*** Electromigration

Why Some Events are Non-Catastrophic ("Latent")

- Amount of ejected metal may be too small to cause catastrophic failure
- After melting and re-crystallization, some metal may form bridge across the void, keeping circuit closed
- Interconnect cross-section may be smaller, more susceptible to later electromigration failures



Complexities Involved in Predicting Device Sensitivity to Latent Damage

- Insulator thicknesses influence thermal diffusion – *the Si substrate is the actual heat sink*
- Although the current drawn by the DUT is known, the current through an individual interconnect is not known
- Wide variety of metal dimensions, number of levels of metal, and insulator thicknesses are used among devices
- *Unless you look for it (laser testing or post-irradiation diagnostics) you don't know it's there*

Impact on Future SEL Testing

- If a latchup sensitive part is going to be flown with latchup circumvention circuitry, is the circuit mitigating *latent* damage?
- Vulnerability to electromigration-related failures may increase after latent damage is experienced.
- Latent damage may become a larger problem as the semiconductor industry moves toward using more levels of metal and smaller interconnects.

Conclusions

- Critical current density to be aware of: $10^7 A/cm^2$
- Latent damage may occur as fast as 200ns
- Latent damage is difficult to observe during most testing for SEL
- Latchup mitigation efforts should take this failure mode into account
- Newer, smaller and denser devices may exhibit more of this problem

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Laser Induced SEE Testing

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Scanning Electron Microscopy