

# A Reliability Evaluation Methodology for Memory Chips for Space Applications when Sample Size is Small

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## Abstract

This paper presents a reliability evaluation methodology to obtain the statistical reliability information of memory chips for space applications when the test sample size needs to be kept small because of the high cost of the radiation hardness memories. This methodology can be also used to generate overdriving guidelines and characterize production lines in commercial applications and to obtain de-rating guidelines in space applications.

## Introduction

The memory chips used in space applications normally have been radiation hardened (RH) against the total dose effects and single-event effects (SEE), resulting from the space radiation environment which poses a certain radiation risk to all electronic components on the earth-orbiting satellites and planetary mission spacecrafts[1]. This radiation-hardness can be achieved by either special processing, such as the use of doped SiO<sub>2</sub>, double-layer oxide structure and thin epitaxial layers, or/and design techniques, such as special SRAM cells with cross-coupled resistors or capacitors to reduce the SEP susceptibility [1]. Because of this special process and design efforts, the RH memory chips are very expensive compared to commercial ones, typically about two orders of magnitude higher. Therefore, a large sample size for reliability testing is not always feasible, especially for end-users in a cost constrained environment.

On the other hand, the electronic systems used in spacecraft usually have much higher reliability requirement because of the nature of the mission. One single bit error/failure on a memory chip is often considered the failure of the memory chip, but the information or distribution of the first bit failure is not the type of information usually available from the RH electronic part manufacturers, or from the commercial electronic part distributors, the two sources of electronic parts in space community. In order to achieve the long-term reliability goal of the space missions, memories are powered at a voltage lower than nominal V<sub>dd</sub> which sacrifices the speed or performance of the memory in exchange for a longer life time. This derating practice requires the voltage acceleration factor, which again is not available for memory chip end-users in space community. Therefore, the challenge is how to obtain the above necessary reliability information on a limited sample size.

In this paper, we present a reliability evaluation methodology to extract the reliability information from accelerated memory testing and simulations by using a small memory testing sample size. The information extracted includes the time-to-first-bit failure distribution for memory reliability projection, voltage acceleration factor and/or activation energy plus memory performance and reliability relationship for overdriving and de-rating guidelines. SRAMs are selected to demonstrate the reliability

evaluation methodology, but the general conclusion may apply to other type of memories, such as EEPROMs.

## Experimental Details and Results

The SRAM chips used in this study are from a standard commercial 0.25um technology production line. The memory chips were tested at 5.05V and 4.95V at 125°C and 5.05V at 100°C. Random testing pattern was used and only functional bit errors were recorded as bit failures. The testing program is designed to keep stressing the SRAM chips and record the time each bit failed until either the number of bit failures accumulated to 100 or the whole memory failed the functional test. The leakage criterion was intentionally set high, so we could collect enough bit functional failures for data analysis. But when the leakage current reached a certain level, the memories tend to fail very rapidly. For the purpose of this study, we are only interested in the early bit failure distribution and behavior.

The early bit failure distributions at 5.05V and 4.95V at 125°C, 5.05V at 125C and 100C are plotted in Figure 1 and Figure 2 respectively. The information on these two plots gives the estimate of the voltage acceleration factor and activation energy, which will be explained in the next section.

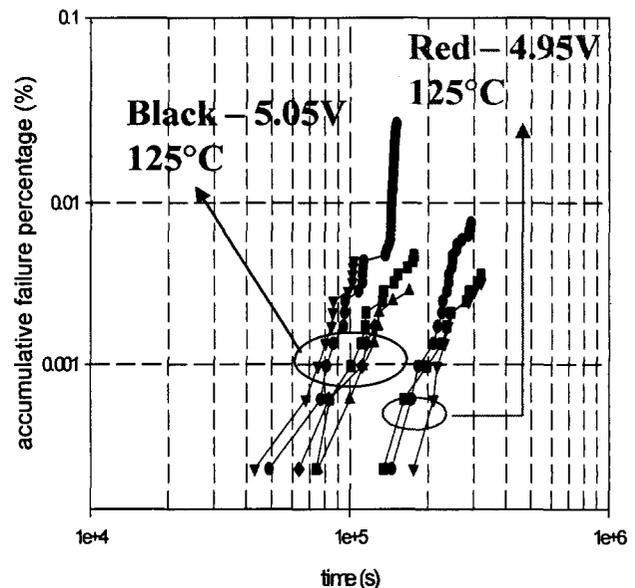


Figure 1. SRAM functional error distribution biased at 5.05V (black) and 4.95V (red) under 125°C.

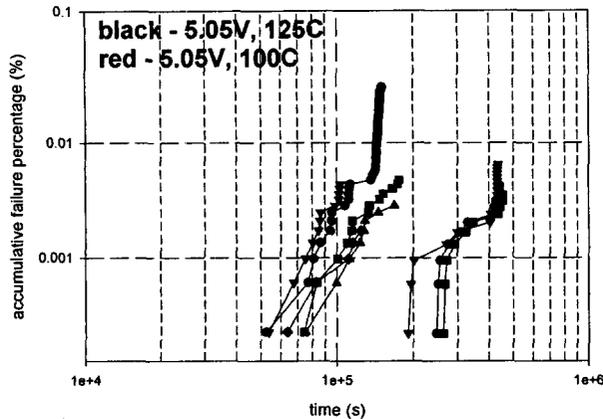


Figure 2. SRAM functional error distribution biased at 5.05V at 125°C (black) 100°C (red).

Both Figure 1 and 2 show a tendency towards bimodal distribution, indicating that the failure mechanisms may not be the same for the first and second groups of bit failures. Note that the early bit failure distributions from different samples seem to be straight lines in a log-normal probability plot. Based on this observation, we may assume that the early bit failure distributions follow log-normal distribution and this is fundamental to develop and apply the proposed methodology detailed in next section. We believe that this behavior is expected for a qualified production line because of the process and chip design consistency.

### Reliability Simulation for First Bit Failure Distributions

Based on the observation on Figure 1 and 2, we can assume that the early bit failure distribution  $D_i$  on each chip follows lognormal distribution with a median  $\mu_i$  and a standard deviation  $\sigma_i$ . It means that each early bit failure distribution has its own median and standard deviation values which are different from other early failure distributions. To decide the parameters  $\mu_i$  and  $\sigma_i$ , the median and standard deviation of each early bit failure distribution  $D_i(s)$  (letter  $s$  stands for testing sample) were first calculated on each testing sample under the same stress condition and then the median and standard deviation of the median distribution  $D(\mu)$  and standard deviation distribution  $D(\sigma)$  of each early bit failure distribution were estimated for the stress condition assuming a normal distributions for both  $D(\mu)$  and  $D(\sigma)$ . Therefore, the parameters  $\mu_i$  and  $\sigma_i$  will be from median distribution  $D(\mu)$  and standard deviation distribution  $D(\sigma)$ , respectively. Assuming a number of  $n$  bit failures per chip and a number of  $m$  chips under testing, the early bit failure distribution on each chip ( $1 \sim m$ ) can be simulated by randomly choosing a  $\mu_i$  from  $D(\mu)$  and a  $\sigma_i$  from  $D(\sigma)$ .

Note that the first bit failure is defined as the first bit failure of a memory. This definition means that the first bit failure determination is a function of memory size, *not* the smallest random number simulated from the bit failure distribution. This is very important because the number of bit failures assumed, as well as the number of chips assumed, should only increase the accuracy of the simulation and should *not* have any impact on the final results. But if the smallest random number is picked as the first bit failure, the larger the size of the bit failures per chip, the smaller first bit failure time is expected.

Figure 3 shows the simulated first bit failure distribution with assumed 100 bit errors per chip, 100 chip per run and 16 runs for the stress condition of 5.05V. The actual first bit failure data are fallen in the simulated data range, indicating that the simulation assumptions, algorithm and approach are valid.

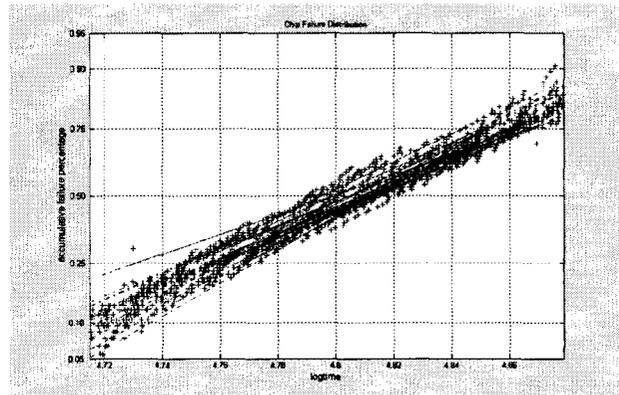


Figure 3. Simulated first bit failure distribution with 100 bit errors per chip, 100 chips per run and 16 simulation runs.

Figure 4 shows the first bit failure distribution simulation result for both stress conditions. The voltage acceleration factor can be obtained for guidelines on overdriving and de-rating. Voltage acceleration model is assumed as  $t \propto e^{-\beta V}$  [2,3], where  $t$  is the time-to-failure,  $V$  is the applied voltage and  $\beta$  is the voltage acceleration factor which is calculated as 7.8953 in Figure 1 and 7.9968 in Figure 4, compared to  $7.0 \pm 1.4$  in [3]. This indicates that our data and simulation agree well with existing SRAM testing results for the first bit failure distributions published. The activation energy for the first bit failure is estimated at around 0.52eV using the same approach and the SRAMs tested have shown similar activation energy and voltage acceleration factors.



Figure 4. Simulated chip first functional error distribution with 100 bit errors per chip, 10 chip per run and 16 runs for both 5.05V and 4.95V bias conditions. The voltage acceleration factor is estimated as 7.99/V.

### Discussions

This information is essential to project reliability under overdriving bias condition in commercial applications and help to characterize the production line since the SRAM cells are representative for the CMOS process. It is a little complicated in de-rating practice, when the performance reliability relationship will also need to be decided.

Figure 5 shows the ratio of applied voltage over Vdd versus the ratio of the SRAM first bit failure time at the applied voltage over the first bit failure time at Vdd. For example, if 1.1Vdd is applied overdriving the 2.5V and 3.3V SRAMs, we will expect a 7X and 14X decrease of device life time over the device life time at Vdd. Or, if 0.9Vdd is applied to de-rate the 2.5V and 3.3V SRAMs, a 7X and 14X increase of device life time over the device life time at Vdd will be expected.

The time to failure plotted on Figure 5 is the time to 0.1% failure fraction on the first bit failure distribution, but it holds for time to any failure percentage since the information presented is the ratio instead of absolute life time.

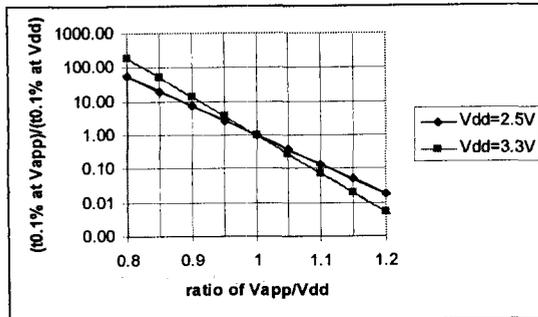


Figure 5. The ratio of the first bit failure time as a function of apply voltage over Vdd for the SRAMs tested.

To achieve the same device life time ratio over Vdd, 2.5V devices needs further overdriving or de-rating than 3.3V devices. This means that if the voltage acceleration does not change much within the technologies, lower Vdd applications need higher overdriving and de-rating factors to achieve the same device life

time increase ratio than higher Vdd applications. This calls for careful de-rating (not overdriving) practice because the difference between the input high and Vdd is getting smaller for newer technologies and therefore leaves a smaller room for de-rating.

## Summary

The reliability analysis and testing results on 0.25um commercial SRAMs are reported to demonstrate a reliability evaluation methodology to extract the necessary reliability information from a small sample size and help to generate overdriving and de-rating guidelines for memory chips. Lower Vdd applications for the CMOS technology may need to have higher overdriving and de-rating factors to achieve the same device life time increase ratio and may have less bias de-rating room, assuming the same voltage/bias acceleration.

## References

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