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Phase Measurement System

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Outline

- Phase meter development
- LISA photoreceiver
- Optical materials

FPGA Phasemeter, Konstantin Gromov

Requirements

- 1. Noise floor of 5 microcycles/$\sqrt{Hz}$ from $\sqrt{(15/4)}$ mHz to 1Hz
- 2. Heterodyne frequency range from 10 kHz to 15 MHz
- 3. One output at 10 Hz with a triggering accuracy of 30 nsec.
- 4. Second output at ~100 kHz
- 5. Scalable to multiple channels, at least 2, possibly as many as 6-9 (with relaxation of requirements (3) and (4) for some of the channels

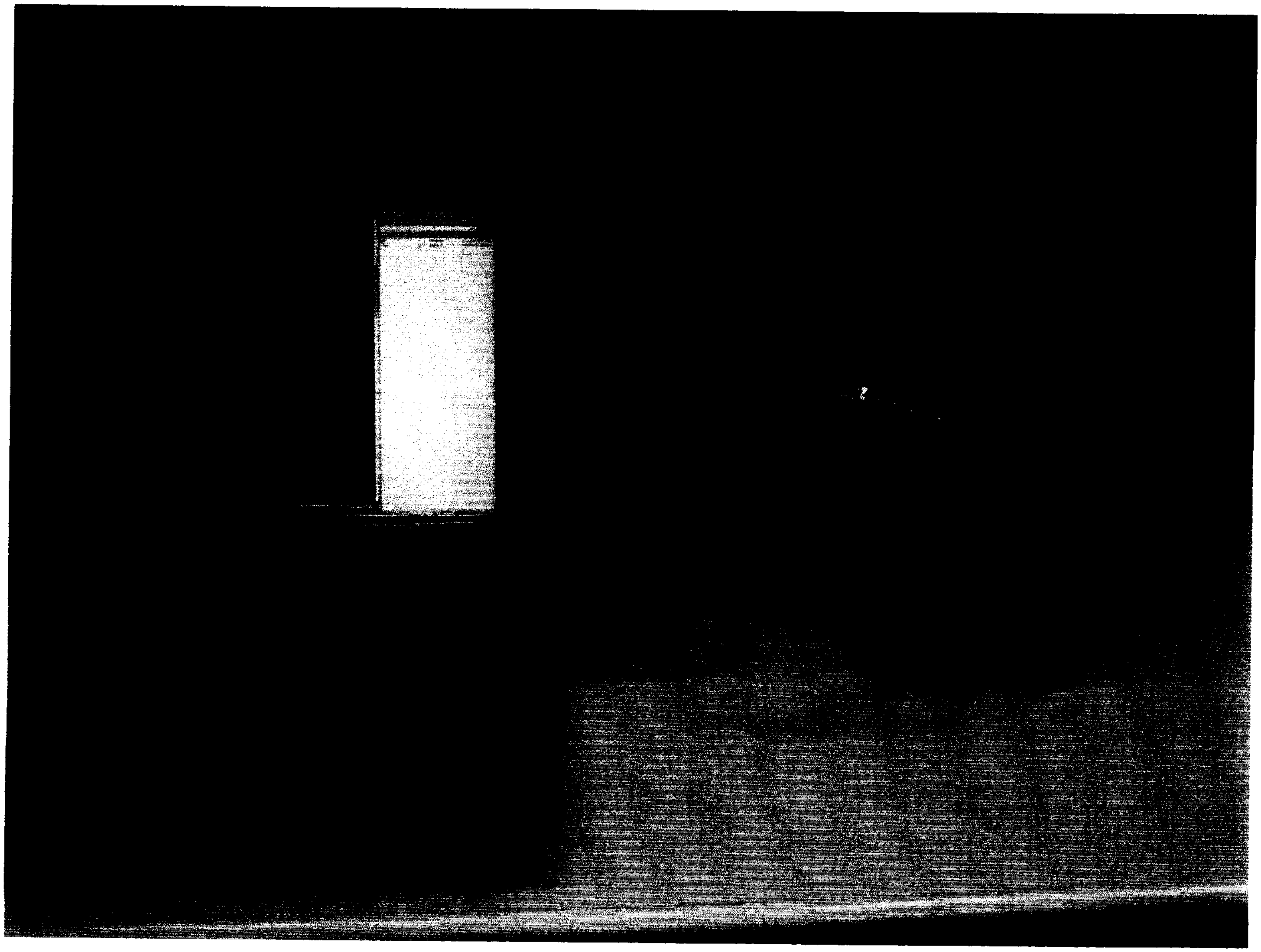
Approach to Phase Meter Design

- Implement most of Phasemeter in reconfigurable - portable H/W platform (WildCard)
- High level control and interface from the host system
- No real time required for the host system (Windows Box)

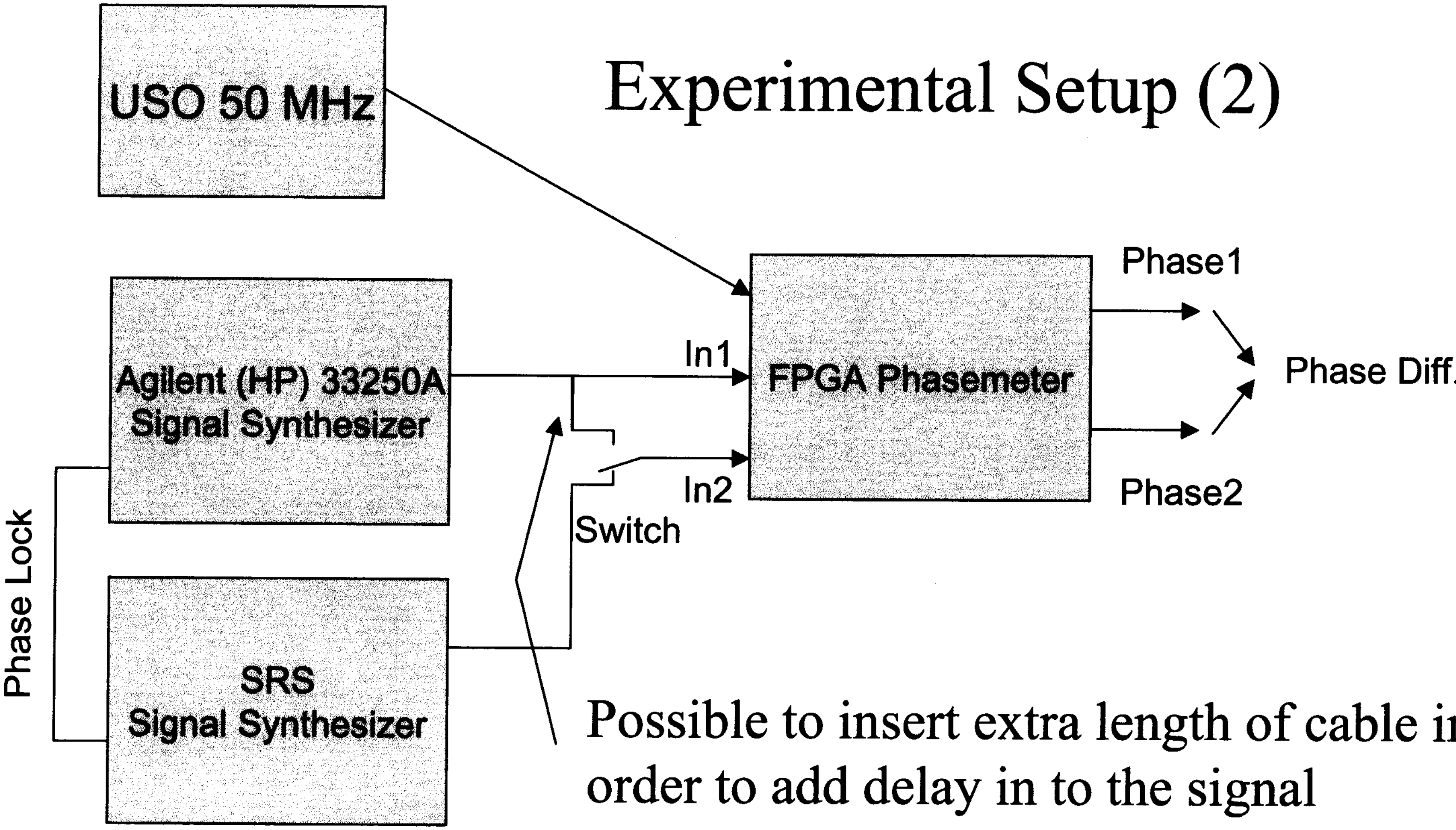
Principle of operation

- FPGA Phase meter is a digital system (it is equivalent to single bit quantizer)
- All phase information is contained in the zero crossings
- Phase meter averages phase over sampling period and reports average phase
- Start of the sampling period could be specified to 1 clock (USO) cycle

Experimental Setup



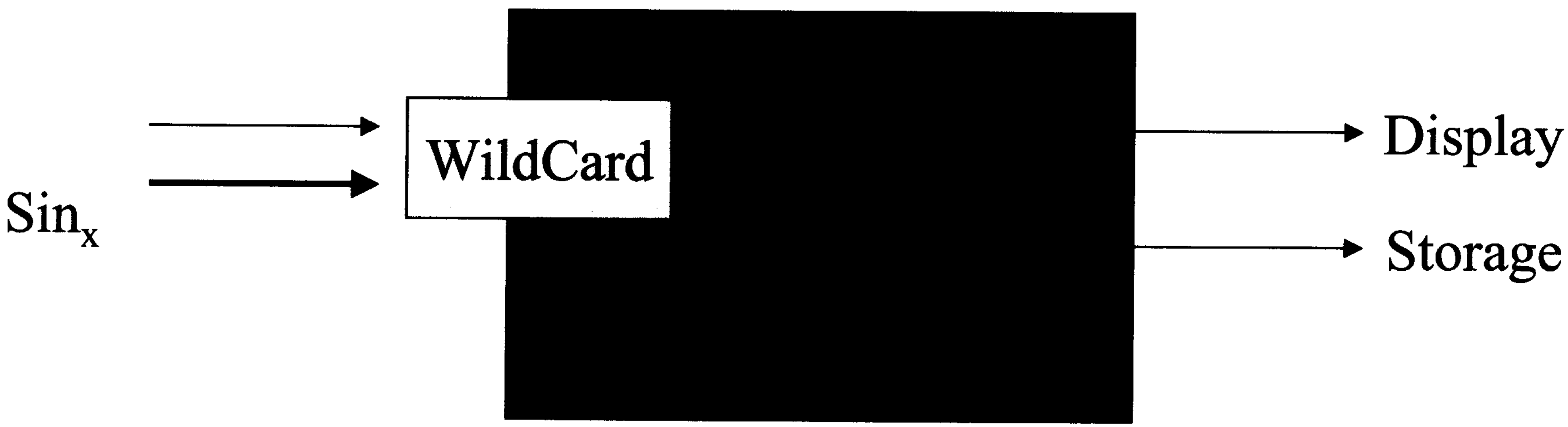
Experimental Setup (2)



Possible to insert extra length of cable in order to add delay in to the signal

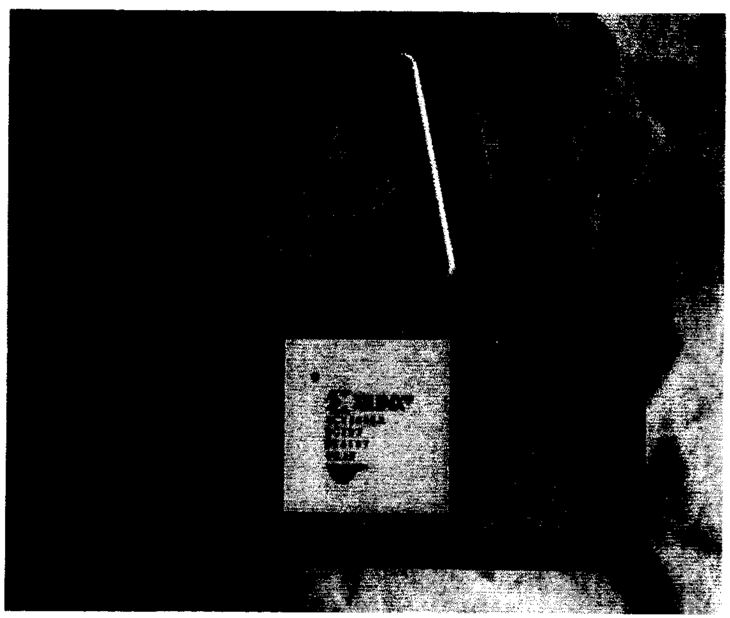
Conceptual drawing: signal splitting is done by 2-way splitter, Switching is done by reconnecting cables.

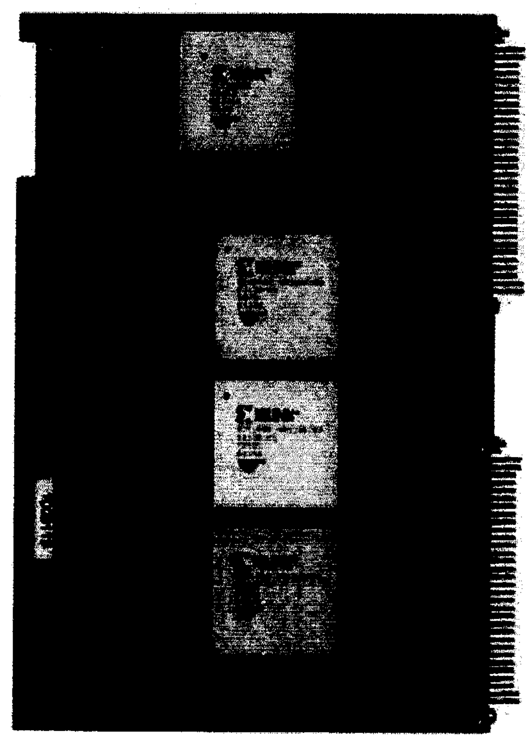
HW and Design Description (1)



HW and Design Description (2)

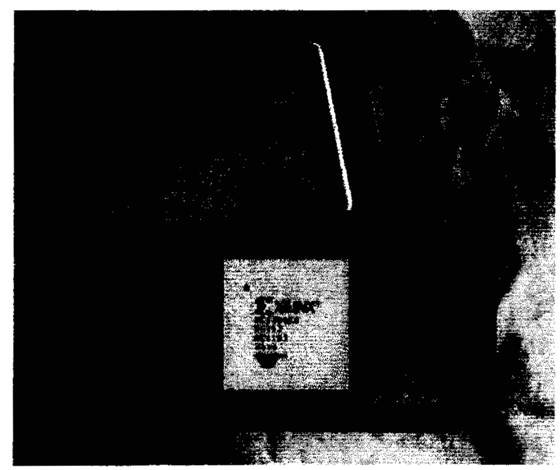
- Annapolis Micro Systems, Inc.
- Range of products
- Xilinx FPGA Based



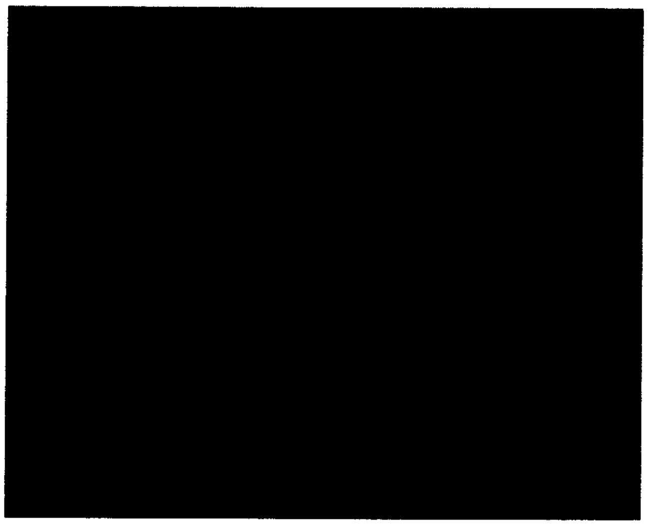


WILDCARD

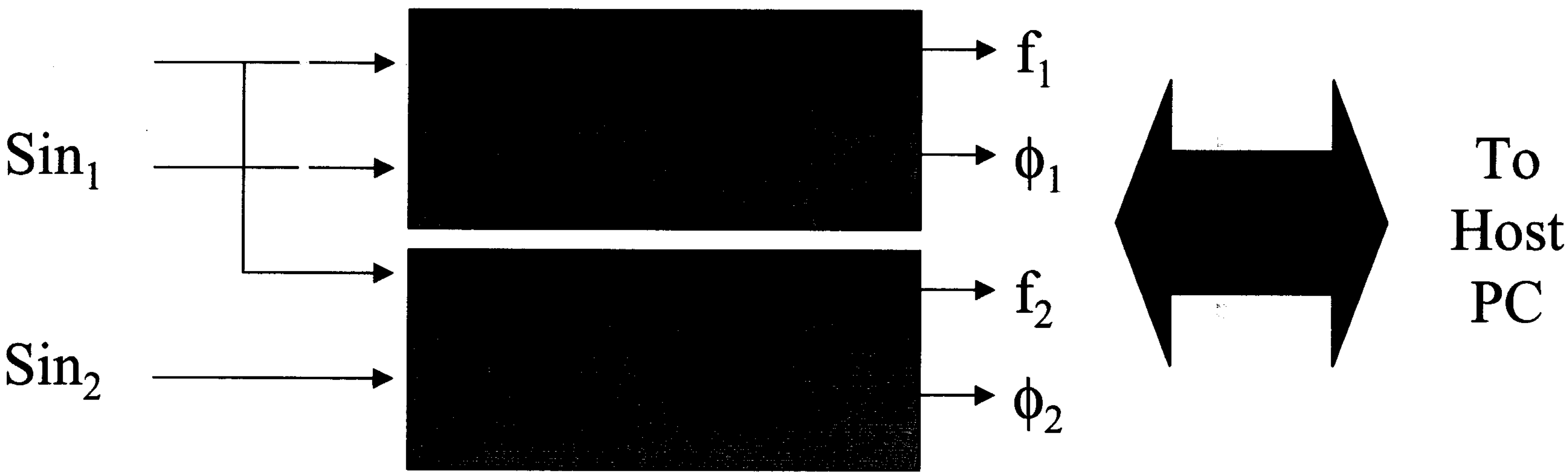
- Use in portable and wearable computers
- Type II PC Card - single height format
- 32 bit PCI interface
  - Multichannel DMA Controller
  - Programmable Clock Generator
- Single Processor Element - Virtex 300 (Xilinx XCV300E FPGA)
- 2 independent memory ports
- 2 15 pin I/O connectors
- Windows 2000/98 and Linux
- Multi-thread safe software support
- PE Current Monitoring



WILDCARD (2)

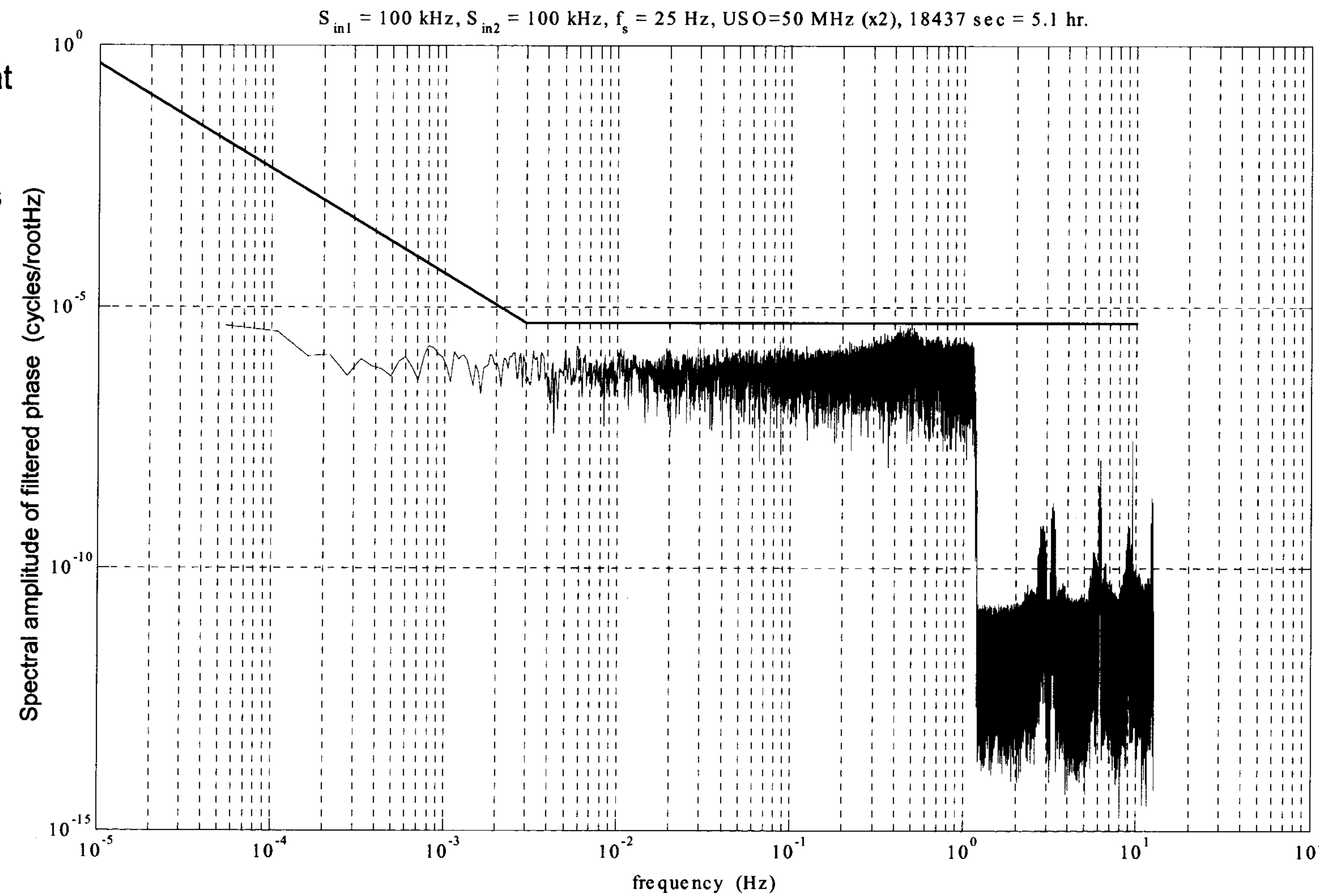


HW and Design Description (3)

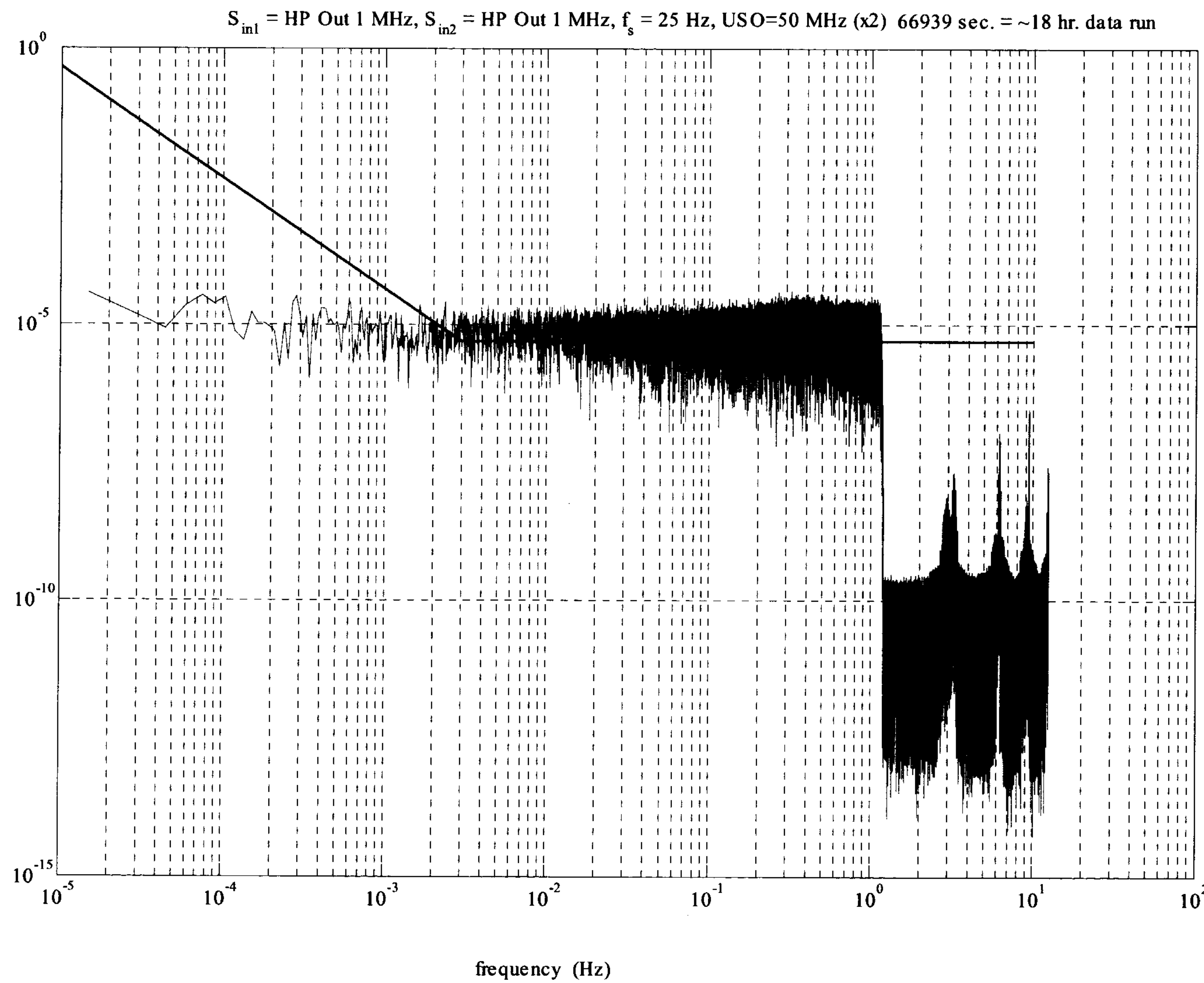


Experimental Results

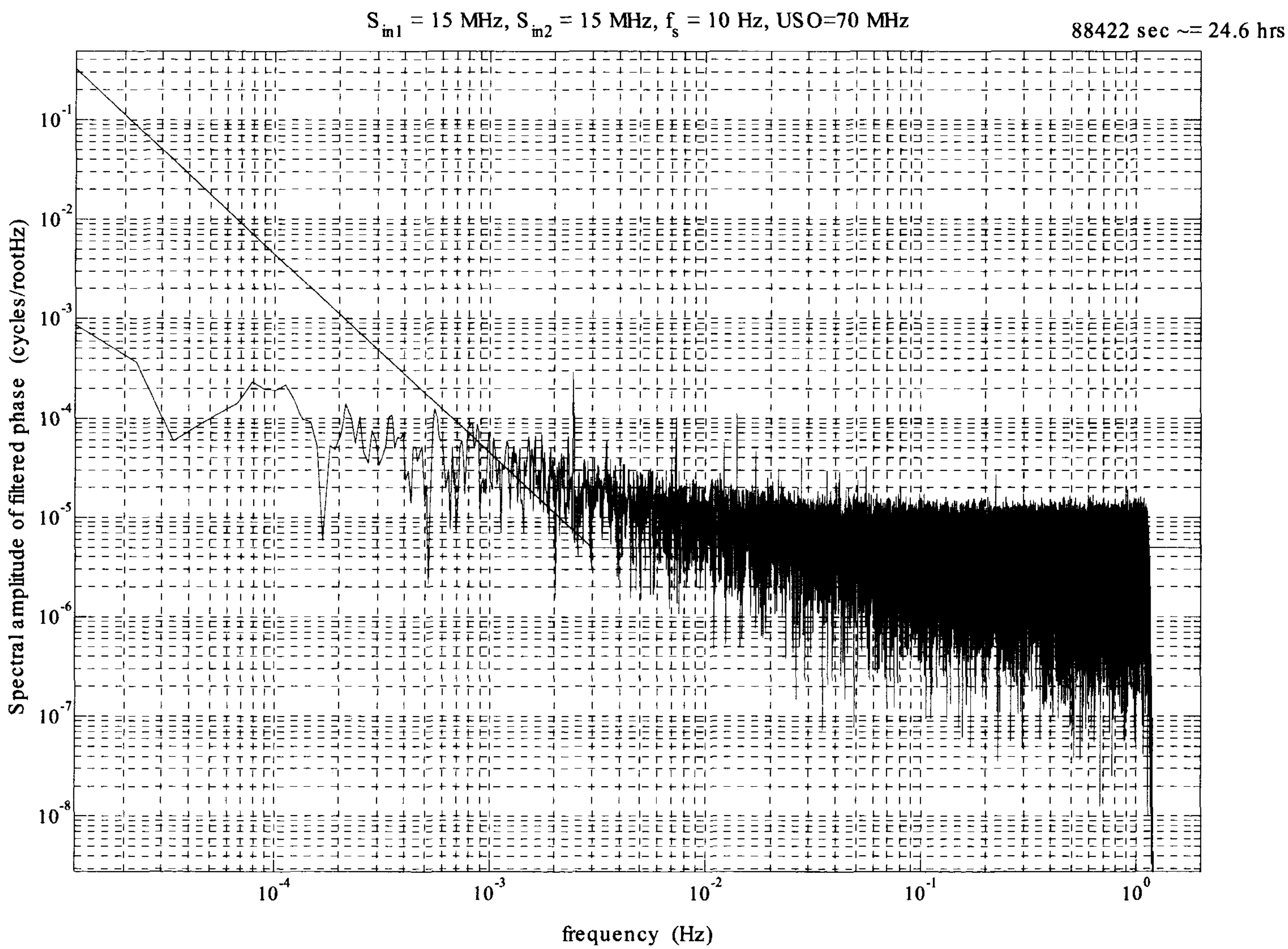
- New FPGA Code That uses Pos and Neg edges of USO
- 5.1 Hour Test Results
- Input Signal 100 kHz (Same signal split into two inputs)
- Phases sampled at 25Hz
- USO is 50 MHz



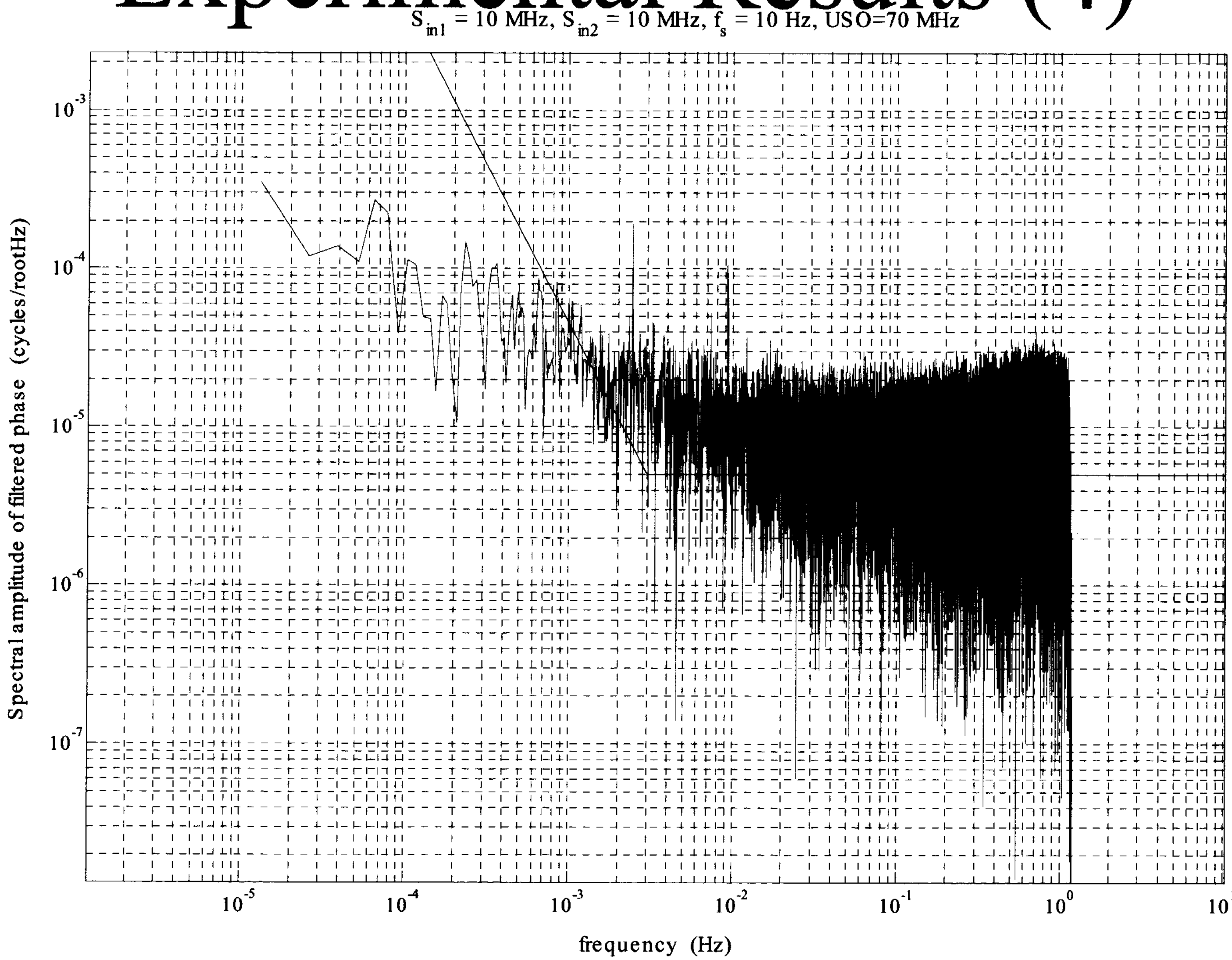
Experimental Results (2)



Experimental Results (3)



Experimental Results (4)



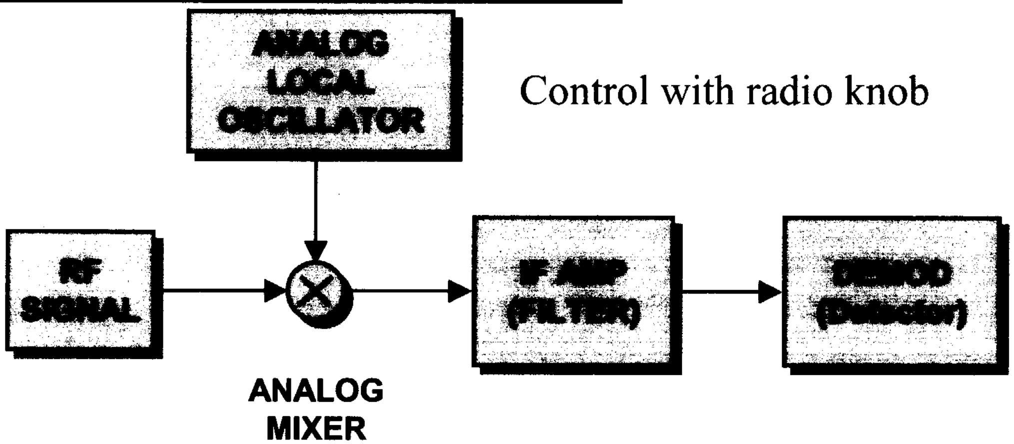
Future Work

- Increase Clock (USO) Frequency
- Switch to faster FPGA
- Achieve LISA Performance
- Extensively test and verify design
- Transfer to standalone system
- Transfer to space-qualified FPGA

Digital Receiver Principle (Martin Marcin)

Purpose : Extract narrow band signal from wide band source

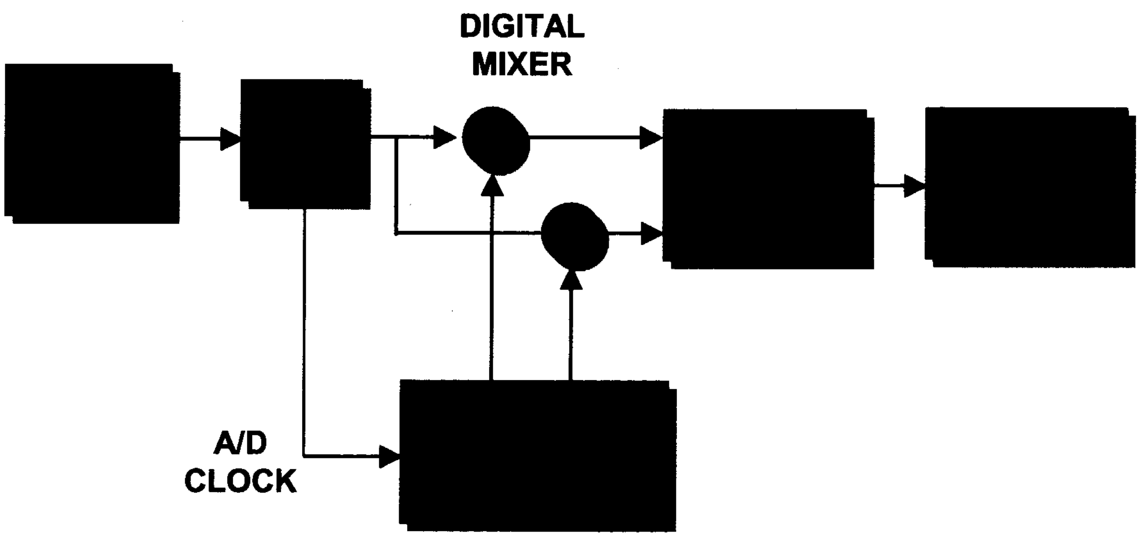
- **Conventional Heterodyne Receiver**



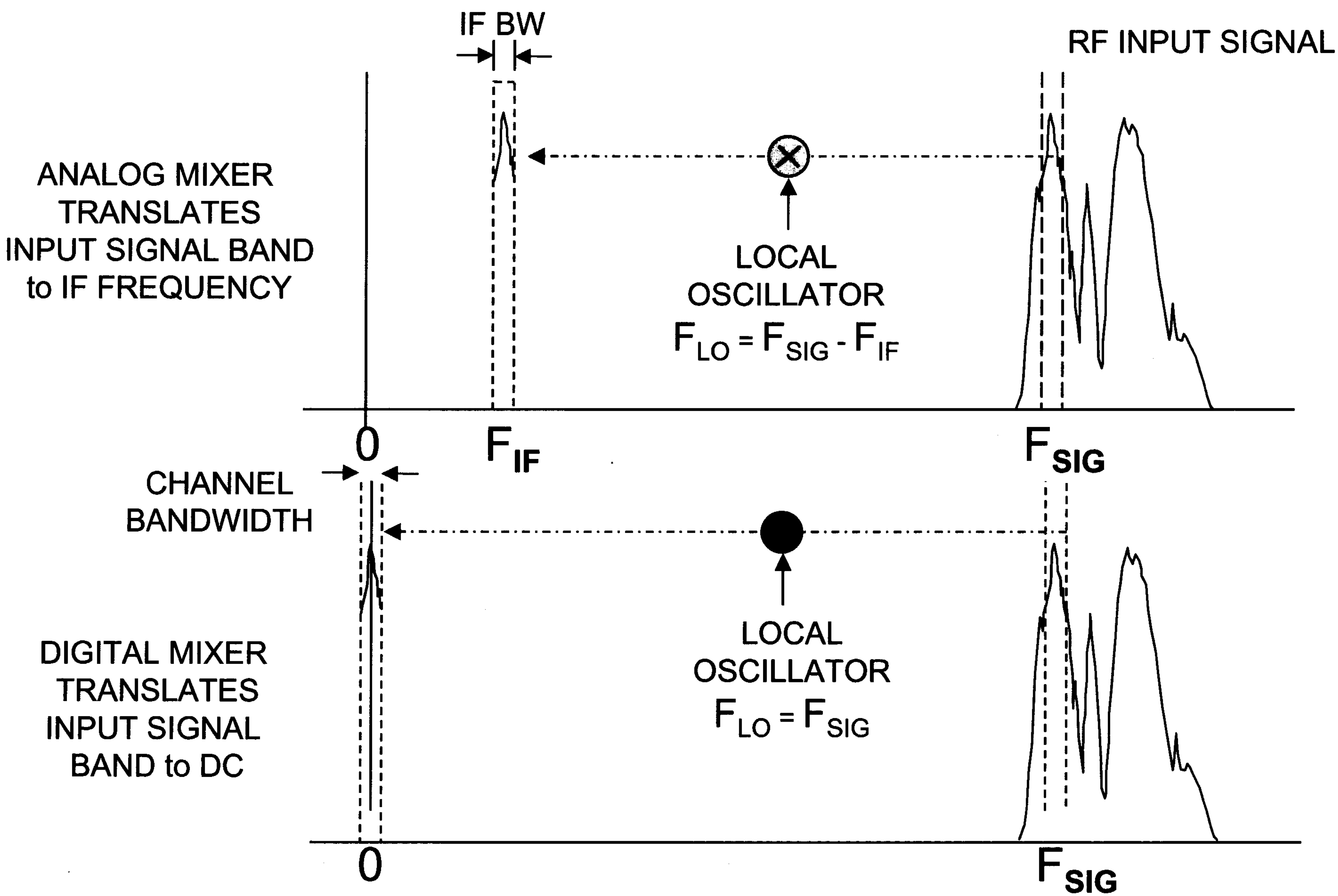
Control with radio knob

Recover original signal.
AM: envelope detector
FM: frequency discriminator

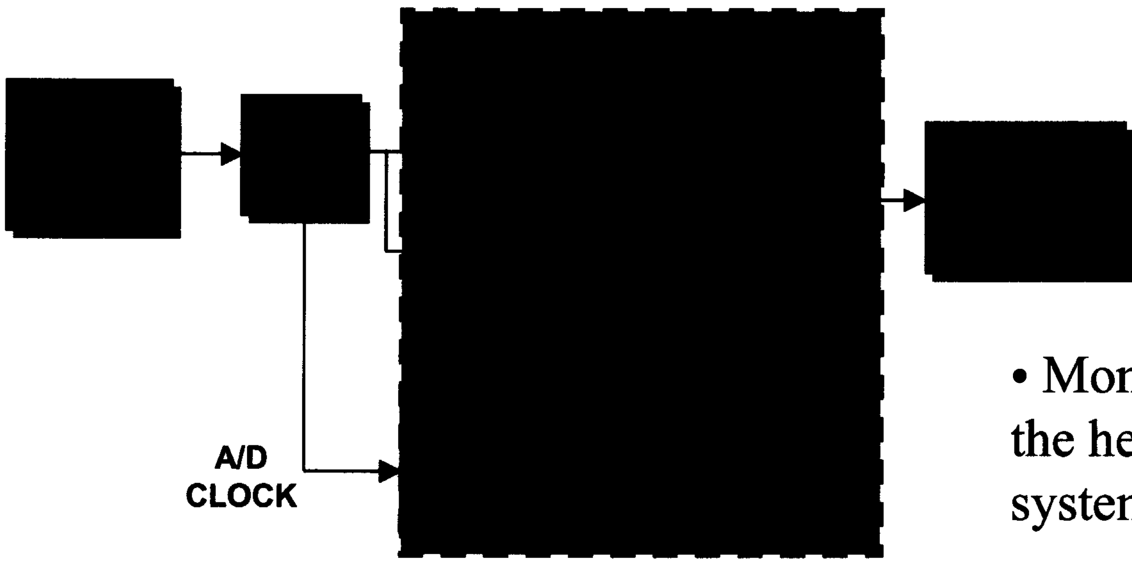
- **Digital Receiver**



Digital Receiver Principle - 2



Digital Receiver Principle - 3



- A/D converter requires band limiting of input signal to avoid aliasing
- Monolithic digital receiver chip is the heart of the digital receiver system

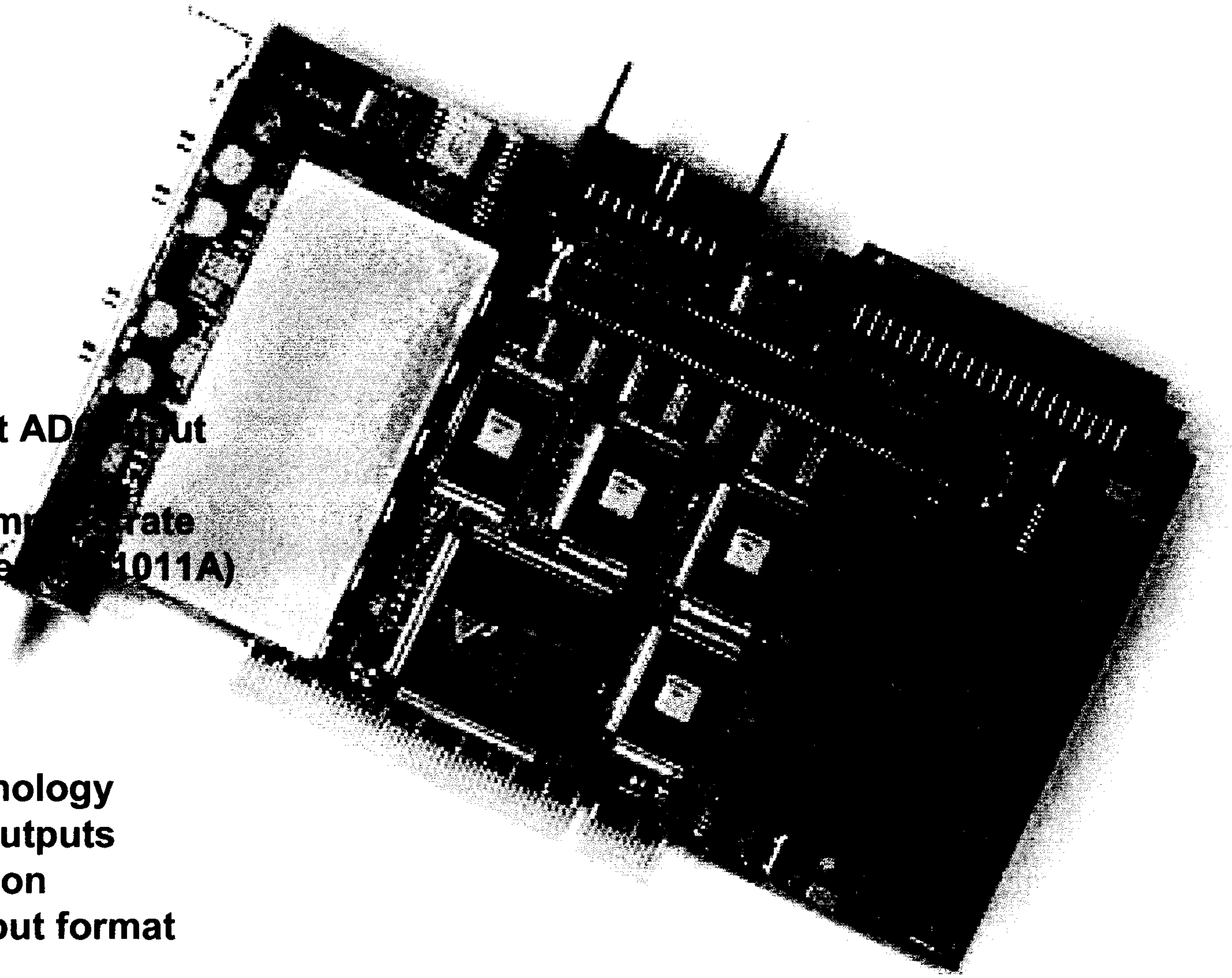
- Translation and filtering are major functions of receiver chip.
- DLO produces digital samples of sine and cosine at the A/D sample clock rate.
- Dual digital multiplier performs complex mixing for frequency translation.
- Low Pass Filter output bandwidth is programmed by setting a decimation factor, D.

Output BW = ADC Sample Rate / D

Details

COTS Prototype

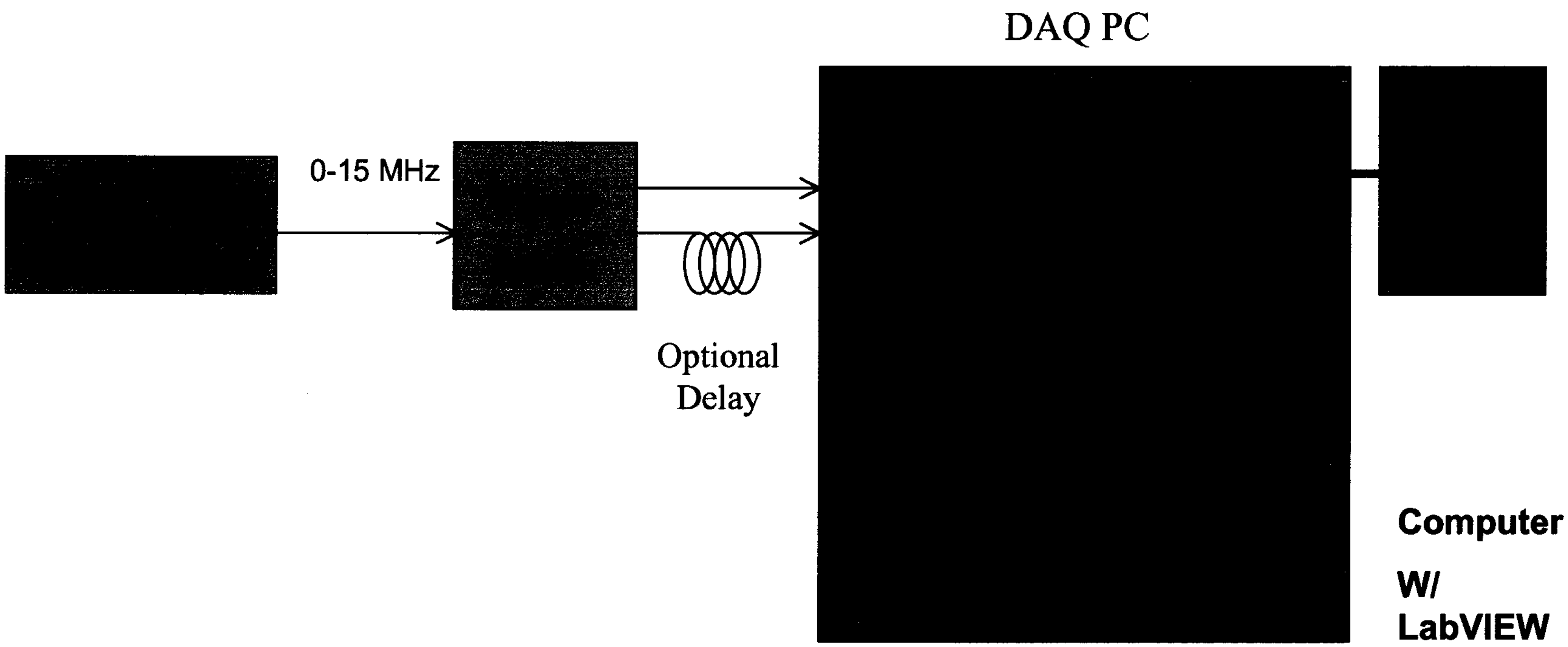
Interactive Circuits and Systems ICS-652-DC50-N



ICS652 :
- 2 independent , 14-bit ADC input channels
- 65 MHz maximum sample rate
- dual narrowband tuner (GC1011A) daughter card
- PCI format

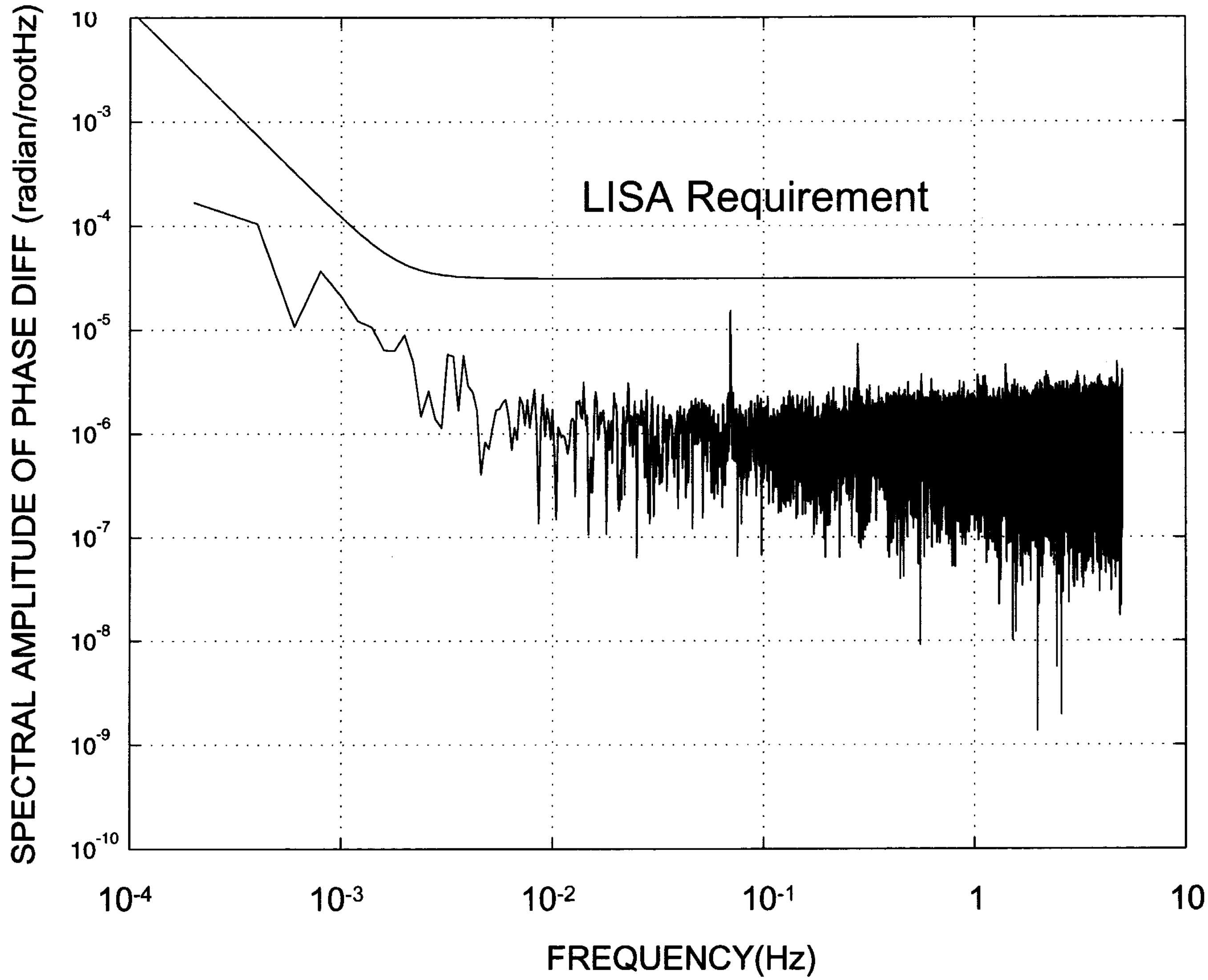
GC1011A :
- 1 micron CMOS technology
- 12-bit inputs, 16-bit outputs
- 0.1 Hz tuning resolution
- Real or Complex output format

Experimental Setup

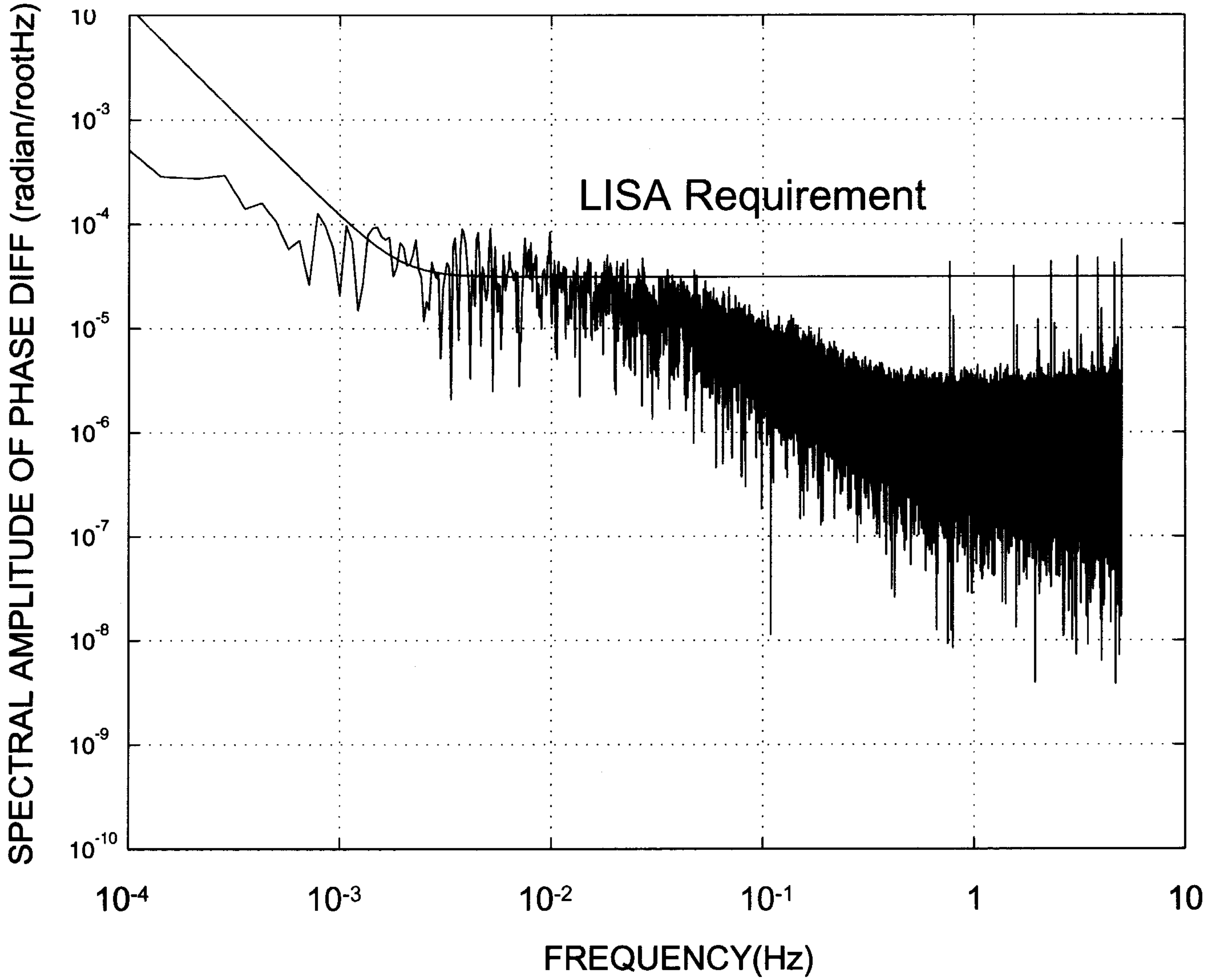


Measure: Phase(channel 1) - Phase(channel 2)

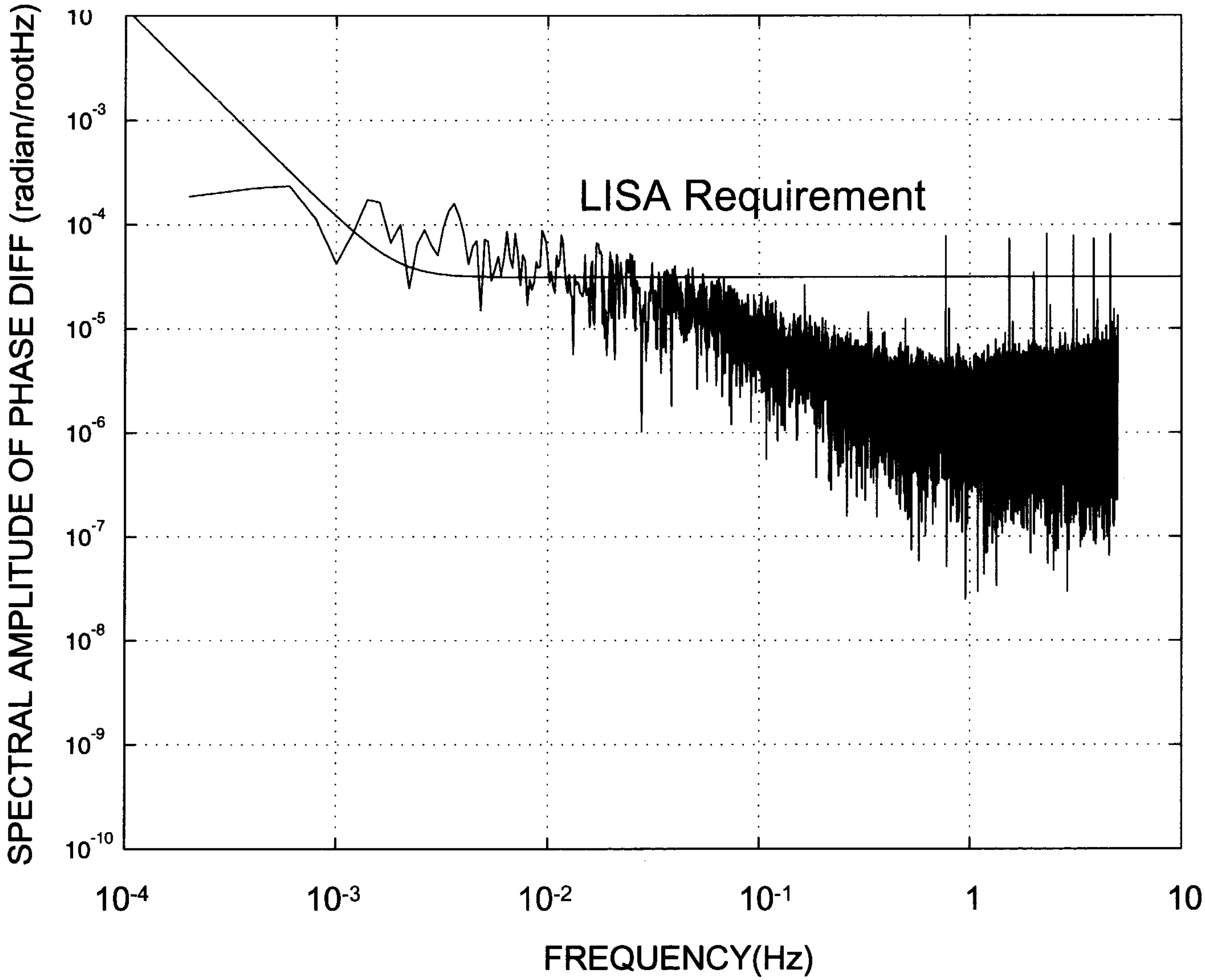
030808135256, **10kHz** identical signals, output rate=7.8125kHz,
80% filter, D=8192, integration rate=**10Hz**



030812134455, **8 MHz** identical signals, output rate=7.8125kHz, 80% filter, D=8192, integration rate=**10Hz**



030809125048, **15 MHz** identical signals, output rate=7.8125kHz, 80% filter, D=8192, integration rate=**10Hz**

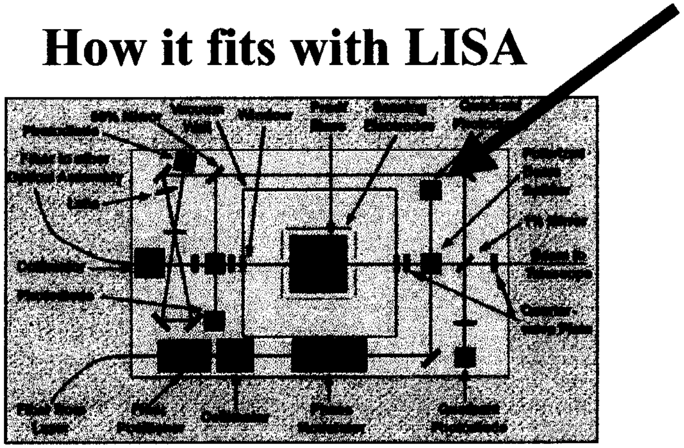


Future Work

- Investigate externally triggered acquisition
- Investigate externally clocked mode (OCXO delivery 9/03)
- Optimize DAQ routine since LabVIEW overhead is significant

Main LISA Photo receiver (Carl Christian Liebe)

How it fits with LISA



Baseline Requirements

- Photon noise limited
- Received beam ~15 pW/channel
- Local Beam: 0.25 mW/channel
- 4 Channels
- 200 MHz bandwidth
- Lowest possible power consumption (<1 W)

Main LISA Photo receiver – Design Issues

Amplifier Chip

Selected OPA657, best available combination of wideband and low noise

Current Noise: 2 pA/sqrt(Hz)
Voltage Noise: 4.8 nV/sqrt(Hz)
Gain Bandwidth Product: 1.6 GHz

Photo receiver Configuration

Transimpedance amplifier
Post amplifier stage
4 Channels (quad photo diode) for pointing sensor
Measured bandwidth: 50 MHz

Photo Detector Selection

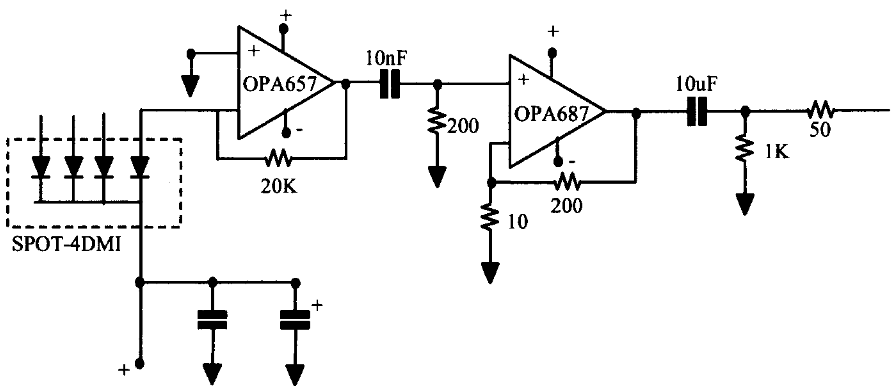
	IR enhanced Si	Si	InGaS	Comment
Capacitance (pF/mm^2)	4	4	125	>10 for InGAs
Quantum Efficiency	0.25 A/W	0.4 A/W	0.8 A/W	

InGas has too large a capacitance. Only Si enables bandwidth for LISA applications

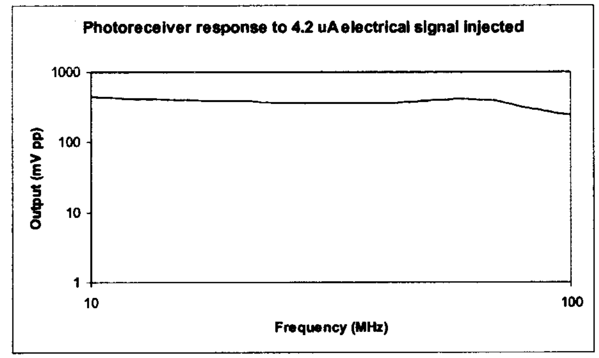
UDT, DMI-4SPOT selected, 0.25 mm^2, 1pF
Will later utilize IR-enhanced Si Detector

Main LISA Photo receiver – 1 Channel Prototype

Electrical Diagram

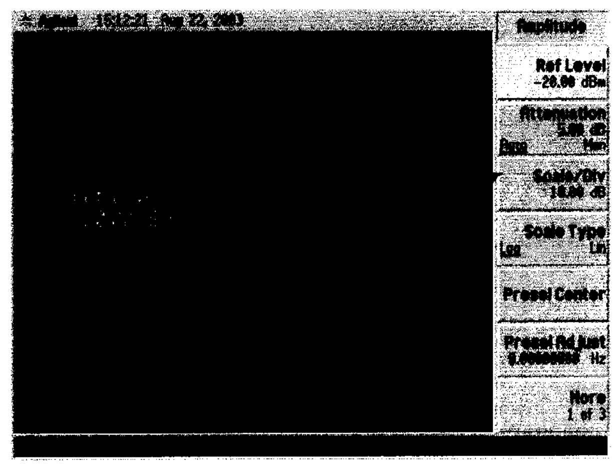


Response



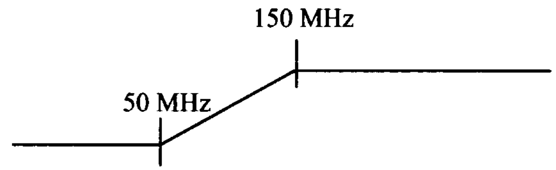
Photo

Output Noise (with and without illumination)



Main LISA Photo receiver – Future Work

Extended Bandwidth



Adding extra amplifier with zero at 50 MHz
Explore other methods

4 Channels photo receiver

Main LISA Photo receiver - Conclusions

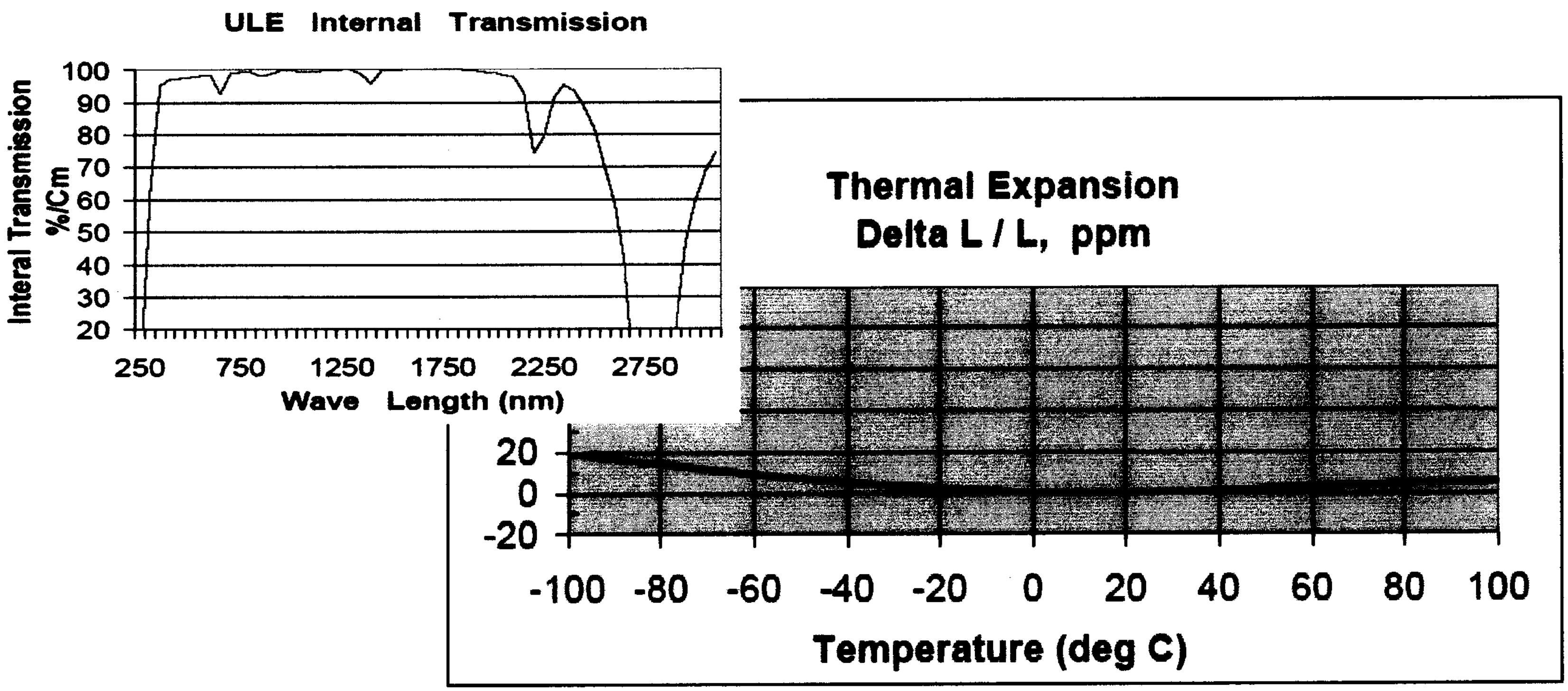
Prototype in Hand. Tests show:

Shot noise is 3 times larger than elec. noise up to x MHz
Response flat within 1-2 db up to 50 MHz
Extending bandwidth is under investigation

LISA's need for low CTE optics?

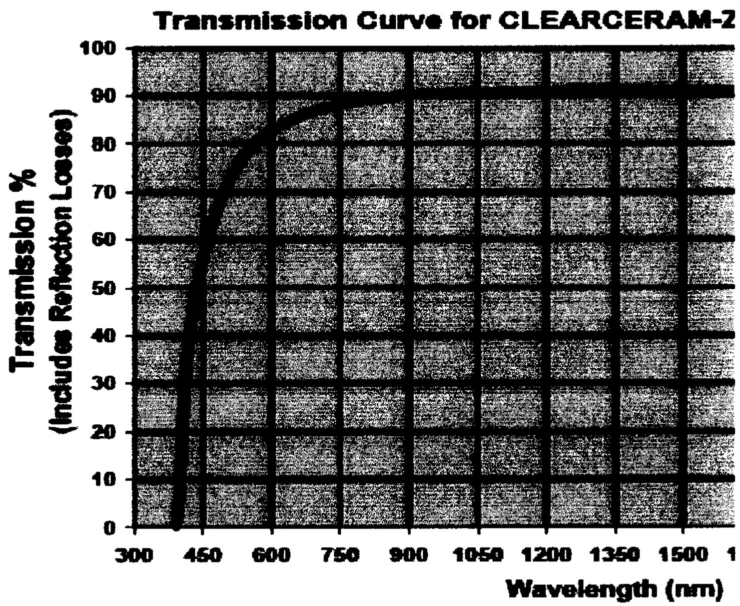
- Several large optics within LISA need to be stable over 1000's of seconds
- ULE is a present the baseline material of choice, however, it has issues:
  - Good material for spacer, but not good in transmission;
  - Therefore, ULE can only be used as part of the payload and other materials are needed for the transmissive optics;
    - This results in a mismatch of CTE for the payload, and hence, stresses in the optics are inevitable;
  - Furthermore, the CTE curve for ULE is unpredictable

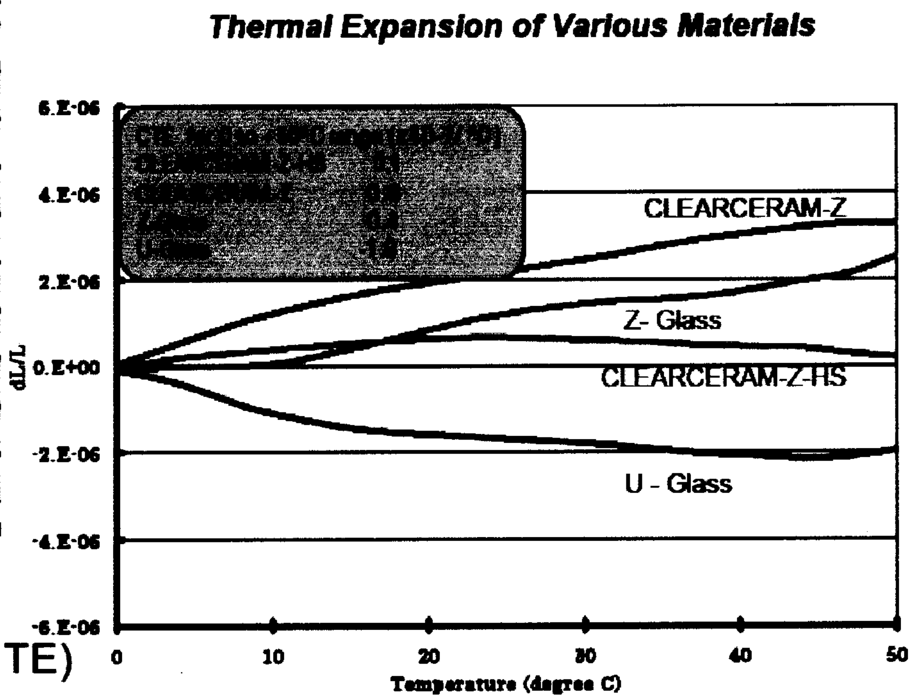
Published Data on ULE



- CTE is 0±30 ppb/^{0}C over 5 to 35 ^{0}C
  - However the turning point is not well defined, or reproducible

Published Data on ClearCeram



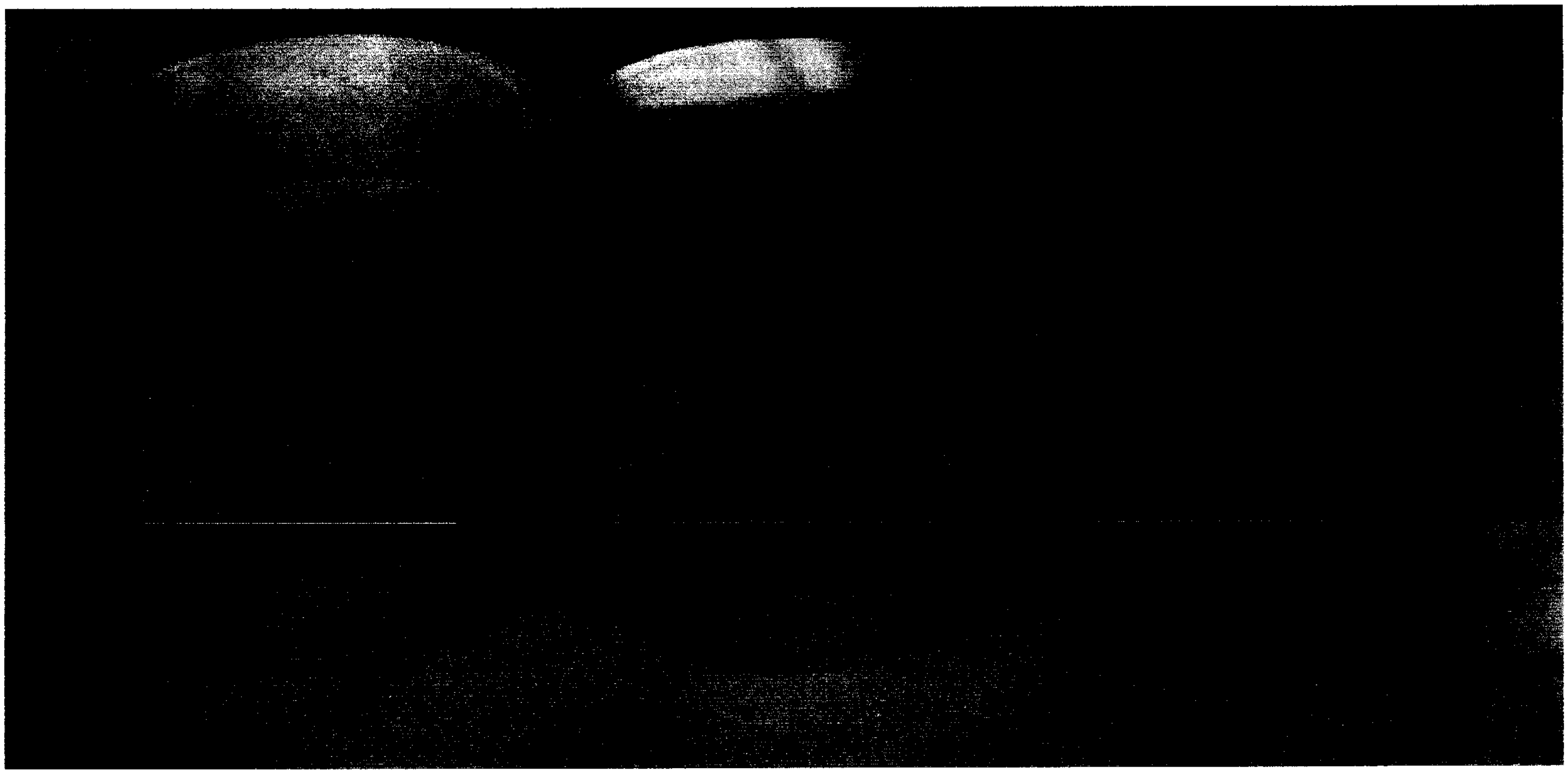


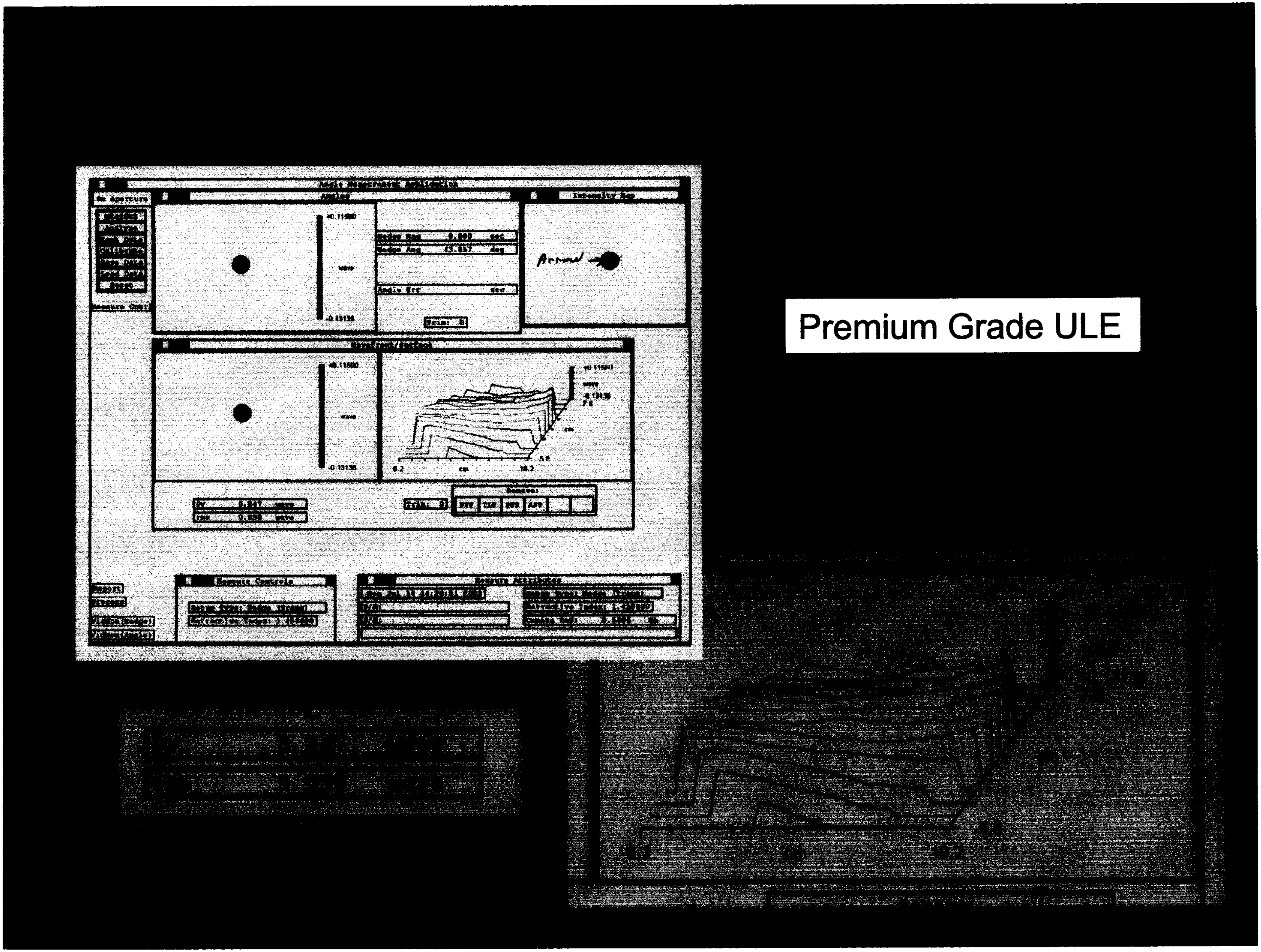
Data above based upon Ohara's measurements of individual samples. Other samples may provide different results.

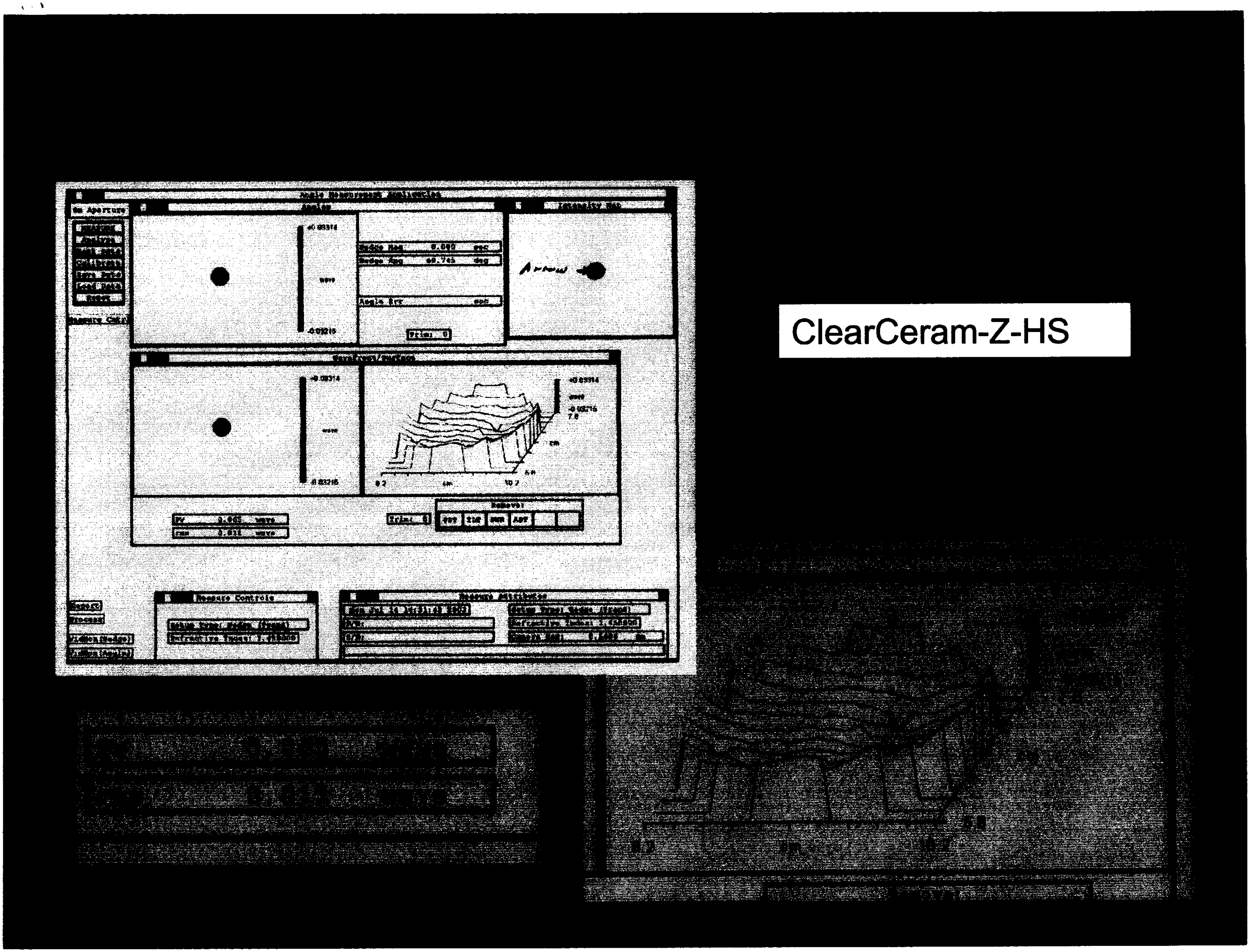
TE)

- CTE is 0±10 ppb/^{0}C over 0 to 5
  - No data on turning point.

Task Technical Status




Premium Grade ULE
Arrow


ClearCeram-Z-HS

CTE Data will appear here

Assessment

- This task is producing preliminary results that show a new optical material, ClearCeram-Z-HS from Ohara Corp., may be more appropriate for use in LISA than other low CTE materials.