

# EEPROM Bit Failure Investigation

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## Introduction:

Two EEPROM single bit failures were reported by a recent JPL space mission. One failure was observed approximately six months into flight and the second bit failure approximately seven months later. The two bit failures were located in the same physical MCM package but different dies. In both cases, the contents changed from "0" to "1", i.e. from charged state to discharged state. This presentation summarizes the reliability investigation of these EEPROM single bit failures.

## Reliability Analysis and Experimental Details:

A statistic reliability analysis on the EEPROM bit failures has been performed based on the EEPROM data sheet and its reliability report provided by the manufacturer. The analysis shows that an intrinsic EEPROM data retention bit failure should not be expected within the first six years of operation under operating condition of 50°C to 60°C, which was the temperature of the mission observing the two bit failures. However, an extrinsic bit failure resulting from a weak cell can happen any time before an intrinsic bit failure occurs. Furthermore, because of process induced and/or poorly programmed extrinsic reliability characteristics, weak cells may have several order of magnitude lower data retention or endurance lifetime and much higher failure rate and cannot be predicted in most cases. The basics of failure mechanisms for weak cells are the same as that for nominal cells, but the activation energy may be much lower and therefore weak cells are more susceptible to high temperature operation. We believe that the weak cells, either process induced or poorly programmed, may be the root cause of failures.

In order to investigate the reliability characteristics and obtain the activation energy of the weak cells, a diagnostic and write/read cycle testing plan was designed by modulating the write voltage externally to emulate weak cells. The experiment was performed on EEPROM chips from the same manufacturer. In the study, we have demonstrated that weak cells fail earlier and have lower activation energy as we expected. Nominal cells can become weak cells if the memory chip is not operated properly.

## Conclusion:

We have concluded that "weak cells", due to either process-induced defective cells or poorly programmed cells, may be the root cause of the bit and page failures observed, since the statistic reliability analysis on the EEPROM indicates that an intrinsic EEPROM data retention bit failure should not be expected within the first year of operation under 60°C. Diagnostic and write/read cycle testing to emulate weak cells were designed and performed to demonstrate that weak cells can fail earlier than a properly programmed array and that nominal cells can become weak cells if the memory chip is not programmed or operated properly. Read cycles can accelerate data retention failures on these weak cells. We have also concluded that the program timing of the EEPROM is very sensitive and that board timing margins need to be extensively analyzed to avoid possible program timing induced weak cells, which in turn may become early bit failures. It is necessary to point out that since the failed bits on the mission which observed the bit failure were not re-written, we can not verify our hypothesis with an actual failed part.

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# Outline

- Observations
- Reliability Analysis
  - Endurance versus data retention
  - Radiation
  - Excessive read cycles
  - High temperature operation
  - “Weak cells”
- Experimental Details
- Conclusions
- General Recommendations

# Observations

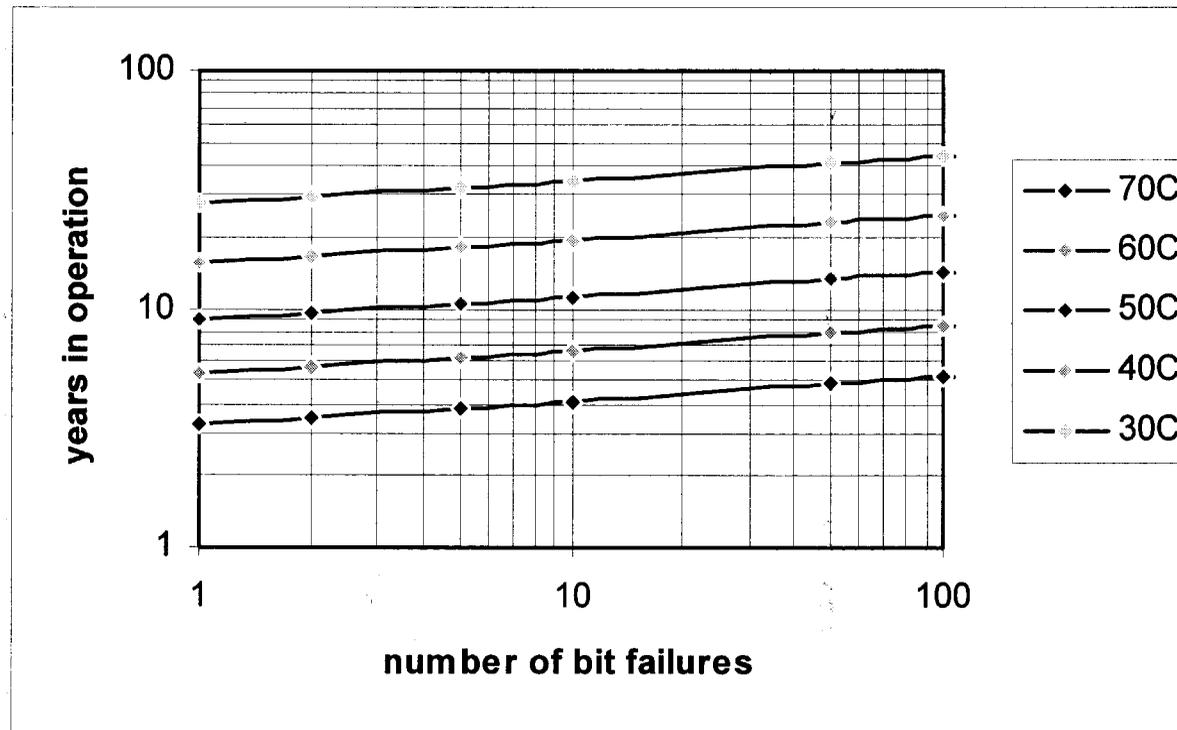
- One EEPROM bit failure was observed on a space mission approximately six months into flight and a second bit failure approximately seven months later. The two bit failures were located in the same physical MCM package but different dies.
  - Bits changed from "0" to "1", i.e. from charged state to discharged state
- What is the possible root cause?

# Reliability Analysis

- Endurance versus data retention
  - 10X shorter life of data retention after 10,000 erase/write cycles per manufacturer data
  - The space mission only had around 10 write/erase cycles
  - Bit failures observed appeared to be data retention resulting from cell discharge
- Radiation
  - The process technology of the EEPROM (not CMOS technology) under investigation is robust to TID in excess of 100krad while the mission to date has less than 2krad
  - Other study demonstrated that no errors occur in a properly programmed device with the technology after over  $1e7 \text{ cm}^{-2}$  ions of high LET ions while the total fluence of particles capable of inducing a bit error at 2krad is approximately  $1e4 \text{ cm}^{-2}$
- Excessive read cycles
  - Impact of read cycles on discharging cells is much smaller than that of write cycles unless excessive read cycles are performed on weak cells

# Reliability Analysis

- High temperature operation
  - An EEPROM data retention bit failure should not be expected within the first seven years of operation at 55°C.

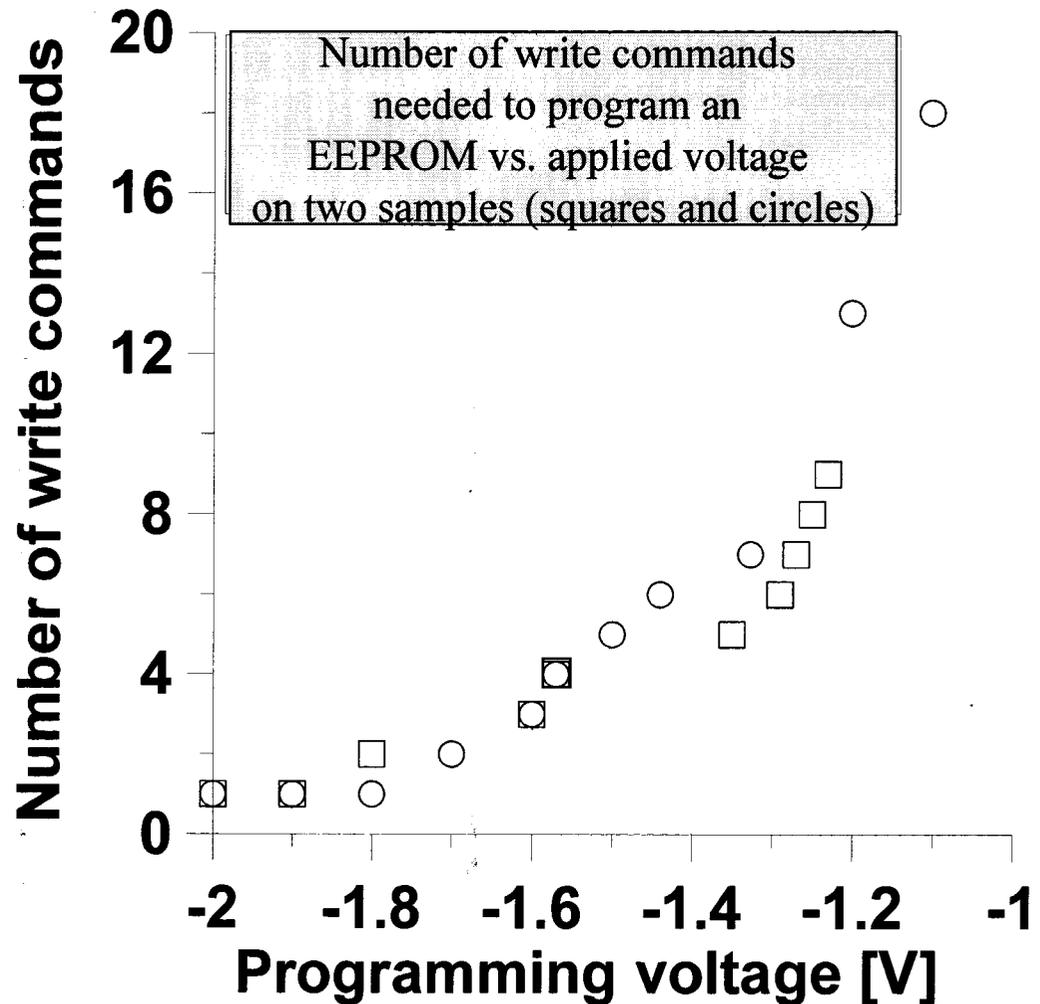


# Reliability Analysis

- “Weak cells”
  - Weak cells can be process-related.
    - Process-induced weak cells can be defective cells resulting from defective oxides, oxide thinning, oxide excessive trapping, abnormal leakage paths through silicon or oxide, adjacent via bridging, adjacent metal bridging, metal flakes, metal voids, etc.
  - Weak cells can be induced by poor timing and/or noise margin when programming.
    - Cells may either have lower write voltage or shorter write time, which results in less charge stored in the cells to begin with and therefore shorter data retention lifetime.
  - Reliability of weak cells has the following characteristics.
    - Shorter lifetimes and higher failure rates
    - Lower activation energies

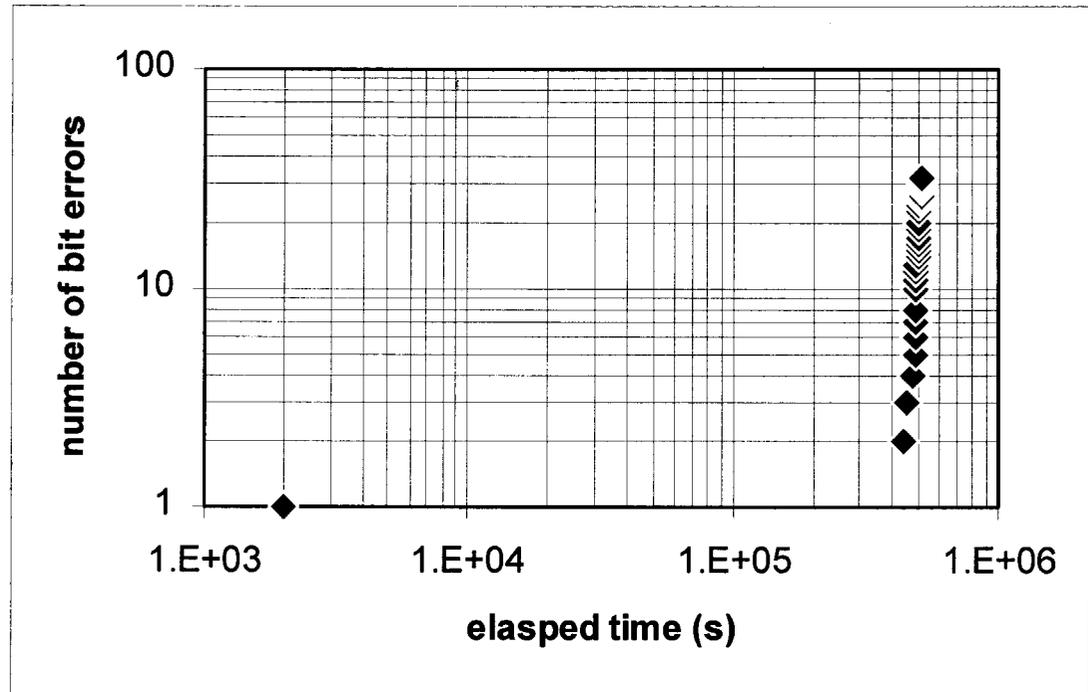
# Experimental Details

- Experiment design
  - Partially programming EEPROM cells by modulating voltage associated with charge pump to emulate weak cells, which have less charges



# Experimental Details

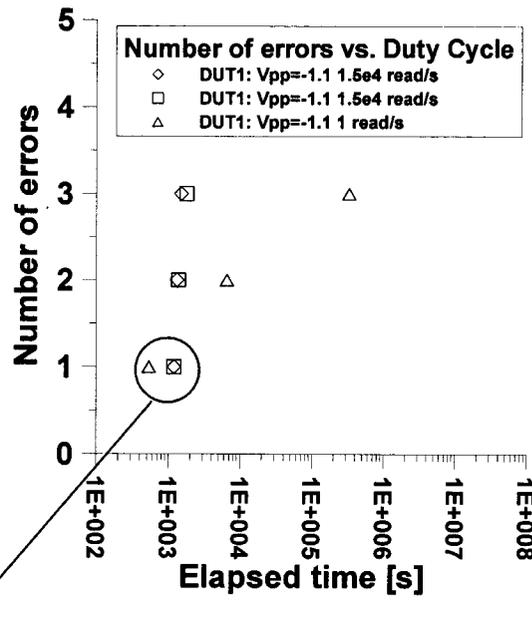
- EEPROM bit error growth
  - Function of time
  - $1.5 \times 10^4$  DUT readouts per second
  - Lifetime for weak cells is significantly shorter than 7-year prediction based on the manufacturer's data retention information (slide 5)



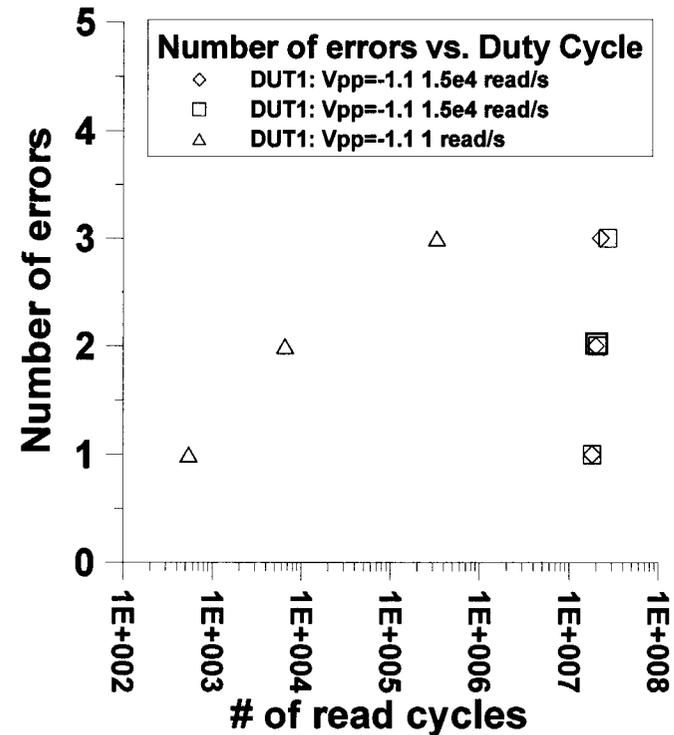
**Number of bit error as a function of elapsed time for the emulation of weak cells**

# Experimental Details

## The relative contribution of readout frequency on bit failures



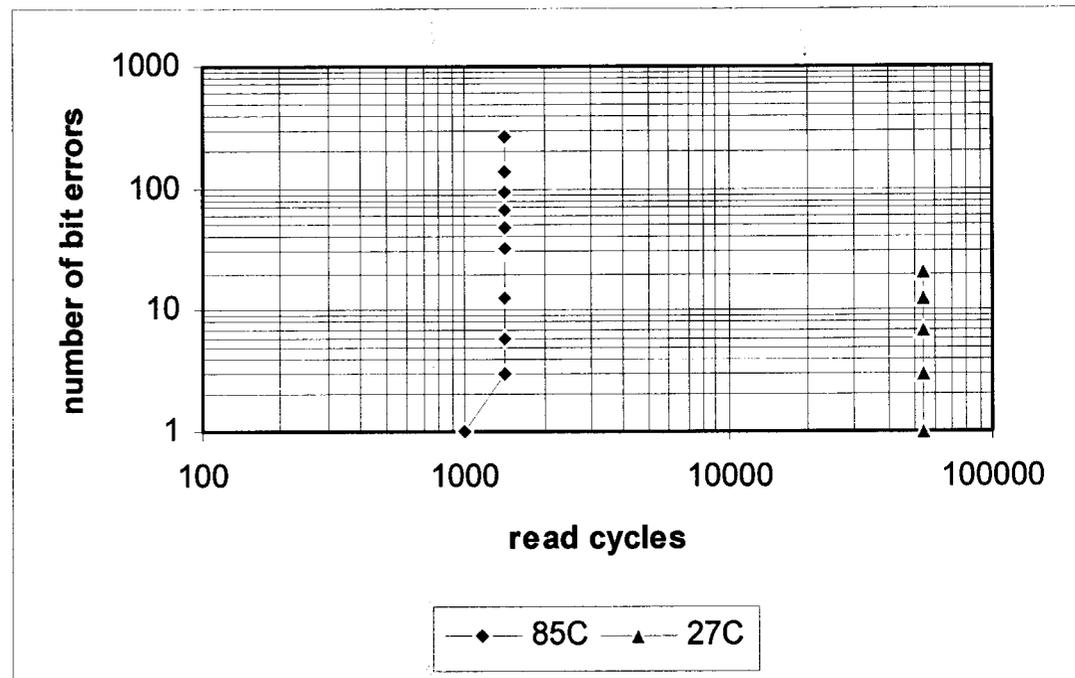
- This consistency implies that the electric field present during readout does not significantly affect the time it takes to report the first error. It also indicates that the first error is predominately an issue of the data retention characteristics of the EEPROM, and the electric fields present during a read operation have a second effect.



- The frequency of device reads does have an effect on the rate of error growth. After the first bit error, higher read frequency yields faster error growth rate.

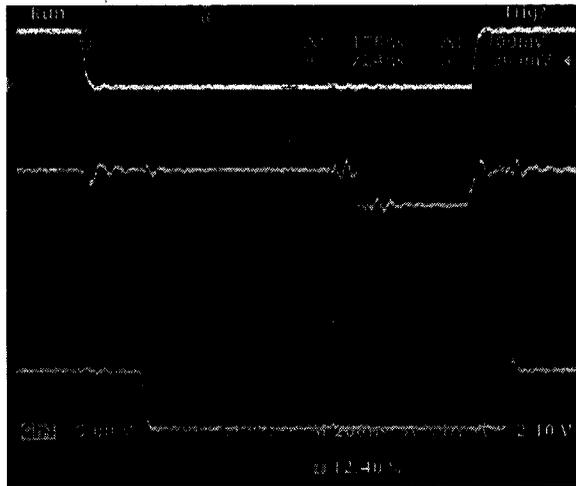
# Experimental Details

- Activation energy for bit failures
  - $E_a$  is expected to be smaller for weak cells than for intrinsic cells
  - 1.1eV versus 0.5~0.7eV
  - Weak cells can be more easily thermally activated to discharge



Number of bit failures as a function of read cycles at 27°C and 85°C for activation energy estimate.

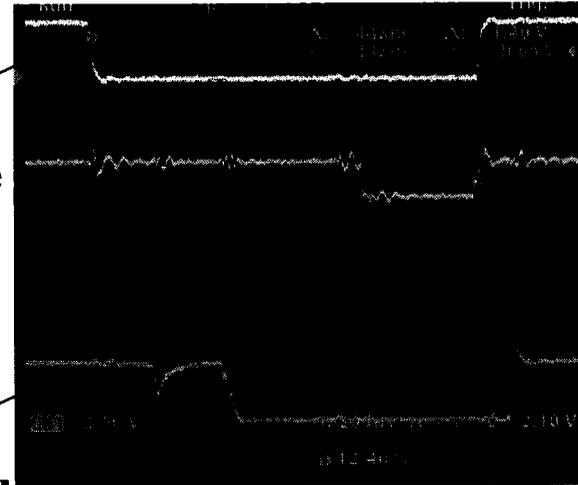
# Experimental Details



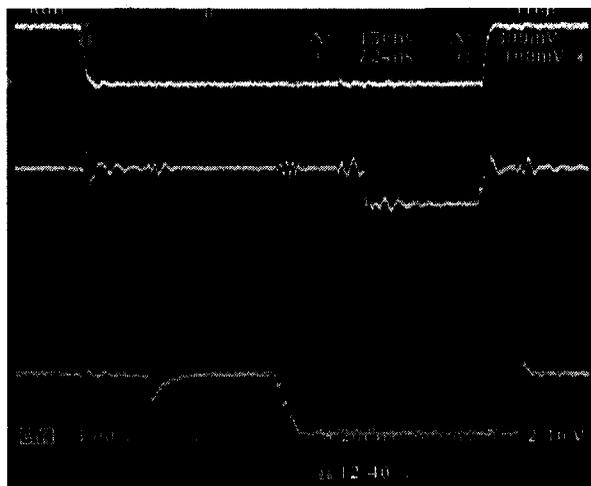
**Good bit.**

**Chip Enable**

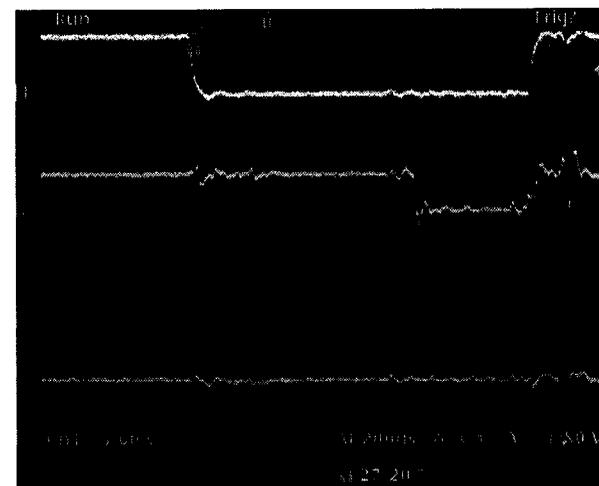
**bit monitored**



**Bit continue failing**



**Bit beginning to fail**



**Bit eventually failed**

# Conclusions

It is necessary to point out that since the failed bits on the mission which observed the bit failure were not re-written, we can not verify our hypothesis with an actual failed part.

# Conclusions

- “Weak cells” are most likely responsible for early EEPROM failures.
  - Diagnostic and write/read cycle testing to emulate weak cells have been designed and performed to demonstrate that weak cells can fail in a very short period of operation time with or without excessive read cycles
- “Weak cells” can be induced by process and/or poorly programmed timing and/or noise margin.
  - Nominal cells can become weak cells if the memory chip is not operated properly.
  - Program timing of the EEPROM is very sensitive and that board timing and noise margin needs to be extensively analyzed to avoid possible program timing induced weak cells, which in turn may become early bit failures.
- When using EEPROM for space applications
  - Design in bit and page redundancy to allow for programming around failed bit or pages.
  - Make sure programming timing meets EEPROM operation specification with necessary margin.
  - Do not exceed the manufacture's specified number of write/erase cycles and specified operating temperature
  - EEPROM should be written all “0” and then read for a number of read cycles before burn-in test or any higher temperature bake or testing for EEPROM pre-screen to mitigate against extrinsic escapes.