

Development of a Novel Power System for Space Applications

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Abstract—

The X2000 Advanced Avionics Project is developing a new generation of power system building blocks. Using application specific integrated circuits (ASICs), power switching modules and electronic slices to construct a scalable power system that can be used on multiple deep space missions including future missions to Europa, Jupiter and Mars. The key developments of the X2000 Power System effort are four power ASICs, one power module for switching, and two types of power slices used for switching and control. These components enable a modular and scalable design approach, which can result in a wide variety of power system architectures to meet diverse mission requirements and environments. Generic Power Switch slices can be used for the power distribution to regular spacecraft loads, for the control of spacecraft propulsion valves and for the actuation of pyrotechnic devices. The number of switching elements per load, pyrotechnic firings and valve drivers can be scaled depending on mission needs. Telemetry data is also available for all the switch elements via an I²C data bus. The X2000 power system components enable power management and distribution for a variety of power buses and power system architectures. Power bus architectures may include various types of energy storage and power sources. Volume and mass savings can be as high as 40% and 50% respectively. In addition to volume and mass savings the X2000 power system is being developed for use in extreme radiation environments such as those surrounding Jupiter. This paper will describe the power ASICs, Module and Slices, the key performance capabilities, and the power system architecture of a sample system. In addition the current development status of the X2000 Power System components will be presented.

1. Introduction

Potential
The Deep Space Avionics Project (DSA Project) formerly known as the X2000 Advanced Avionics Project is a Jet Propulsion Laboratory project developing a new generation of complete avionics slices and modules for use on future deep space missions. The effort includes the development of electronic components & boards, which can be used as building blocks in the design of generic spacecraft avionics systems. All avionics slices and modules are designed for use in centralized or distributed spacecraft architectures. Specifically the power subsystem components are being developed for a low voltage (30V) power management and distribution subsystem. The power subsystem components may be included on missions such as the recently proposed mission to Jupiter and its moons. Such missions to deep space are generally challenging due to their duration. The majority of these types of missions have a longer than 10 year life requirement. As an added complexity missions to Jupiter and its moons are surrounded by an extreme radiation environment. These two combined challenges force the research to improve the lifetime and radiation

tolerance of electronic components and parts used in the design and fabrication of power system modules. In general components used in state of the art low voltage power system designs are limited to surviving an environment less than 300 Krad. Specifically Field Programmable Gate Arrays (FPGAs) are limited to surviving in a 100Krad environment and other linear control circuits such as FET drivers, operational-amplifiers & comparators are limited to 300Krad environments. The Deep Space Avionics project has taken the approach of developing a set of Application Specific Integrated Circuits (ASICs) as the path to achieve power electronics, which are radiation tolerant to higher levels (>1 Mrad). The current Deep Space Avionics Project is leveraging off previously sponsored work by the Jet Propulsion Laboratory (JPL). Previously, JPL had teamed with Boeing (ASIC Design) and Honeywell (ASIC foundry) under the X2000 Integrated First Delivery Project. During this past effort the team developed an analog ASIC cell library to be used for future ASIC designs. By combining the analog cell library developed by Boeing and the digital circuit cells

developed by Honeywell, mixed signal ASICs for power applications, which are 1 Mrad hard, can be designed and produced. This challenging process of ASIC design and fabrication is currently being proven. Although the challenges are elevated the benefits can be rewarding for multiple missions. Using mixed signal ASICs for power system design can reduce the number of components necessary for a system. By using components that are inherently radiation hard, less shielding is required and higher reliability is achieved, resulting in overall mass and volume reduction. This result is mostly beneficial to spacecraft designers that are constantly constrained by volume and mass requirements.

The electronic components being designed for use in a low voltage power management & distribution subsystem are five ASICs, one switching module and two electronic boards.

The following five ASICs are being developed:

1. Switch Control ASIC – High Side (SCAH)
2. Switch Control ASIC – Low Side (SCAL)
3. Analog Interface ASIC(AIA)
4. Command Interface ASIC (CIA)
5. Pulse Width Modulator ASIC (PWMA)

The following one switching module is being developed:

1. Power Actuation and Switching Module (PASM)

The following two electronic boards are being developed:

1. Power Switch Slice (PSS)
2. Power Control Slice (PCS)

All ASICs are inherently 1 Mrad hard as a result of the Honeywell fabrication process. The two switch control ASICs (SCAH – SCAL) are used in the PASM design. The PASM along with the AIA and the CIA are used in the design of the two electronic boards/slices. The PWMA can be used in the design of various levels of power and voltage power converter units, therefore, producing a variety of 1 Mrad hard power converter designs. These converters can easily be used for diverse applications on a spacecraft ranging from powering science instruments to providing housekeeping power to the power subsystem components. In turn the two generic electronic boards along with the power converter units can be used in the design of a distributed or centralized power system. A combination of these boards can be used for the purpose of switching most types of avionic loads, the firing of pyrotechnic devices, and the actuation of valves. In addition, these boards can be configured to control a regulated or a unregulated spacecraft power bus. The power bus can be designed to have any combination of power source and energy storage device. Figure 1 exhibits the flow of the DSA power subsystem components leading to a centralized configuration, assembled in a commercial Compact Peripheral Component Interconnect (Compact PCI) chassis. The

individual power ASICs, modules and boards are described in the following sections.

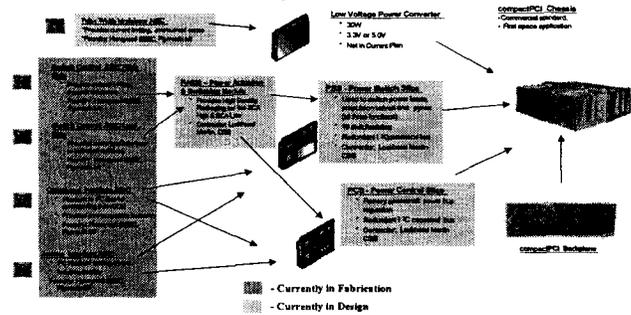


Figure 1. Flow of Deep Space Avionics Power System Components

2 Power Subsystem Building Blocks

2.1 Switch Control ASICs (SCAH – SCAL)

The SCAH and SCAL ASICs are designed as a chipset to control one solid-state switch (such as a MOSFET) for general switching purposes. The chipset is fabricated on the Honeywell HX2000 foundry and the first ASICs were completed in June 2003. The chipset has the capability to be powered by redundant 5V power supplies. Power-on-Reset (POR) circuitry was designed to keep the circuit in a known state during initial power on and in the event of power loss. On chip voltage references are designed for both ASICs. The ASICs have the capability of providing analog telemetry for both current and voltage for each solid-state switch they control. Logic command inputs are compatible with both 3.3V & 5.0V standard CMOS logic. Currently the chipset is designed to interface with a 100V MOSFET appropriate for use in most lower voltage applications. However, with adequate isolation between the interfaces of the two chips it can be used in higher voltage applications. Figure 2 exhibits a block diagram of the SCA chipset.

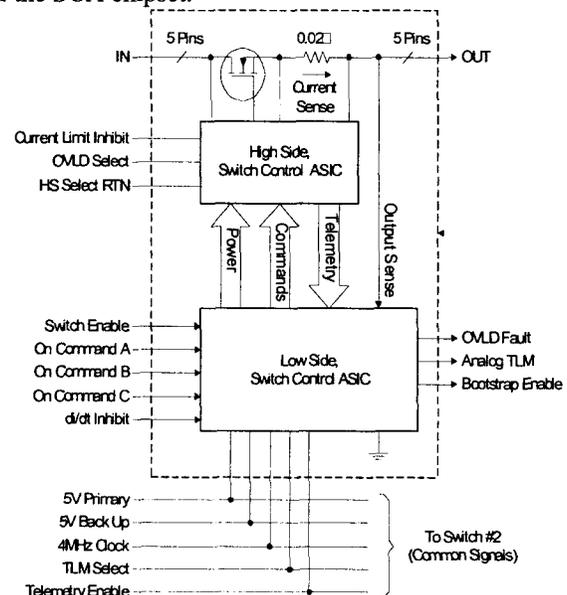


Figure 2. Switch Control ASIC Block Diagram

2.2 Analog Interface ASIC (AIA)

The AIA provides ground isolation between the data buses and the power system electronics. The AIA receives and processes commands to the Command Interface ASIC via two I²C transceivers. Isolation of these signals is provided by a transformer pack mounted on the board. An internal 8.25Mhz clock is designed on chip with the capability of interfacing with an optional external clock. An on-chip oscillator watchdog forces the AIA in a fail-silent mode if the event of an oscillator failure. This chip is powered by redundant 3.3V power sources. A power-on-reset signal must be provided by an external source such as a power converter. Like the SCA, it is also fabricated on the Honeywell HX2000 process, which makes the chip 1Mrad hard. The first ASICs were produced June 2003. Testing of the ASICs is currently being conducted. Figure 3 exhibits a block diagram of the AIA. In applications where fault containment regions must be minimized two AIAs can be used to interface with one Command Interface ASIC creating a fault tolerant data bus interface on the board.

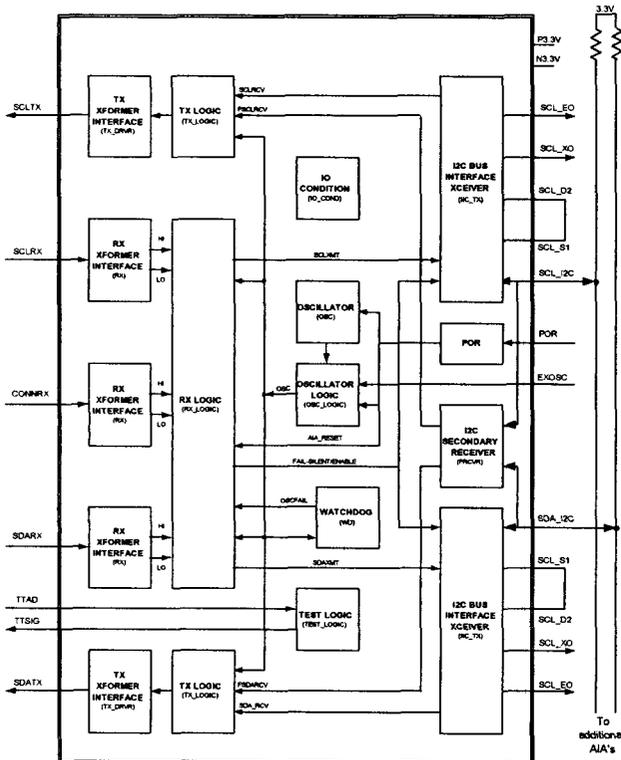


Figure 3. Analog Interface ASIC Block Diagram

2.3 Command Interface ASIC (CIA)

The CIA is a micro-controller that is based on a M8051 core processor with multi-frequency operation. The CIA has two modes of operation, one at 16.5 MHz and another at 8.25 MHz. In addition it has a sleep mode for low power consumption. It can interface with the central processing unit via an I²C standard data bus. Isolation is provided by the transformer pack mounted on the board. The design provides for two I²C ports for flexibility of fault containment region design. There is 8KB and 12KB of program and data memory respectively available on

chip. The CIA also has the capability to boot up from an external ROM and store data to a larger external memory device. The chip can be powered by two 5.0V sources for the analog circuitry and two 3.3V sources for the digital circuitry. Both voltages are then cross-strapped internally for higher reliability. Internal power-on-circuits (POR) are also designed to hold the circuit in a known state during initial power on and in the event of a power loss of both power supplies. In addition a custom 8-bit analog-to-digital converter, which processes the analog telemetry inputs from the switch control ASIC is built-in. Capability for current & voltage monitoring exists. An internal watchdog is also incorporated in the design and forces a fail silent state in the event of a failure. Figure 4 exhibits a block diagram of the CIA. The CIA is currently being fabricated on the Honeywell HX3000 process line and the first wafers will be produced in October 2003. Testing of individual ASICs will follow subsequently.

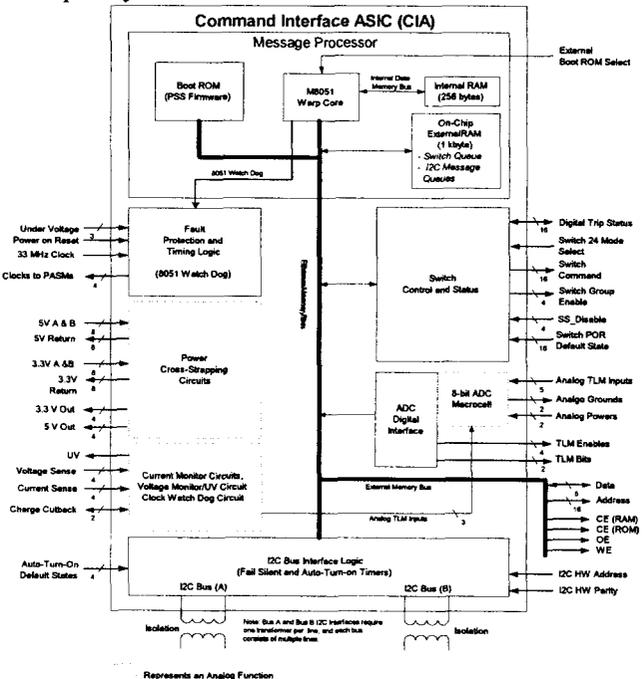


Figure 4. Command Interface ASIC Block Diagram

2.4 Pulse Width Modulator ASIC (PWMA)

The PWMA is currently in design. The objective of this effort is to design a single ASIC that can be used as a building block for a family of radiation hardened power converters. Taking advantage of the analog cell library created for the other ASICs along with the design and modelling tools the PWMA design process has a high likelihood for success. The ASIC will contain necessary functions for power conversion such as pulse width modulation, synchronous rectification, voltage references and drivers for FETs. As a DC/DC converter building block, the PWMA will accommodate isolated and non-isolated converters using typical spacecraft input bus voltage as large as 130V. The design of the ASIC is

currently being performed by JPL and fabrication is planned for early 2004.

2.5 Power Actuation and Switching Module (PASM)

The PASM is a solid state general purpose switching module. Each PASM has two switches that can be used in various configurations. These switches can be configured in a series/parallel or bi-directional connection to the load, thus, providing better flexibility to system engineers when establishing the system architecture. The PASM package design is based on a new technology that enables higher density packaging of ASICs. JPL's industry partner Lockheed Martin - Commercial Space Systems (Newtown, PA) is currently designing the PASM. The Power High Density Interconnect (Power HDI) packaging technique developed by General Electric is being used for the PASM. The PASM provides current and voltage telemetry, current trip and limit capability, soft start (di/dt) and back EMF suppression for inductive loads. The current trip and limit capability of the PASM is 3.0A and 5.0A respectively. The individual switches are command resettable once tripped. In addition overload fault telemetry output is available. Nominal limit for di/dt control is 7.5 A/ms. Figure 5 exhibits a block diagram of a PASM.

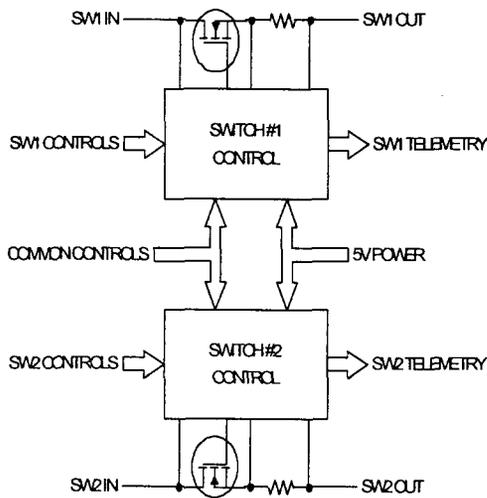


Figure 5. PASM Block Diagram

2.6 Power Switch Slice (PSS)

Each power switch slice is an electronic board, which can be used for switching various spacecraft loads. The PSS is designed using two AIAs, one CIA and eight PASM's. Each PSS is in a 3U Compact PCI configuration and provides the capability to individually command sixteen switches on a board. The power system design becomes scalable by using a number of PSS boards, which is determined based on the quantity of loads that a specific spacecraft requires to switch and also on the architecture and reliability philosophies. Switches assigned to loads can be classified as loadshed or critical for the proper operation of a spacecraft, depending again on architecture

and reliability philosophy. Commands are received via I²C to the CIA. The CIA processes and can command the individual switches in steady state or pulse mode. Pulse mode turns ON a switch for a specified duration after a specified delay. Steady state will turn a load ON or OFF indefinitely until commanded otherwise. The pulse mode

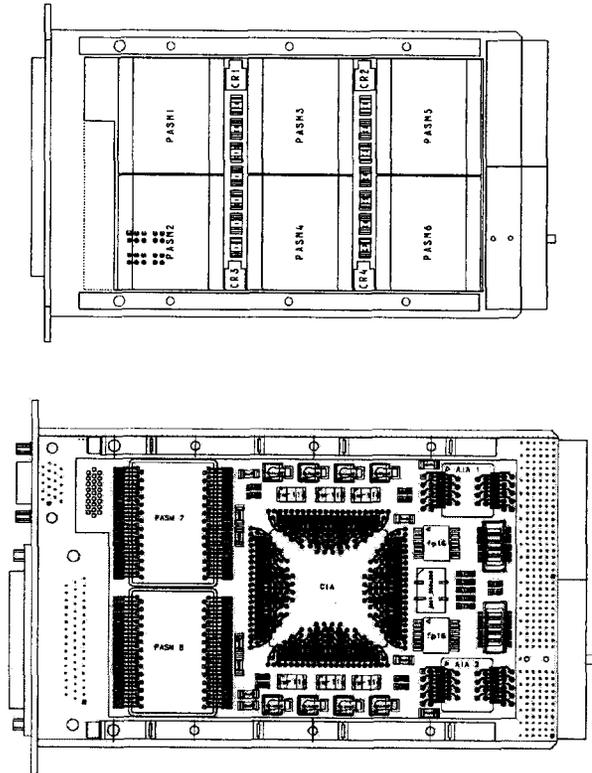


Figure 6. PSS Floor Plan

can be used in the design of valve drive electronics and the steady state mode can be used in switching regular spacecraft loads such as heaters, science instruments etc. The PSS can also be configured for the firing of various pyrotechnic devices. Utilizing the switch pulse command and the switch enable command in the design of the pyrotechnic system allows for additional safety protection, resulting in a more robust pyro system. The majority of the functionality on the PSS board is embedded in the design of all the Power ASICs being used. By using the power ASICs and other discreet radiation hard devices the PSS is inherently radiation hard to 1Mrad. Figure 6 exhibits a floor plan of the two sided PSS board.

2.7 Power Control Slice (PCS)

The PCS is an electronic board that is used for power bus regulation. Each power control slice is designed using two AIAs, one CIA, six PASM's and an external memory device. The external memory device stores the control algorithm for the power bus. Currently the algorithm is designed to control a direct energy power bus. The direct energy power bus is assumed to have a radioisotope thermoelectric generator similar to those flown on the

Gallileo and Cassini missions as the main power source. In addition the power bus has a lithium ion battery for energy storage for load leveling and power negative events such as orbit insertions. By storing the control algorithm in the local memory on the PCS board, the PCS can be easily reconfigured for other control functions. In the current configuration the PCS control loop balances the amount of RTG current available to the battery with the spacecraft load demand, while limiting battery charge current. The PCS board is also in a 3U Compact PCI configuration with 12 solid state switches, eight are used in the power bus control and the remaining four are utilized for auxiliary loads such as a protected loads bus (pyrotechnic device bus). A single PCS can be used to control a power bus. However, configuring the system with three PCS boards, which can be majority-voted, allows for a single fault tolerant design.

3.0 Sample Power System

Figure 7 exhibits a block diagram of a sample power system configured using Deep Space Avionics power system components. A number of power switch slices are used for switching regular spacecraft loads, pyros and propulsion valves. Three power control slices are controlling the RTG to its peak power point and also regulating the battery charge current.

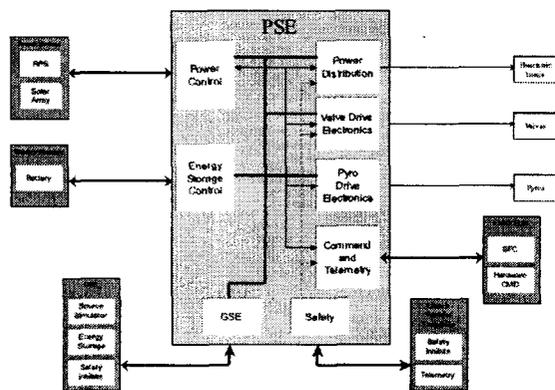


Figure 7 Sample Power System Block Diagram

4.0 Summary

The Deep Space Avionics project is developing electronic components that are high reliability and radiation hard for future spacecraft power systems. These components can be used to architect a centralized or distributed power system for future long life deep space missions such as missions to Jupiter. Using these components a power system can be designed to have a regulated or non-regulated power bus. In addition, a power system designer is not limited in the types of power sources and energy storage devices that can be selected. Commanding of the power system is achieved through an I²C data bus. Power distribution to a variety of loads such as heaters, pyros and propulsion valves can be achieved by using the same generic building blocks being developed. The basis of the building blocks being developed is a set of five mixed-signal ASICs (AIA, CIA, SCAH, SCA and PWMA) one switching module (PASM) and two electronic boards (PSS and PCS). To date three ASICs have been designed and fabricated and are under evaluation. The remaining of the components are in design and are planned to be tested in mid 2004.

Acknowledgment

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