

A High Voltage Dickson Charge Pump in SOI CMOS

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Abstract

An improved charge pump[†] that utilizes a MOSFET body diode as a charge transfer switch is discussed. The body diode is characterized and a body diode model is developed for simulating the charge pump circuit. An increase in voltage pumping gain for a silicon-on-insulator (SOI) Dickson charge pump is demonstrated when compared with a traditional bulk CMOS Dickson charge pump. A 6-stage Dickson charge pump was designed to produce a 20 V output from a 3.3 V supply, using a 4 MHz, two-phase non-overlapping clock signal driving the charge pump. The design was fabricated in a 0.35 μm partially depleted SOI CMOS process. An efficiency of 72% is achieved at a load current of approximately 20 μA .

I. Introduction

As the desire for unmanned spacecraft and interplanetary exploration increases and the enabling technology comes to fruition, MEMS devices such as microgyroscopes (for navigation), microseismometers (for detecting seismic activity), micrometeorological equipment (such as a microhygrometer for measuring humidity), mass spectrometers (for identification and classification of chemical species), and micropropulsion engines become invaluable in the cost-effective push in space related research [1]. MEMS devices such as these require a range of DC bias voltages, from 15 V to well over 60 V, to perform the necessary environmental interactions [1-3].

Among the different on-chip, high-voltage generators, the Dickson charge pump is a classic solution [4]. However, the pumping efficiency of the bulk-CMOS Dickson charge pump is degraded due to the threshold voltage drop of the charge transfer switch (CTS) transistors, and the voltage gain of the pumping stages closer to the output is further degraded by the increase in threshold voltage due to the body effect of these MOSFET switches [5]. The utilization of SOI MOSFET body diodes in place of the typical bulk MOSFET switches reduces the voltage drop across the switches significantly. The goal of this paper is to present improvements achievable in an SOI Dickson charge pump circuit as compared to a bulk CMOS realization. While no comparisons to other charge pump circuit topologies are drawn, the improvements should be equally applicable to many other bulk CMOS DC/DC converter circuits when implemented in SOI.

II. Background

Two popular topologies for stepping up DC voltages are the charge pump DC/DC converter [4] and the boost switching DC/DC converter [6]. Each of these DC/DC converter topologies offers performance advantages and disadvantages. In the past, the boost converter has been the predominantly used converter. The boost converter can provide much more power than the charge pump and is more than 90% efficient, but the boost converter requires large inductors. For many on-chip applications it is desirable to avoid the use of inductors because of their size, non-linearity, and interference. It is for this reason that charge pumps have been so widely used in integrated circuit (IC) applications. Charge pumps are designed using MOSFETs or diodes as switches, and they utilize energy-transfer capacitors instead of inductors, thus enabling them to be readily implemented on-chip.

Charge pump switches can be diodes, diode-connected MOS transistors, or MOS body diodes. While bulk MOSFET transistors have a significant parasitic drain capacitance and latch-up issues, an SOI process can be used to overcome these limitations [7-9]. Other compelling advantages of SOI technologies are excellent tolerance of transient radiation effects and superior thermal properties [8,10].

In bulk CMOS circuits, the p-n junction between the substrate and well forms a "parasitic" diode. The breakdown voltage of this diode is a limiting factor for pumping high voltages if this type of transistor is used in a charge pump. If a potential in the charge pump is reached which is greater than the value of the breakdown voltage, the circuit will cease to operate properly, if at all. However, in an SOI process this substrate-well diode does not exist, since the transistors are isolated from each other and built upon an insulating oxide layer. With proper circuit topology selection, this affords the opportunity to pump to much higher voltages on-chip, where the limitations will now be oxide breakdowns for capacitors and/or the buried oxide layer [11].

III. SOI MOSFET Body-Diode Switch

In an SOI process, each MOSFET body is isolated from other neighboring transistors due to the buried oxide (BOX) layer. The cross-section of an NMOS SOI transistor is shown in Fig. 1. The two p-n junctions of this structure form a back-to-back diode configuration as indicated in the drawing [12]. The MOSFET CTS connection used in the SOI Dickson charge pump developed in this work is implemented by connecting the gate (G), drain (D), and body (B) together. In this implementation, the floating-body of the NMOS is connected to the drain, thus shorting the junction from the p-type body to the n-type drain. Now, only one diode exists

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between the gate-drain-body connection and the source. In this configuration the gate-drain-body connection will serve as the anode and the source as the cathode. This technique is not advisable in bulk CMOS technology. Consider an n-type wafer, where each NMOS switch is put into its own floating p-well (i.e., the well is not connected to the lowest potential in the circuit). If the p-well, n⁺ drain, and gate are connected together a parasitic bipolar transistor (n⁺ emitter = source, p-well = base, n-epi = collector) results that can turn on and conduct through the n-epi layer shared by all circuitry.

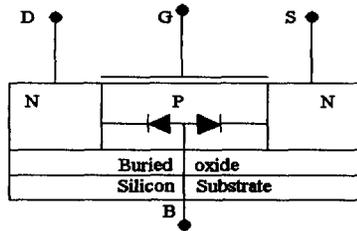


Fig. 1. Cross-section of an SOI NMOS device demonstrating the body diode connections available.

Fig. 2 shows the two-dimensional Medici [13] simulation results of an SOI NMOS body-diode. In Fig. 2 (a), the cut-in voltage of the silicon body diode is reduced from its typical value of 0.7 V to approximately 0.4 V due to the charge accumulation under the gate as the body-diode anode (gate-drain-body connection) voltage increases. Fig. 2(b) shows a cross-section of the NMOS body diode forward biased at 0.6 V to better illustrate the gate-induced cut-in voltage reduction. In this figure, the gate electrode (dark gray) is slightly discernible on the top right of the structure above the gate oxide (black), while the source electrode (dark gray) is shown on the left side of the figure and is separated from the gate electrode by an interlayer dielectric (black). The thick black region in the bottom of the figure is the BOX layer and the active Si region is the multi-shaded gray region between the BOX layer and electrodes. The vertical white line represents the p-n junction of the body diode, where the right-most Si area is the anode or p-type channel region of the MOS structure and the left-most Si area is the cathode or n-type source region of the MOS structure. The shading in the Si region represents the electron concentration at 0.6 V forward bias, where white is a highly concentrated region of electrons around the source contact, light gray is the moderately doped source region, and dark gray is the low-electron concentration in the p-type channel region. The accumulation of electrons with a positive gate bias is shown as the light gray region immediately under the gate. This accumulation of charge in the junction vicinity creates a diode with a decreased built-in potential just under the gate oxide. The increase in gate voltage increases the number of available carriers for conduction, similar to the effect of increasing diode temperature.

In this work, the Honeywell 0.35 μm SOI process was

used to fabricate the Dickson charge pump utilizing the body diode of NMOS transistors. BSIM3v3.1 MOSFET model parameters were available for the design of the circuit; however, this model does not give accurate characteristics of the body diode, particularly when the body diode is used as described above [14]. Therefore, a new model for the body diode was needed to precisely characterize its behavior.

The body diode of the NMOS is modeled using a standard diode model [15]. The diode model parameters listed in Table 1 are used to fit the measured body diode on-state characteristics. The simulated on-state characteristic of the body diode is compared with the measured body diode on-state curve in Fig. 3. These on-state curves are virtually identical, demonstrating the model accurately describes the behavior of the body diode.

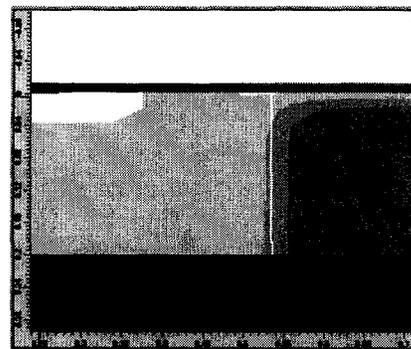
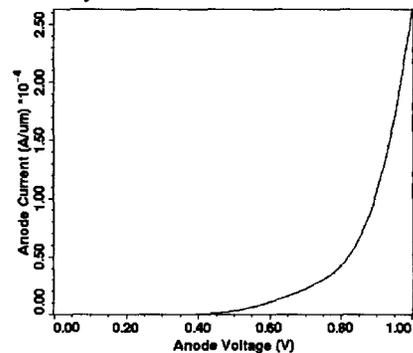


Fig. 2. a) On-state simulation result of 2D SOI body diode and b) 2D structure demonstrating increase (lighter region) in electron concentration under gate with increase in body-diode anode voltage.

Table 1. Body Diode Modeling Parameters

Parameter	Value
I_s	25 nA
n	2
R_s	14.975 Ω

The relevant diode model parameters are the saturation current I_s , the emission coefficient n , and the diode series resistance R_s .

IV. Improved Dickson Charge Pump

Fig. 4 shows the complete circuit of a 6-stage improved Dickson charge pump DC/DC converter; including charge

pump circuit, non-overlapping clock generator, and buffers. The operation of the charge pump is identical to that of the Dickson charge pump topology [11]. In short, when $clk1$ goes high, the voltage across the respective capacitors connected to $clk1$ stays constant thus forcing the top-plate voltage to increase by the magnitude of the clock signal (3.3 V). This turns on the diodes immediately to the right of those capacitors and begins to transfer charge to the capacitors connected to $clk2$. Then, when $clk1$ goes low and $clk2$ goes high the same dv/dt action occurs on the capacitors connected to $clk2$ now turning on the other diodes, transferring charge left-to-right in the circuit, and successively pumping up the voltage. The diodes shown in the figure are the body diodes of SOI NMOS transistors as discussed in section III. The value of the capacitor in each stage is 30 pF. The value of the parasitic capacitance is estimated to be 6 pF or 20% of the total capacitance at each stage. Typically, the ratio of the parasitic capacitance to the capacitor value is between 0.1 and 0.2 [16].

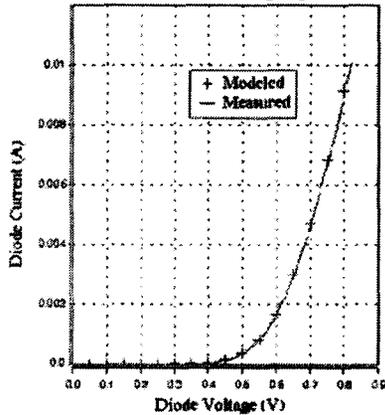


Fig. 3. Measured (—) and simulated (+) body diode on-state characteristic.

Two non-overlapping clocks are needed in the Dickson charge pump to prevent clock feed through. The circuit used here requires one clock signal input and generates a two-phase non-overlapping clock. The amount of overlap is determined by the delay through the NOR gate and the buffer on the NOR gate output. When the input clock goes high, this forces $clk1$ low and subsequently $clk2$ high. When the input goes low, $clk2$ becomes low. Only after $clk2$ goes low, $clk1$ can go high. Buffers are required at the output of the two non-overlapping clocks in order to drive the capacitors at each stage.

The voltage gain of a charge pump is primarily a function of the number of stages, n , in the pump. An n -stage Dickson charge pump ideally has a voltage gain equal to $n+1$. The output voltage of this six-stage charge pump will ideally be $(6+1)*V_{in}$ or 23.1 V for a 3.3 V input. In actuality, the output voltage also decreases by 0.7 V per switch when a typical silicon diode is used in the circuit. So, under no-load

conditions a six stage charge pump with an input voltage of 3.3 V would have a best-case expected output voltage of approximately $23.1 V - 7*0.7 V = 18.2 V$. On the other hand, utilizing the SOI body-diode described above with a 0.4 V drop, the best-case output voltage is expected to be $23.1 V - 7*0.4 V = 20.3 V$, an increase of 2.1V or over 10%.

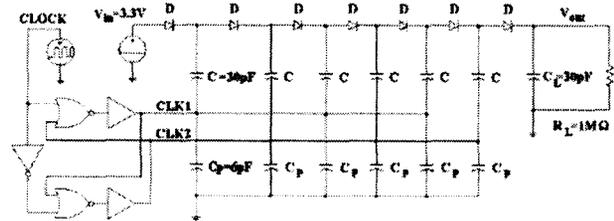


Fig. 4. Six-stage charge pump with non-overlapping clock generator.

Dickson charge pump circuits are typically designed to operate at a fixed switching frequency with a rated output load current and voltage. For a charge pump circuit with a given stage capacitance, switch resistance, load current, and output voltage, there exists an optimal value for the switching frequency that will provide the maximum power efficiency.

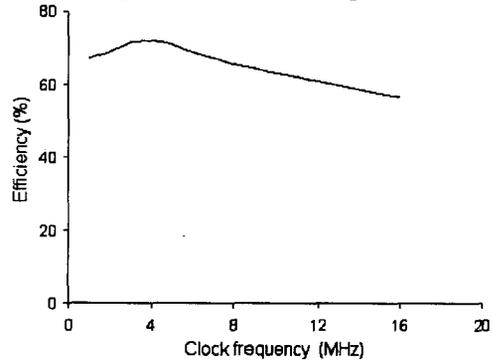


Fig. 5. Optimization plot of converter efficiency versus clock frequency.

The power loss in the Dickson charge pump circuit is composed of two parts; one is the resistive power loss (also called conduction power loss) and the other is the dynamic power loss (also called switching loss). The resistive power loss (or I^2R loss) occurs when the switch is on, and the dynamic power loss occurs because not all of the charge accumulated on the stage capacitors is transferred to the next stage. Some of this charge is transferred to the parasitics of the MOS body-diode switches and the bottom-plate capacitance of the stage capacitors. There are two circuit parameters that aid in controlling the efficiency when designing the charge pump circuit that must be optimized: the switching frequency and the on-state conductance of the body diode. The switching frequency is controlled by selection of the clock frequency, and the on-state resistance is controlled by the selection of the CTS. Utilizing the SOI MOSFET body diode reduces on-state losses, but care has to be taken not to make the devices too large because of increased parasitic capacitance.

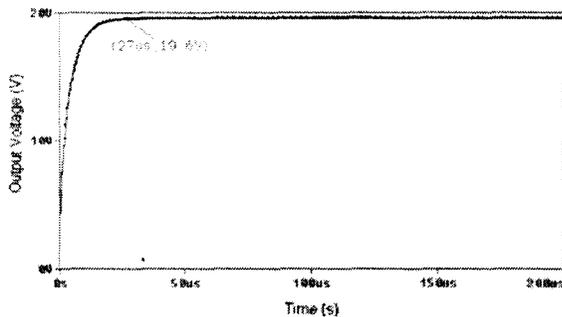


Fig. 6. Simulated output voltage after start-up for a 1 MΩ load.

From the above discussion, it is apparent that there exists an optimal value for switching the transistors so that the power loss is minimum, i.e., the efficiency is at a maximum. The simulation results in Fig. 5 show that at first, when the clock frequency increases, the efficiency increases. This occurs until the clock frequency reaches about 4 MHz. When the clock frequency is increased further, the efficiency goes down due to increased switching losses. Therefore, the optimum operating clock frequency is about 4 MHz for the given switch size and capacitor values.

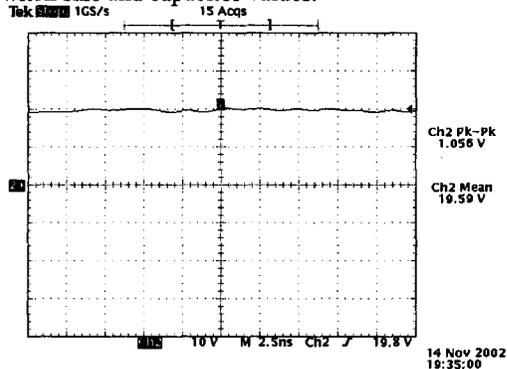


Fig. 7. Measured output voltage for a 1 MΩ load.

Simulation results of the improved charge pump circuit are shown in Fig. 6. The circuit produces 19.6 V with a 1 MΩ load at steady state. It can be seen that the output voltage at steady state is about 19.6 V. The circuit needs about 27 μs to reach steady state. Fig. 7 shows the same result (19.6 V) for the measured case.

With V_{in} at 3.3 V, a 4 MHz clock frequency and a 1 MΩ load, the circuit provides 19.6 V at the output. The output voltage ripple is 1.056 V. The efficiency is calculated using the conventional definition of the output power divided by the input power. With a 1 MΩ load, the improved charge pump has a power efficiency of 72%. Note that all capacitors are implemented on-chip.

VI. Conclusion

In this work, a six-stage Dickson charge pump was designed utilizing the body-diode of SOI NMOS transistors fabricated in a 0.35 μm CMOS process. Utilizing the body-

diode of the NMOS significantly reduced the voltage drop across the switch. A diode model was developed to simulate the behavioral characteristics of NMOS body-diode. This diode was placed in a subcircuit and the BSIM3 diodes effectively removed by proper parameter settings. The advantages of the SOI process allowed for a high pumping gain and output voltage. Using a two-phase non-overlapping clock switched at 4 MHz and an input voltage of 3.3 V, the six-stage charge pump was able to achieve an output voltage of 19.6 V with a load of 1 MΩ. The improved Dickson charge pump efficiency was 72%. Future work will involve investigations into other charge pump topologies in SOI to enhance efficiency and produce voltages in the 30 – 60 V range for MEMS applications.

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