High voltage bandgap reference design using SOI Technology

Vinesh Sukumar, Seeni Subramaniam, Pang Don, Kevin Buck, Herbert Hess, Harry W. Li, Dave Cox, **M.M.Mojarradi
Microelectronics Research and Communications Institute, University of Idaho, Moscow, Idaho, U.S.A.

**Jet Propulsion Laboratory, California Institute of Technology, Pasadena, California, U.S.A.

Abstract—A high voltage bandgap reference circuit has been designed and implemented in an SOI CMOS technology. The design is capable of maintaining a stable value, in the temperature range from 0°C to 100°C. The design is also validated against process and power supply fluctuations. An innovative approach replaces the traditional lateral pnp transistor method.

I. INTRODUCTION

Microelectronics employing Silicon-on-Insulator technology has been widely regarded as an industrial success story of the twentieth century. This has given rise to Metal-Oxide-Semiconductor devices which have shown superior characteristics in extreme environmental conditions and high-density applications. Currently, the need for precision performance in many optical and communication interface devices has given growth to Microwave Silicon-on-Insulator (SOI) technology. National Aeronautics and Space Administration (NASA), is interested in developing system-on-a-chip (SOAC) solutions for future flight missions. Developing analog and mixed signal circuits is part of the SOAC design effort using this emerging technology.

High voltage reference circuits can be found in many applications in mixed signal circuit design, wherever a stable and precise voltage reference is needed. They have the promise of being used in embedded power generation and storage circuit design. These devices must be capable of long-term reliable operation at high temperatures and power supply fluctuations. Conventional bandgap reference circuits use lateral bipolar pnp transistors. Previous design efforts in a CMOS SOI 0.8µm process conducted at the Microelectronics Research and Communications Institute (MRCI), University of Idaho, have also concentrated on using the lateral bipolar pnp transistor. It has been found from a fabrication test result conducted in the CMOS SOI 0.8µm process that lateral bipolar pnp transistors produce poor temperature coefficients [1]. Further, it is very difficult to fabricate bipolar transistors with good electrical characteristics as the silicon film becomes thinner [1]. Thus, new alternatives were being encouraged for a viable bandgap reference circuit on any SOI process. This paper describes the design of a Bandgap Reference Circuit, using SOI technology, replacing the traditional lateral pnp transistor approach.

II. PROPOSED BANDGAP REFERENCE CIRCUIT

In general, bandgap voltage reference circuits combine the positive temperature coefficient of the thermal voltage with the negative temperature coefficient of the diode forward voltage. This helps in achieving a voltage reference with a zero temperature coefficient. The principle is depicted in Figure 1.

![Figure 1 General principle of a bandgap reference [2.]](image)

The motivation for a high voltage bandgap reference in a 0.5 µm SOI process came when a method failed for a fabricating p-channel high voltage transistors. The ease of symmetrical biasing schemes could no longer be employed in this technology. And, it would not be efficient to simply design using the usual cascoding method: long strings of p-channel low voltage transistors would have been needed to take the place of a single high voltage p-channel transistor. This is important so that the drain-to-source voltage is maintained well below the breakdown voltage.

Thus, a new method was developed to mitigate the absence of a high voltage p-channel transistor for the biasing branch. Figure 2 shows the circuit diagram with the additional new biasing branch arrangement used to achieve this purpose. Using conventional low voltage reference design approach, the circuit could have been designed using only three
branches, namely branches 2, 3, and 4. This approach works only if low voltage n-channel and p-channel transistors were used to design the reference. But this approach fails when the designer utilizes a high voltage n-channel transistor to drop a large voltage across its drain-to-source junction in branch 3. This happens because of insufficient biasing for the cascoded low voltage p-channel transistors in branch 2. The p-channel transistors in branch 3 that make up the current source can be kept at a minimum count [1].

So, a new branch is proposed to bias branch 2 appropriately. The new branch creates the biasing structure to drop the source-to-drain voltages across the p-channel transistors in branch 2.

All transistors are sized and biased such that the drain to source voltage will not exceed a 20V breakdown voltage requirement. The devices are sized such that short-channel effects can be safely ignored. All lengths of the devices are in the order of 11 to 14 times larger than the minimum gate length permitted for a 0.35 μm process. Also, the body diodes in branches 3 and 4 are denoted with $K = 5$, meaning there are $K$ body diodes in parallel even though only one is shown, in order to make the circuit diagram less cumbersome. The high voltage n-channel transistor has a breakdown voltage of approximately between 24 V and 27 V.

The specification of the design are shown in Table 1.

<table>
<thead>
<tr>
<th>TABLE I</th>
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<tbody>
<tr>
<td>Operating Temperature</td>
</tr>
<tr>
<td>Supply Voltage Range</td>
</tr>
<tr>
<td>Output Voltage at Room Temperature</td>
</tr>
<tr>
<td>Supply Current</td>
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<tr>
<td>Temperature Dependence</td>
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<tr>
<td>Maximum Deviation of $V_{ref}$ with process fluctuations</td>
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III. HIGH VOLTAGE MOS STRUCTURE

Figure 4 gives a cross sectional overview of the High Voltage Microwave SOI MOSFET. This device is designed to have higher drain to source and drain to gate voltage. This is achieved by placing a lower doped drift region between the drain and the gate. Although this approach increases the on-resistance of the transistor, the voltage tolerance of the device increases by two to eight times the rated process voltage in sub-micron fabrication process. The gate overlap of the drift region and the length of the lightly doped drift region can affect the breakdown voltage and lifetime characteristics of the device. If the drift region is too long there may not be enough carriers that reach the channel region of the transistor. If the gate-overlap is too short the breakdown voltage of the transistor decreases.
IV. TEMPERATURE INDEPENDENT CIRCUIT DESIGN

The design to create a stable voltage reference starts with the usage of simple KVL technique. From previous section, it is known that the cascade-biasing scheme forces the same amount of current through the diodes in branches 2 and 3, $I_1$ and $I_2$, respectively. First, we derive voltage equations to define the diode forward voltage drop seen in branch 3.

In this configuration, the voltage across diode D1, $V_{s1}$, must be equal to the combined voltage across D2 and $R_1$.

$$V_{s1} = I_1 R_1 + V_{s2}$$  \hspace{1cm} (1)

From the fundamental diode equation, we have

$$I_1 = I_s e^{V_{s1}/nV_T}$$  \hspace{1cm} (2)

(2) can also be shown as,

$$V_{s1} = nV_T \ln \left( \frac{I_1}{I_s} \right)$$  \hspace{1cm} (3)

Where $I_s$ is the reverse saturation current of the diode, $n$ is the grading coefficient, and $V_T$ is the thermal voltage, approximately 26 mV at room temperature. In a similar fashion to (3), we can also derive another equation to define the diode voltage of D2, which consists of $K$ body diodes in parallel

$$I_2 = K \cdot I_s e^{V_{s2}/nV_T} \Rightarrow V_{s2} = nV_T \ln \left( \frac{I_2}{K \cdot I_s} \right)$$  \hspace{1cm} (4)

Now, using equations 1, 2, 3, and 4, we can solve for the resistance, $R_1$,

$$R_1 = \frac{nV_T \cdot \ln K}{I_1}$$  \hspace{1cm} (5a)

Substituting the values would give.

$$R_1 = 40 \Omega$$  \hspace{1cm} (5b)

The reference voltage in the output branch 4 is,

$$V_{REF} = I_3 \cdot L \cdot R_1 + V_{s3}$$  \hspace{1cm} (6)

In (6), the term $L \cdot R_1$, must be equivalent to $R_2$. A term having all the desired variables for temperature tolerant design can be found by substituting (5) into (6), and deriving,

$$V_{REF} = (L \cdot n \cdot V_T) \ln K + V_{s3}$$  \hspace{1cm} (7)

The temperature coefficient of the thermal voltage is $+0.085$ mV/°C. The temperature coefficient of the diode forward voltage drop is approximately $-2.2$ mV/°C.

Now, $V_{REF}$ can be defined with respect to temperature changes,

$$\frac{\partial V_{REF}}{\partial T} = L \cdot n \cdot V_T \ln K \left( \frac{\partial V_T}{\partial T} + \frac{\partial V_{s3}}{\partial T} \right)$$  \hspace{1cm} (8)

Solving (8) set to zero, the value of L was found to be approximately 6. The term K was fixed at a value of 5. The grading coefficient, $n$, is approximately 2.6. The values were derived after numerous iterations to get the best practical numbers for layout considerations.

Substituting the values of L, n, K in (7) gives

$$R_2 = 242 \Omega$$

$V_{REF} = 1.22V$ (approximately)

The next section shows the SPICE simulation results of this design.

IV. SPICE SIMULATION RESULTS

Figure 5 below shows the dc SPICE simulation result of the reference voltage with respect to temperature variation. $V_{REF}$ was found to be approximately 1.23 V. Simulations using the typical model for transistors show only a $0.74\%$ variation between 0 °C and 100 °C.

![Figure 5 Reference voltage behavior with temperature.](image)

Typical, best and worst case SPICE models are also used to test the validity of the design (Figure 6). The results show a 20% variation from the design value of 1.2V. These models have incorporated changes in threshold voltages of the transistors that are extracted from the test data.

It is also desirable to know how the reference voltage is affected by changes in power supply voltages. Figure 7 shows how the reference voltage behaves for a wide sweep in the power supply, VDD. The desired reference voltage reaches for supply voltage equaling 12V. The reference shows a fluctuation of less than 1% for VDD reaching between 12V and 25V.
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VII. ACKNOWLEDGEMENTS

A test chip is being fabricated in a 0.35μm Microwave Silicon-on-Insulator process as seen in Figure 8. Test results for the design will be presented as part of another paper.

VI. CONCLUSIONS

An innovative High Voltage Bandgap Reference circuit is presented. A novel approach eliminating the traditional lateral pnp model is proposed. This design also exhibits a low current consumption. An appropriate reference voltage behavior with respect to temperature, process variations, and power supply fluctuations is achieved. The proposed bandgap reference could be key technology for high voltage CMOS design.

REFERENCES

