

FLUX - Revolutionary Circuit Technology for High End Computing

A. Silver, A. Kleinsasser
Jet Propulsion Laboratory
silverrp@vaxeb.jpl.nasa.gov
kleins@vaxeb.jpl.nasa.gov

L. Abelson, P. Bunyk, Q. Herr, G. Kerber
Northrop Grumman Space Technology
lynn.abelson@ngc.com, paul.bunyk@ngc.com
quentin.herr@ngc.com, keorge.kerber@ngc.com

M. Dorojevets
SUNY-Stony Brook
midor@ece.sunysb.edu

Abstract

Scaling CMOS to higher performance for high end computing requires limiting prime power and improving computing efficiency. In space, rad-hard parts are required. Superconductor single-flux-quantum (SFQ) circuitry is an attractive solution. We project 50 K gates/chip operating with 100 GHz clock while dissipating only ~5 mW. Total power per chip, including cooling to 5 K, is ~2.5 W. SFQ processor chips will be more efficient than CMOS. In addition, > 99 % of the power is unregulated. Extremely low supply voltage, as low as 2 μ V/GHz, enables the ultra-low power of SFQ circuits. A 100 GHz clock requires only 200 μ V. FLUX is a technology development program to validate SFQ technology for high end computing: LSI fabrication, chip architecture, design methodologies, 50 Gb/s inter-chip communication, and packaging. We discuss the status and limitations of FLUX, and future plans for SFQ processors for a petaFLOPS machine. The baseline Hybrid Technology, Multi-Threaded design uses 4096 SFQ processors operating at 50-100 GHz to achieve 10^{15} FLOPS. Total SFQ processor power is ~250 kW.

1. Motivation

High end computing at sustained petaFLOPS level and beyond remains an elusive goal, despite significant advances in semiconductor technologies. The Department of Energy ASCI program has acquired teraFLOPS class machines to help manage the nuclear stockpile and NEC has developed the Earth Simulator (ES) supercomputer [1]. These computers have large footprints and require megawatt power levels. ASCI White requires 12 MW [1]. Even so, MPP machines cannot sustain more than a fraction of peak performance. Scaling COTS-based machines to petaFLOPS suggests $\sim 10^5$ of processors with immense switching networks and very high power systems. The PVP NEC Earth Simulator has a very large footprint and requires very high power levels. The computer system has a 50 m by 60 m footprint on three floors, plus a dedicated power plant. ES has 5120 processors with 40 TFLOPS, peak. The processors dissipate 170 W each, and a total power of

7 MW [1]. There is a critical need for new hardware technologies as well as new architectural approaches to achieve these performance levels at acceptable power. The Hybrid Technology, Multi-Threaded (HTMT) architecture study [2] identified advanced hardware and architecture approaches that can leapfrog conventional incremental advances. We present here a revolutionary processor hardware approach for high end computing – superconductor single-flux-quantum (SFQ) LSI logic.

1.1 Efficiency

Total power is a critical factor for both ground- and space-based computing. State-of-the-art supercomputers require large footprints and megawatts of power, limiting siting opportunities. One can anticipate that this situation will get progressively worse as we move to the next level.

Low-power semiconductor logic operates with volt-level power bus. Superconductor logic, based on the switching characteristics of Josephson junctions, works at millivolt-levels. Operating at cryogenic temperatures, SFQ gates require ~ 75 times lower energy per switching event than room temperature circuitry to be stable against thermal noise. Since the on-chip power dissipation of each SFQ device is so much smaller than semiconductors, one can place SFQ devices and chips very close and still allow removal of the heat dissipated at maximum speed. This proximity also improves computing efficiency as discussed below.

The HTMT baseline design [2] assumes 4,096 superconductor processors that will be conductively cooled by a single closed-cycle cryocooler. Refrigeration systems to cool large superconductor computing engines to 5 K are readily available. For systems of this scale, it presently requires ~ 400 W to cool 1 W at 5 K.

Although semiconductor transistor delays have been demonstrated on picosecond scales, circuits operate at much lower speeds. However, SFQ gates perform logic and transmit data between densely packed gates with minimal power at rates approaching 100 GHz. We consider a figure of merit for the maximum performance

as $FLOPS = 6NF_c$, where high throughput requires simultaneously maximizing the number of active gates per clock cycle (N) and the clock frequency (F_c) measured in MHz. Although SFQ LSI cannot challenge the gate density of CMOS, it can achieve much higher clock rates and increase the number of gates per cycle substantially beyond the recent SFQ state-of-the-art. Higher speed SFQ circuitry is achieved without employing deep sub-micron lithography, although such tools are available if required. Consider the following comparison. Both a 2 Mgate CMOS chip at 1 GHz and a 20 Kgate SFQ chip at 100 GHz will be capable of 12 GFLOPS. The CMOS chip will dissipate 80 W and thus requires cooling to maintain operational speed, while the SFQ chip dissipates only 2 mW. Including cooling at 400 W/W, the SFQ chip requires only 0.8 W of unregulated power at room temperature.

SFQ technology enables on-chip data transmission at the clock frequency via superconducting thin film stripline and microstripline. These thin film transmission lines have low loss and low dispersion and can be placed as close as lithography permits with negligible cross-talk. In addition, Herr, et al. have demonstrated 50 Gb/s inter-chip data transmission through MCM substrates using matched striplines [3,4].

1.2 Application in space – radiation-hardness

High performance space-borne computing enables autonomous missions and consequently reduces the required communication bandwidth for uplink/downlink operations. A unique requirement for space applications is radiation hardness. As semiconductor technology reduces power, it also degrades radiation resistance, necessitating redundancy. Superconductor circuitry is based on metallic niobium (Nb) and niobium nitride (NbN) Josephson junctions that are intrinsically rad hard. Because SFQ LSI circuits are constructed with metallic films above superconducting ground planes, the substrates serve only to mechanically support the circuitry. In addition, the very low impedance of SFQ devices (1 to 100 Ω) makes charge buildup unlikely and unimportant. A major issue in space is the weight and power of cryocoolers. There are now several options available for long-life space cryocoolers. For some deep space missions, portions of the spacecraft could be "close" to the required temperature for SFQ circuits and so would require minimal additional cooling, compared with CMOS, which requires heating to function. NbN can operate at 10 K, making it a good fit for space cryocoolers [5].

1.3 Background

Here we describe SFQ LSI technology in sufficient detail to illuminate its advantages for high end computing. SFQ circuitry is based on the unique physical properties of superconducting materials at temperatures below their critical transition temperature, T_c , unique features of electron tunneling between superconductors, and innovative circuit implementations.

- The static electric field vanishes inside a superconductor; consequently, the dc electrical resistance is zero. "Paired" conduction electrons, called Cooper pairs, carry the current that flows with no voltage, called a supercurrent.
- Not just a perfect conductor, a superconductor is also perfectly diamagnetic. Thus, superconducting ground planes are perfect shields between wiring layers.
- Electric currents and magnetic fields only penetrate superconductors to a shallow, frequency-independent depth. This improves the ability of superconducting thin film microwave transmission lines to transmit high data rate signals.
- Superconductors behave as coherent macroscopic quantum objects. Magnetic flux in multiply-connected superconductors, such as rings, is quantized in units of the flux quantum, $\Phi_0 = h/2e = 2.07$ mV-ps.
- Superconductors exhibit a unique "kinetic" inductance associated with supercurrent flow within the penetration depth.
- For single electrons, superconductors have a very small energy gap, typically millivolts, compared with volts for semiconductors. The small energy gap voltage, V_g , ultimately leads to very low power devices.
- Electrons and electron-pairs can "tunnel" between superconductors separated by a thin insulating barrier. Electron tunneling conductance is small and extremely nonlinear below V_g . Pair or Josephson tunneling carries a supercurrent below a maximum value, referred to as the critical current, I_c .
- Superconductors have very low rf surface resistance. This surface resistance increases as f^2 from zero at dc, compared with $f^{0.5}$ for normal conductors. Above a frequency $f = 2eV_g/h$, superconductors behave as normal conductors. This frequency is ~ 700 GHz for Nb.
- Cryogenic temperature operation offers greater stability, virtually eliminates thermally activated degradation and failure mechanisms, and produces very low thermal noise, thereby enabling higher sensitivity detectors and wider bandwidth for analog and digital applications than semiconductors, and enables lower power circuitry.

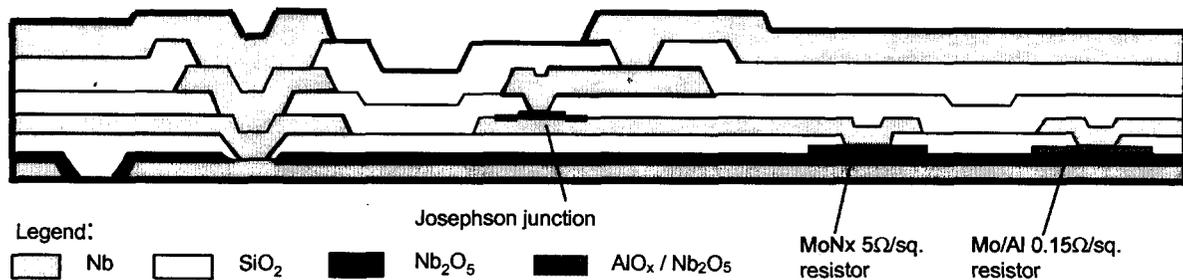


Figure 1. Cross-section of Nb LSI chip

We are interested here in metallic superconductors Nb and NbN, which have T_c of 9.2 K and 16 K, respectively.

2. Recent advances in SFQ technology

SFQ LSI represents a significant improvement [6,7] over previous superconductor logic families employed by IBM [8] and the MITI program in Japan [9]. Those earlier programs were based on voltage-latching gates that dissipated more power and were limited to several GHz. In addition, latching logic required multi-phase rf power systems while SFQ logic uses only dc power.

SFQ circuit design has now reached a new level of maturity. Recent demonstrations include chip-to-chip communication at up to 60 Gbps [3], series biasing of circuit blocks to reduce power supply current [11], and place-and-route design methodology using passive transmission line interconnect [12].

SFQ circuits are implemented in thin film LSI formats similar to semiconductor LSI. The principal differences are the materials and dimensions required to achieve equivalent speeds. SFQ LSI requires only deposition and etching of metal and dielectric films, fabricated completely on top of supporting substrates that have no electrical function. Silicon wafers are typically used

because of their low cost, availability, and compatibility with processing tools. Most of these tools are similar, or identical, to those used in semiconductor foundries. SFQ foundries typically use lithographic tools one or more generations behind commercial CMOS foundries. Today's SFQ LSI is at 1- μ m feature size [13].

The FLUX project uses the Northrop Grumman Space Technology (formerly TRW Space & Electronics) foundry. Figure 1 shows a typical cross-section profile. The foundry capability and roadmap are shown in Table I [13]. Since inception of the FLUX project in Feb. 2000, the foundry has advanced two complete generations as shown in the table.

SFQ circuits operate by the creation, elimination, and propagation of single magnetic flux quanta (Φ_0) in small monolithic thin film inductive loops (a few picohenries) containing Josephson tunnel junctions. Josephson junctions can switch and perform logic functions in a few picoseconds. Bits are stored as a persistent supercurrent in the inductor, at zero voltage. Bits propagate from one gate to the next as picosecond SFQ pulses, not voltage levels. Data propagates beyond the adjacent gate using matched stripline.

We design SFQ LSI circuits using stable design rules [14] and commercial CAD tools adapted for SFQ

Table I Foundry Capability and Roadmap

	1998	2000	Now	+ 2 yrs	+ 4 yrs	1992 CMOS
Minimum feature size (μ m)	1.5	1.0	1.0	1.0	0.75	0.5
Minimum junction size (μ m)	2.5	1.75	1.25	1.00	0.75	NA
J_c (kA/cm ²)	2	4	8	12	20	NA
Number of masks	12	12	14	14-18	18	~20
Number of resistor types	2	2	2	2	2	NA
Metal line pitch (μ m)	4	3	2.5	2.4	2	1.2
No. of metal wiring layers	4	4	4	4 - 6	6	3
Planarization	No	No	Partial	Yes	Yes	Yes
Pin count	128	128	128	640	1200	500
F_{max} (GHz) Divide by 2	150	210	300	370	475	1
Processor clock (GHz)	30	40	60	80	100	0.2
Gate density (Kgates/cm ²)	5	8	16	32 - 64	128	300

circuits. The methodology has advanced to include electrical simulations using WR-Spice™, topological design using Cadence™ layout tools, automated error-checking against fixed design rules, layout versus schematic checking, and VHDL. P-cells and gate libraries speed design and reduce errors.

The foundry capability has profound implications for the expected performance of SFQ chips: gate density and speed. First among the process characteristics is the conductance of the junctions, measured by their supercurrent density, j_c . In SFQ circuits, the minimum I_c is $\sim 100\mu\text{A}$, fixed by the operating temperature. Maintaining this current as j_c increases requires shrinking the junction. Since junctions are one of the smallest features, the minimum linear dimension must be reduced as $j_c^{-0.5}$. Intrinsic speed increases as $j_c^{0.5}$, because the supercurrent is shunted by the junction capacitance. Equally important is the fact that the junction impedance, hence the circuit impedance, increases as fast as the speed. Raising the impedance enables narrower transmission lines, increasing circuit density. Second, density depends on the available number of wiring levels [15]. NGST processes available at present have four superconducting metal levels, including the ground plane. Incorporating more levels will require planarization, which is being explored for future improvement.

3. SFQ processors in HTMT architecture

The HTMT Phase II project was a multi-investigator project that defined architecture, processor hierarchy, memory hierarchy, networking, and software for a petaFLOPS computer. K. Likharev of SUNY-Stony Brook was the principal investigator for the SFQ technology and processor definition phase that preceded FLUX. The baseline design for HTMT included 4096 SFQ processors (SPELL) connected to 4096 DRAM-PIM processors [16]. Each SFQ processor is supported by adjacent cryogenic RAM (CRAM) and interconnected by a cryogenic network (CNET). The COOL instruction set [17] and the SPELL-1 multi-threaded processor micro-architecture were developed by M. Dorojevets of SUNY-Stony Brook.

From this study, design requirements for the SFQ LSI were developed. These requirements exceeded the available SFQ state-of-the-art in both complexity and speed. It was recognized that a technology development project was required if SFQ LSI chips were to be available for HTMT.

4. FLUX project

4.1 FLUX plan and goals

FLUX is the SFQ technology development vehicle within the HTMT program. The goal is to validate the proposition that SFQ LSI logic can be developed to at least 50 K gates/chip operating at 50 - 100 GHz clock rates and interconnected on multi-chip modules. FLUX is a series of demonstrations leading to an SFQ processor of LSI SFQ logic chips operating at clock rates approximately 30 GHz interconnected for serial data transmission at the clock frequency on multi-chip modules. FLUX is a multi-organization project between JPL (management), NGST (formerly TRW) in Redondo Beach, CA (foundry, design, integration, and test), and SUNY-Stony Brook (architecture and gate-level design). Each successive demonstration is expected to be more complex, operate at higher speed, and use a more advanced foundry process and design tools.

FLUX-1 is an 8-bit single-chip microprocessor designed to operate at 20 GHz. It was initiated in Feb. 2000 using TRW's then new 4 kA/cm² LSI process. In addition to the 8-bit μP , the chip includes scan path test circuitry.

FLUX-2 is a 32-bit multi-chip floating-point multiplier with vector register memory operating at 25 GHz. It will use NGST's latest 8 A/cm² LSI process. FLUX-2 also will include scan path circuitry for testability.

FLUX-3 is a special purpose processor, designated SuperPro. We expect it to be the last phase before constructing a multi-processor high performance computer prototype.

4.2 FLUX status

We are completing FLUX-1 and starting design of FLUX-2. FLUX-1 was the first use of TRW's new 4 kA/cm² foundry process. (Before FLUX-1, circuits were fabricated in a well-established 2-kA/cm² process.) Dorojevets developed the FLUX-1 architecture and processor organization [18,19]. Likharev's team at SUNY began an initial FLUX-1 chip design; the design was later revised and implemented at TRW [20,21]. Figure 2 is a photograph of the final FLUX-1 chip that is being tested at NGST. It is 10.3 mm wide by 10.6 mm high and contains the equivalent of 5K gates. We have demonstrated serial data transfer rates as high as 60 Gb/s on-chip and between chips on a substrate using an innovative flux quantum pulses propagated through impedance matched thin film transmission lines.

FLUX-2 is in the early design stage. The project has been defined as a 32-bit floating-point multiplier connected to a 4-kbit vector register memory as shown in Figure 3. The FPU is expected to be on two chips, the VR memory on one chip. These three chips will be mounted on a single MCM and interconnected word-wide at the 25 GHz clock rate. The vector register

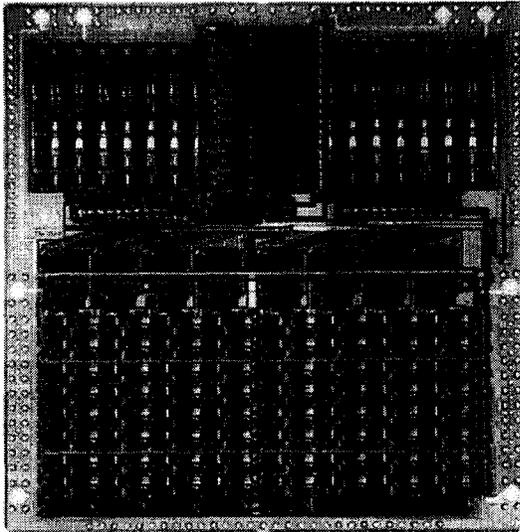


Figure 2. Photograph of FLUX-1 chip (Rev 2)

implementation employs FIFO shift registers. It has been demonstrated [22].

The SFQ gate library has been translated from the 4 kA/cm^2 to the 8 kA/cm^2 process. Options for the FPU architecture have been identified [23]. VHDL design tools have been put in place and exercised for the first time.

4.4 Major hurdles

Significant engineering hurdles in SFQ and supporting technologies remain before production of the prototype computer. These include

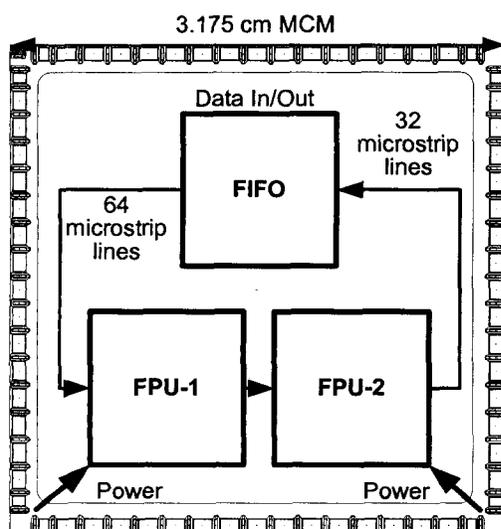


Figure 3 Block diagram of FLUX-2

- SFQ foundry improvement,
- reduction of SFQ chip power and supply current,
- availability of improved MCM substrates,
- wideband and low thermal conductance input/output technology,
- wideband cryogenic network,
- cryogenic RAM, and
- wideband 3-d packaging.

The foundry needs to supply low defect density chips junctions with:

- j_c at least 20 kA/cm^2 ,
- $0.8 \mu\text{m}$ minimum feature size,
- I_c uniformity $< 2\%$ (1σ),
- at least 3 more metal layers
- $1 \mu\text{m}$ metal line pitch,
- at least 64-kbit CRAM chips with 0.1 ns access, and
- cryogenic network switches capable of operating at 50 GHz clock with sufficient bandwidth to support the processors.

Chip power needs to be reduced an order-of-magnitude, closer to the theoretical limit of $05. \text{ nW/gate/GHz}$ [24]. Simultaneously, we need to reduce the supply current to each chip by recycling the current. NGST has demonstrated two methods for achieving current recycling, but not yet on large circuit blocks operating at high clock rates [25].

The MCMs used on FLUX are Nb wiring on Si substrates. FLUX-1 used 2 Nb levels; FLUX-2 will use 3 Nb levels. At least 7 wiring levels are required for high data rate transmission, plus power and clock, and we are seeking a commercial source based on standard ceramic or glass substrates with 7 added high conductivity, thin film layers.

The DoD Crossbar switch project, also an element of the HTMT program, is developing a 2-10 GHz cryogenic switch between semiconductor parallel processors and memory [xbar]. We need a cryogenic network switch between SFQ processors and CRAM that supplies at least 10 Gb/s serial data rate. Electrical, optical, and hybrid interconnects are being explored. Crossbar has demonstrated wideband, thermally efficient ribbon cable at several GHz.

There are no demonstrated solutions for 0.1 ns access, 64-kbit CRAM chips. VanDuzer is demonstrating a hybrid CMOS-superconductor memory that operates at 5 K . It uses high density CMOS RAM and fast, low power superconductor sense and output buffer. NEC demonstrated an SFQ RAM concept, and others have been proposed, but no demonstration has been made that approaches the scale required.

Low latency is required in order to achieve computing efficiency. One aspect of latency is time-of-flight (TOF) between processors and between processors and memory. At high clock rates, latency as measured by

clock cycles increases for a given physical configuration. We need compact 3-d packaging to minimize time-of-flight latency, and to improve cryogenic efficiency.

5. Summary

We have presented the status of FLUX, the technology development vehicle for SFQ circuit technology for high end computing. This is an attractive option for high performance computing because it is low power (particularly at the chip level), clock rates can be anticipated at 50-100 GHz, chips can be packaged compactly, and inter-chip communications can be at 50 Gb/s serial data rate. FLUX is a multi-phase project that leads to a prototype machine. Significant progress has been made. Major engineering hurdles remain, but they are not judged to be insurmountable.

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