Technology Readiness Overview: **March 2003**

Low-k interlevel dielectrics technology

Mihail P. Petkov, NASA Electronic Parts and Packaging, Jet Propulsion Laboratory

Brief description of low-k technology

Semiconductor manufacturers have been shrinking transistor size in integrated circuits (IC) to improve chip performance. This has resulted in increased speed and device density, both of which were described well by what is known as Moore's Law – chip performance will double every ~18 months. The speed of an electrical signal in an IC is governed by two components – the switching time of an individual transistor, known as transistor gate delay, and the signal propagation time between transistors, known as RC delay (R is metal wire resistance, C is interlevel dielectric capacitance):

$$RC\,delay = 2\rho\varepsilon\left(4L^2/P^2 + L^2/T^2\right),$$

where: ρ is metal resistivity, ε – permittivity of the interlevel dielectric (ILD) (ε is referred to as k in this field), L – line length, P – metal pitch, T – metal thickness.

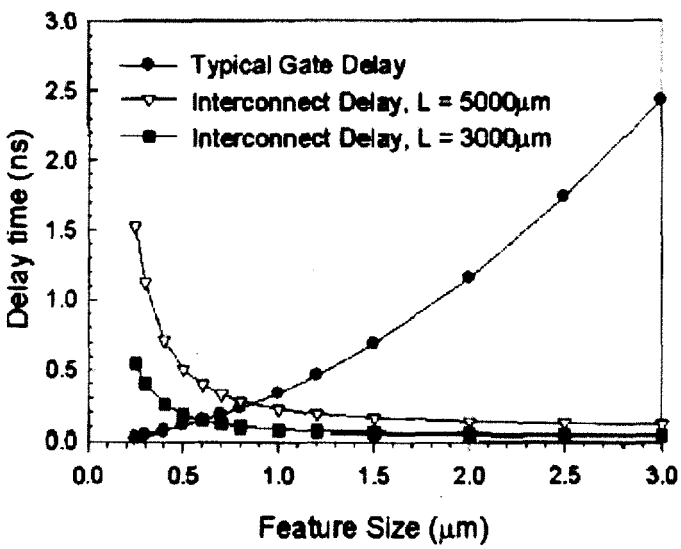


Figure 1. Comparison of intrinsic gate delay and interconnect (RC) delay as a function of feature size. In sub-micron technologies, the interconnect delay becomes the dominant factor as shown in the plot.

Moore's Law existed only because the RC delay was negligible in comparison with the signal propagation delay (Figure 1). For sub-micron technology, however, this no longer holds; the RC delay becomes the dominant factor.

To facilitate further improvements, semiconductor IC manufacturers are forced to resort to new materials with no

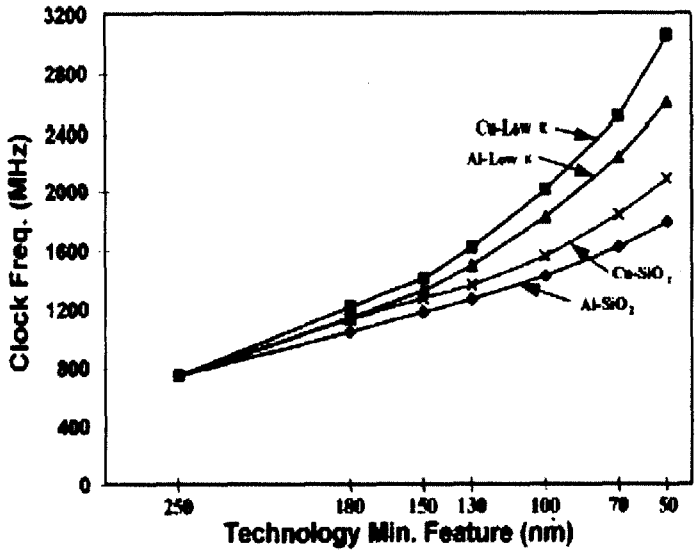
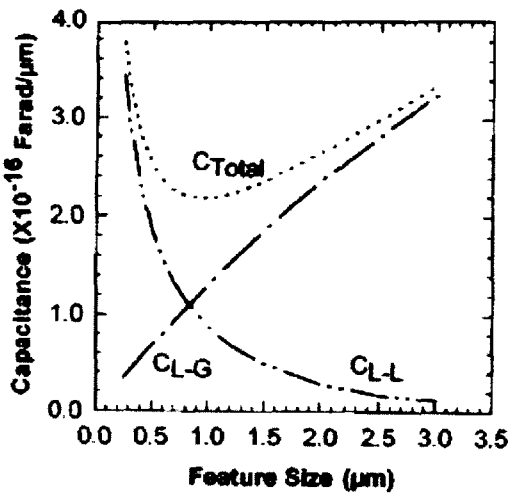


Figure 2. Microprocessor clock speed for different metals and dielectrics as a function of feature size

prior use in chip production. These new materials are utilized to reduce the RC delay by either lowering the interconnect wire resistance, or by reducing the capacitance of the ILD. The first "quick fix" adopted by the industry was to lower the dielectric constant of SiO_2 from $k = 3.9$ to $k \sim 3.5$ by doping it with fluorine (thus producing fluorinated silica glass, or FSG), which resulted in modest gains. A significant improvement was achieved by replacing the Al interconnects with Cu, which has ~30% lower resistivity than that of Al. The Cu / FSG technology is capable of supporting the current device technology to the 130 nm generation. Since no other metal can offer notable gains, Cu will remain the choice for interconnects. Therefore, further advances can only be facilitated by the change of the low-k ILD (Figure 2).

The use of low-k dielectrics is also necessitated by the increased proximity of interconnect lines with the shrinkage of feature size, which leads to enhanced "cross-talk" between lines. Figure 3 shows the dependence of line-to-line capacitance, $C_{L\text{-}L}$, and line-to-ground capacitance, $C_{L\text{-}G}$, as a function of feature size.



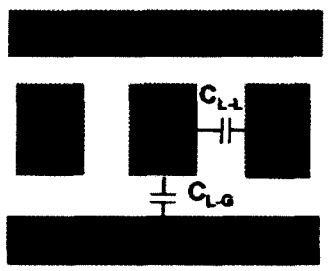


Figure 3. Capacitance components in a simplified structure representative of interconnect wiring: , $C_{L\text{-}L}$ is line-to-line capacitance; $C_{L\text{-}G}$ is line-to-ground capacitance. $C_{L\text{-}L}$ is responsible for the cross-talk.

NASA needs for low-k technology

The combined NASA and military market represents only one hundredth of the entire electronic market. As a consequence of this, NASA faces limited options for use of electronic components – either to absorb the enormous cost of development and production of complex custom-made IC's, or to increase the use of commercial-of-the shelf (COTS) devices. Application-specific IC's (ASICs), whose initial development cost measures in $M, is an indication of the price range should NASA select the former option. The NASA interest in COTS IC's has been highly emphasized in recent years; however, this places the technology selection in the hands of the semiconductor industry.

The IC manufacturers have already defined the semiconductor technology for the future in the International Technology Roadmap for Semiconductors (ITRS), published by International SEMATECH and updated regularly. It is not a question of if, but when and how, the transition to the new materials (low-k ILD, high-k capacitor and gate dielectrics, Cu interconnects) will occur. Low-k technology is already a reality, being implemented in ASICs and microprocessors, and is expanding to FPGAs, DRAMs, etc., and it is only a matter of time before low-k COTS are used in NASA missions.

It is apparent that the low-k technology infusion in NASA projects will face many hurdles. A strong indication for that is that the semiconductor industry has postponed three times the transition to low-k ILDs, another update was made last year, and a new ITRS, which is expected to extend the implementation date once again, will be published in 2003. A consensus expressed at the International SEMATECH Ultra-Low-K Workshop (June 2002) stated that all member companies possess working low-k technology, and its implementation is a business decision. Reliability and yield problems are the major suspects for the implementation delays. Because manufacturer will generally not reveal reliability data, NASA must address not only these concerns, but it must also assess the COTS performance in hostile space environments. For example, most low-k candidates are polymers, which are known to degrade under radiation. In addition, the increased number of materials with different coefficient of expansion in an IC increases the risk of failure in thermal cycling. Also, degraded mechanical strength poses concerns during launch, and poor thermal conductivity may cause overheating.

Technology Readiness Level

Low-k dielectric technology could be classified from the point of view of its readiness for infusion into flight systems according to the technology readiness level (TRL) classification. The low-k technology has been implemented in ASICs (IBM, Fujitsu), and microprocessors with low-k ILD are expected by the third quarter this year (PowerPC by IBM). Other companies have plans to convert to low-k COTS at different times this year. The TRL of the low-k technology is generally at level 5:

TRL 5: System / subsystem / component validation in relevant environment

Thorough testing of prototyping in representative environment. Basic technology elements integrated with reasonably realistic supporting elements. Prototyping implementations conform to target environment and interfaces.

It should be noted that low-k technology has not been proven at thermal conditions outside the commercial range (0-70 °C), and its performance in radiation environments is unknown. ESD performance has been thoroughly tested.

Commercial production and manufacturability issues

Materials with low-k are abundant; however, those capable of integration in the Si microcircuit production process are scarce. For that, the low-k candidate must satisfy not only the electrical requirements, but also sets of thermal, mechanical, and chemical conditions. The integration process proved unexpectedly difficult even for the leading manufacturers. Further complications arose from the fact that there is no "clear winner" among the low-k candidates; rather each company tries to produce the "magic formula". The prolonged search for ideal low-k dielectric and the integration difficulty forced the industry to postpone the implementation of the low-k technology three times (the fourth will probably be announced this year). Compare, for example, the ITRS versions in 1997, 1999, and 2001 (2003 is expected soon).

Semiconductor companies must make a decision when to abandon the FSG dielectric and switch to low-k materials. For high-end devices, the postponement of the

low-k implementation increases the production cost by necessitating two extra metallization layers with Cu / FSG. The major choice however is what low-k production method is more suitable – CVD or spin-on, which differ in how they deposit a thin ILD film (Figure 4). Spin-on drips its polymeric material onto a spinning wafer under normal atmospheric pressure. CVD starts with a gas and precursor molecules, and heats them in a vacuum chamber, where the film forms by thermal deposition of selected ions and radicals. Thereafter, both processes proceed similarly: a photoresist is added, the interconnection pattern is exposed to the wafer, and the resist and low-k film are etched away. Cu is plated onto the film pattern, and the entire wafer is treated to a chemical-mechanical polishing (CMP).

The CVD technology is presently used, which makes it appealing due to the existing wealth of experience. However, the tools ownership cost increases exponentially with downsizing the feature size. Moreover, introduction of sufficient porosity in CVD materials, which is a necessity for <65 nm devices, has not been achieved to date. On the other hand, spin-on low-k tools have a constant price tag for future generations, as porosity is engineered in the spun solution. This, however, is a new, not yet established technology, which has to be integrated into the production lines. Most likely, CVD low-k ILD's will dominate down to the 90 nm generation, after which spin-on ILD's appear to be the obvious choice. Companies, which may opt to select initially CVD and later switch to spin-on ILD, have to absorb the large cost of changing the tools. There is also a notable trend of shifting the process responsibility to tool vendors, which are asked to sell a complete process as opposed to fabrication tools.

These considerations hint at the possibility for enormous gains should a successful product appear, which can redistribute significantly the market shares.

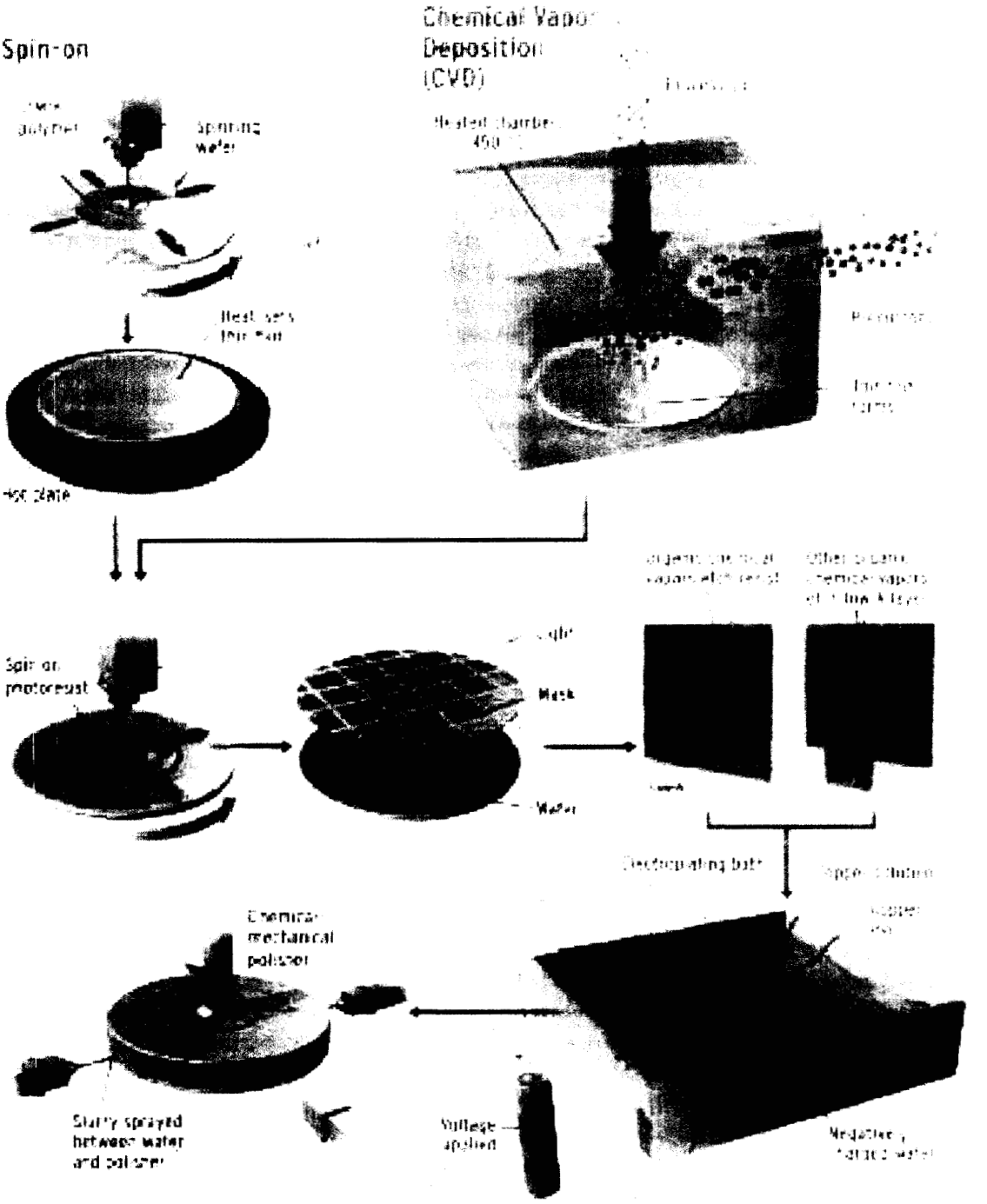


Figure 4. Fabrication process of spin-on and CVD low-k interlevel dielectrics, and the subsequent production stages of Cu interconnect wiring (IEEE Spectrum, Feb. 2003).

Mechanical issues:

The common production problems are associated with the low-k incompatibility with standard processes and conditions. The reduced mechanical strength in comparison with that of FSG poses major concerns during chemical-mechanical polishing (CMP), after the damascene process is complete. The fine abrasive and the slurry cause sufficient stress for the dielectric to break up, Cu lines to come off, a whole layer to delaminate, or connection to devices on the bottom to break. In CVD materials, the weakening agent is the substitute C, which comes in methyl groups, creating more open structure. Spin-on low-k are predominantly polymers, which are naturally weak.

All mechanical properties deteriorate with the incorporation of porosity. This will lead to far more severe problems in the next generation of ultra-low-k ILD's ($k<2.2$). An indication exists that the stresses induced by the plastic package upon cooling can be sufficient to crush a porous ultra-low-k dielectric, which may force changes in packaging technology. Subjected to stress, there is a critical porosity loading at which the fracture mechanism of a porous dielectric changes from delaminating at an interface to internal fracturing. At that porosity the mechanical integrity of a chip is lost.

Thermal issues:

Thermal issues arise from the thermal cycling in a broad temperature region (25°C - 450 °C). The newly introduced materials in a chip have different coefficients of expansion, which leads to the formation of strong local tensile stresses. Furthermore, many materials register gradual structural changes with repeated thermal cycling. Thus, the lowest lying low-k layer, which has been exposed to all thermal cycles (2 per layer; typically 8 layers), may not have the same properties as the top low-k layer, which has been exposed to just 2 cycles. Also, the thermal conductivities of all low-k dielectrics are worse than that of oxide, which impacts the heat exchange and the thermal budget.

Once again, porous ultra-low-k dielectrics have severely deteriorated thermal performance (a power law decrease with porosity), and, consequently, the mechanical properties are also impacted.

Chemical issues:

Some low-k fabrication processes, especially those involving organic ILD's, require the use of materials considered harmful for semiconductors. Compatibility with other existing processes (lithography, CMP, Cu electroplating) is also a concern. For many materials moisture is a corrosive environment!

Porous materials drastically change the chemical performance of the low-k ILD's. The ITRS calls for k = 2.2 (for the 65 nm generation), which requires incorporated porosity of ~20% in all low-k candidates. This value is most likely above the porosity percolation threshold (according to known percolation models), which means that there is a connected path through pores connecting any two regions. At this porosity loading, the low-k ILD acts as a sponge, absorbing process gasses and chemicals, with the risk of expelling them out at another production stage, thereby causing contamination. Moreover, percolated porosity provides a path for Cu ions to diffuse anywhere and metal wires can be shorted.

Considering all of the above, it is not surprising, that the Cu / low-k technology integration was announced in 2000 (Cu-11 technology; IBM), however, the first devices reportedly appeared in 2002.

Material vendors

- CVD low-k dielectrics (130 nm – 90 nm generation):

  Novellus (Coral®), Applied Materials (Black Diamond® with BLOk® barrier layer), IBM (SiCOH).

- Spin-on low-k dielectrics (90 nm and future generations):

  Dow Chemical (SiLK®), JSR (LKD® 5109), ASM International (Aurora®), Honeywell (Nanoglass® and FLARE®), Dow Corning (FOx® and XLK®), Shipley (Zircon®), Schumaker (VELOX-ELK®), Asahi (ALCAP®)

Many of these products are poly-aryls, poly-arylene ethers, or silsesquioxanes (SSQ), such as hidrido- (HSSQ) or methyl-SSQ (MSSQ). MSSQ is hydrophobic, which gives it an edge over HSSQ. The MSSQ is structurally similar to the CVD carbon-doped oxide, but the spin-on process allows for incorporation of porosity on the nanometer scale.

The following materials can be purchased from SEMATECH in the form of blanket wafers, multi-layered structures with oxides and/or barrier layers, and Cu-damascene patterned wafers: SiLK, CORAL, Black Diamond, LKD 5109, and Aurora.

Available device vendors

To this date, high-end devices with low-k dielectrics are produced by IBM (ASICs with Cu-08 technology) and Fujutsu (CS91). Recall that the IBM Cu-11 was initially presented as an integration of Cu and low-k technologies (news briefs on April 3, 2000); however, it does not advertise low-k dielectrics in its present state.

Note that this year is expected to register the transition to high-end low-k products for a number of companies. Therefore, this vendor list will be obsolete in the near future.

General reliability and radiation concerns:

Several foreseeable reliability concerns related to the use of low-k dielectrics in space environments are listed below. It must be stressed, that the incorporation of porosity betters the dielectric properties, but degrades all other characteristics. Furthermore, porous low-k dielectrics are inhomogeneous materials. Their properties do not scale linearly with porosity in the whole range, but undergo first order phase transitions at some porosity loading, called critical percolation threshold.

Space-relevant conditions, which don't occur in production or ground operation, may cause abrupt change of ILD behavior. The full extent of such complications for low-k COTS in NASA missions is not known, and must be determined experimentally. However, some anticipated scenarios can be addressed using raw materials or simple device or test structures; this will benefit their faster implementation in NASA missions.

1. Thermal conductivity

Most of the low-k candidates show thermal stability in the temperature range seen during production. MSSQ is stable in the 450-600 °C range, and SiLK can be processed below 450°C. The thermal conductivity, however, decreases rapidly with the incorporation of porosity, as heat conduction is limited to the solid phase of a porous material. Some studies show a >10 times decrease for materials with ~20% porosity (k~2.2 generation). Thus, a COTS device operating normally at <85 °C may not survive high-temperature environments, due to the inability to dissipate heat sufficiently fast. Furthermore, for porosity above the percolation threshold of the solid phase, the thermal conductivity diminishes. An excellent example is a sol-gel material, called xerogel, which is structurally similar to aerogel.

2. Mechanical strength

The low-k ILD candidates are mostly polymers, containing a large fraction of relatively weak bonds (C-H, O-H, etc.) and are susceptible to plastic deformation. They also contain "free volume" – open-volume areas depleted of bonds, which move under applied stress. Thus, polymers are inherently weaker than SiO_2. Their elastic moduli

decrease dramatically with porosity. It is still unclear whether the hardness of low-k films changes abruptly around the critical porosity volume, as some experiments seem to indicate.

3. Enbrittlement

The problems related to brittleness are not obvious, but are arguably one of the most serious. The transition from ductile to brittle state of a solid dielectric is a problem, which the industry must resolve in order to produce a reliable device package. The porosity, however, plays a dominant role in determining the ductile-to-brittle phase transition as a function of temperature. Highly porous materials are generally more ductile at room temperature, and the ductile-to-brittle transition occurs at lower temperature. Thus, one can envision a scenario in which this transition is shifted to below –60 °C, which meets the military standards. However, exposed to a lower temperature the material may fracture, which will render the device unusable.

4. Permeability to gasses and metal ions

This is arguably the best-known porous low-k property, which undergoes a first order phase transition at the critical percolation porosity fraction. Molecules, atoms and ions, placed anywhere within the volume are capable of reaching any other area through percolation pathways. This may have impact on space-relevant reliability issues, such as corrosion, operation in ion-rich environments (especially O-rich), and moisture absorption. Other reliability aspects relevant to device integrity, such as metal diffusion through porous media and the stability of barrier layers, are completely unknown under conditions which deviate from those relevant to the normal use and device production. They too must be investigated prior to using low-k COTS in space.

5. Radiation cross-linking

The cross-linking of a polymer low-k film must be kept within some tolerable limits in order to keep the device integrity. Too little polymerization will degrade the hardness, whereas too much will make the material brittle. The effects of electron

irradiation on polymers are known. Electron irradiation is used to produce harder, stronger and more fracture-tough non-porous low-k films, but large pores are hard to retain. Only recent advances allowed the incorporation of sub-nanometer pores in MSSQ (LKD film made by JSR). Electron beam curing effects are important, as they influence the characteristics of logic devices; therefore, control over the electron dose is of imperative importance for the final structural properties of the low-k material. With this in mind, the electron exposure is virtually eliminated after device production, whereas the electron radiation in space will continuously increase the low-k brittleness. Furthermore, cross-linking usually releases water. At large amounts, water condensation and/or corrosion may occur.

6. Ion radiation

Another concern is related to the use of low-k COTS in O-radiation environment. The majority of the low-k candidates are highly susceptible to oxidation, which changes dramatically their dielectric constant, in some cases more than a factor of two. This can destroy the signal synchronization, thus rendering a processor inoperable. As cross-linking by radiation, oxidation is associated with the release of water, and thereby with condensation and corrosion. Heavy ion radiation affects the dielectric behavior of polymers as well (shown for polyimide, another low-k candidate).

7. Combined effects

Effects that are caused by the simultaneous action of two or more factors, are most difficult to predict. However, some of them are foreseeable. For example, the increased brittleness through electron irradiation may be within tolerance limits for a device in controlled thermal environment, but may be detrimental in thermal cycling, or continuous extreme thermal exposure.

Reliability and radiation "tall tent poles" for specific mission scenarios

The guidelines below are classified by environment and the missions falling within these typical categories are listed.

1. Thermal environment

Low-k reliability tests are currently performed for commercial use. Thus it can be assumed that their functionality will be guaranteed in the 0 °C – 70 °C range. Thermal stresses due to cycling degrade the mechanical strength of the low-k ILD.

Missions that fall within these parameters:

✓ Spacecraft interior: LEO, ISS, STS, MEO, GEO, deep space and planetary orbiters with thermal control.

Missions that (currently) fall outside these parameters:

× Exterior all orbiters, Aeronautics, Mars surface, Venus, Solar orbiter.

2. Radiation environment

Exposure to electron radiation changes the chemistry and the mechanical properties of low-k ILD's (e.g., see NSREC 2002 Conference). The full extent of the radiation damage is unknown. The typical radiation environment for this assessment is considered for electronics protected by a 100 mil thick Al box.

Missions within these parameters can only be at LEO:

✓ LEO, ISS, and STS.

Missions that (currently) fall outside these parameters:

× MEO, GEO, Jovian, deep space, planetary orbiters, aeronautics, Mars surface, Venus, Solar orbiter.

3. Vibration environment

No available data. The major concerns are the acoustic vibrations during launch, which is relevant to all missions (×), and pyrotechnic shock during engine on/off operation (main engines and flight path correction engines).

4. Chemical environment

The low-k ILD is highly sensitive to chemical environment; however, the ILD is anticipated to be protected in an encapsulated package. In case of PEM's, they are not considered hermetic, and may leak moisture gasses through to the ILD. By far the major concerns are related to moisture intake; water corrodes many low-k ILD's. Gasses of concern are oxidants, and those with strong affinity to carbon.

- ✓ Missions using hermetically packaged ILD are probably acceptable
- × Missions using PEM's must conduct the necessary assessment tests

5. ESD/EMI environment

The ESD sensitivity of low-k dielectrics is not inherent from the low-k technology, but from the fact that they are first implemented in the most advanced high-end devices. In general, with the decrease of feature size, an integrated circuit becomes more sensitive to ESD and electromagnetic induction effects.

6. Other: Cu and low-k integration

There are no data on any combined effects on devices integrating both Cu and low-k technologies, which is the predominant choice in the industry, thereby for COTS.

Qualification guidelines, problems, and possibilities

To avoid exponentially increasing design cost, overall productivity of designed functions on chip must scale at > 2× per node. Non-ideal scaling of planar CMOS devices, together with the roadmap for interconnect materials and package technologies, presents a variety of challenges related to power management and current delivery. "Red bricks", i.e., technology requirements for which no known solutions exist, are increasingly common throughout the ITRS. On the other hand, challenges that are impossible to solve within a single technology area of the ITRS may be solvable with appropriate intervention from other areas. Feasibility of future technology nodes will come to depend on such "sharing of red bricks." Resource efficient communication and synchronization, already challenged by global interconnect scaling trends, are increasingly hampered by noise and interference. Prevailing signal integrity methodologies in logical, circuit and physical design, while apparently scalable through the 100 nm node, are reaching their limits of practicality. Relaxing the requirement of 100% correctness for devices and interconnects may dramatically reduce costs of manufacturing, verification, and test. Such a paradigm shift is likely forced in any case by technology scaling, which leads to more transient and permanent failures of signals, logic values, devices, and interconnects.

Qualification and guidelines for using low-k technology in NASA missions require addressing the many unknowns related to low-k performance in space environments. Considering the problems encountered by the semiconductor industry, which unavoidably postpones the use of low-k ILD's despite the benefits they offer, is a clear indication of the level of difficulty NASA will encounter when dealing with such COTS devices. Therefore, NASA must devote resources toward the assessment of the low-k technology in three stages – (1) on the material level, (2) integrated test structures and devices, and (3) COTS device level. The first stage is not influenced significantly by future technology developments, and can be addressed at the present. This process must rely strongly on interaction with leading manufacturers, as information is proprietary; thus, a basis for information exchange must be found. Radiation, thermal, mechanical

and vibration experimental testing can and should be done first on the material level, and should be extended later to test structures (2nd level) before low-k COTS can be qualified.

Timetable for readiness

The extract from the most recent 2001 edition of the ITRS (below) shows the roadmap for the implementation of the low-k technology in microprocessor units (MPU). Note that the updated version of the ITRS, which will appear later this year, is expected to delay the low-k technology implementation. Also, devices with k = 2.7 were not available in 2001 and only a few were available in 2002. The yellow areas ("manufacturable solutions are known") mark the incorporation of a small amount of porosity below the critical percolation threshold. Larger porosity loads do not result in known manufcaturable solutions (red areas).

Table 62a MPU Interconnect Technology Requirements—Near-term

Year of Production	2001	2002	2003	2004	2005	2006	[illegible]
Interlevel metal insulator —effective dielectric constant (k)	3.0-3.6	3.0–3.6	3.0–3.6	[illegible]	[illegible]	[illegible]	[illegible]
Interlevel metal insulator (minimum expected) bulk dielectric constant (k)	<2.7	<2.7	<2.7	[illegible]	[illegible]	[illegible]	[illegible]

White Manufacturable Solutions Exist, and Are Being Optimized
Yellow–Manufacturable Solutions are Known
Red–Manufacturable Solutions are NOT Known

Table 62b MPU Interconnect Technology Requirements—Long-term

Year of Production	2010	2013	2016
Interlevel metal insulator—effective dielectric constant (k)	[illegible]	[illegible]	[illegible]
Interlevel metal insulator (minimum expected) —bulk dielectric constant (k)	[illegible]	[illegible]	[illegible]

Technology evolution in near term

The low-k technology is evolving fast. There are several basic aspects of the merit for success, which will ultimately determine the outcome of the evolution:

- Dielectric versus mechanical properties approach.

  The dielectric constant for the 130 nm generation is k~2.7. This is achievable with most spin-on polymers (k varies between 2.6 and 2.8) and with CVD materials. However, the approaches to achieving ultra-low-k (k<2.2), which require porosity, are different. One can either start with a mechanically strong material, such as oxide (which has higher k), and incorporate high porosity loading (~40%), or with the weaker polymers, and incorporate less porosity (~20%). The former approach will have to resolve the problems arising from the fact that the pores are inevitably connected, whereas the latter will have to deal with the weakened mechanical structure of the device. The latter may not be immune to pore percolation either. Work is being done in both directions, but currently there is no preferential approach.

- Pore size and morphology

  Extendibility to ultra-low-k by porosity incorporation is the cornerstone of success for each low-k material, and it has a high impact on its commercialization potential. This will rule out CVD materials at some stage (e.g., <65 nm technology). The spin-on dielectrics, however, have not achieved the desired pore size and pore morphology for that generation either. The typical pore size (5-10 nm) is too large in comparison to the pitch size. It is not clear how these materials will evolve, since the present methods are unlikely to produce ~1 nm size pores.

- Integration and contamination problems

  The process of maturing of the low-k technology is hampered by the large number of considered candidates (despite the decrease seen in the last few years). Companies are still looking for the "magic recipe" for the ideal candidate, which satisfies all

previously described conditions, integrates well in the process, and causes no contamination concerns. Until the candidate list is narrowed down to 2 or 3, the technology may not mature sufficiently to produce space-worthy devices.

- Commercial aspects

  For the first time in history, chemical material vendors and chip manufacturers are working together to resolve the integration problems of low-k dielectrics, which led to the formation of partnerships in the industry. One example is the Dow-IBM collaboration, which involves significant resources. Companies with smaller research capabilities monitor the progress preparing to embrace the low-k ILD that makes it first to the market, and purchase the complete process. Thus, the success of the Dow-IBM effort may sway the market in the direction of the Dow product (SiLK). The opposite will result in larger market share for the CVD and MSSQ based materials.

Recommendations for space use of low-k dielectrics

Due to the extent of the research needed to enable the low-*k* technology use in NASA missions, investigation of all low-*k* candidates is unjustifiable. An earlier conducted survey identified 3 low-k candidates with high commercialization potential:

- CVD-deposited carbon-doped silicate films are the choice of low-k for companies that plan to postpone the change of deposition technology to spin-on dielectrics. Chip manufacturers own CVD tools, and the expertise acquired in their use plays an important role in selecting CVD dielectrics. The largest providers for CVD low-*k* (combining to >90%) are Applied Materials (with *Black Diamond*) and Novellus (with *CORAL* films).

- SiLK – a spin-on product by Dow Chemical Co. – has already been implemented in high-end products (ASIC's and microprocessors).

- SSQ (HSSQ and MSSQ) – these are the low-k materials of choice for many vendor companies. As spin-ons, SSQ's are alternative to the CVD materials, which are inadequate for the 100 nm technology node. Due to integration difficulties of SiLK

and cost of CVD low-k, SSQ's is likely to rapidly emerge as the low-k choice of many device manufacturing companies.

Apart from using FSG (Intel), approximately 80-85% of the 130 nm low-k CMOS devices will be made with the above materials. They represent a suitable choice for future NASA research. CVD materials will be used by one (or maximum two) generation of COTS, while the embedded porosity in spin-on dielectrics makes them usable in many COTS generations. It should be noted that, recently, several large companies have made unsuccessful attempts to integrate spin-on low-k dielectrics in their state-of-the-art technology, and have elected to use CVD materials instead. This trend may increase the importance of the CVD materials beyond the initial projections.

The properties of the low-k dielectrics are significantly different from those of the conventional oxide, and the behavior of low-k COTS in hostile space environments can be very different. Due to the present unavailability of low-end low-k COTS devices, qualification of such parts is impossible. However, much relevant information can be learned from blanket films or using simple devices. Materials properties govern device behavior in a number of cases, and their understanding is imperative for the successful use of low-k COTS in space, and for the timely transfer of this new technology to space exploration missions.

The proprietary nature of the low-k materials limits wide access to the ILD candidates. This barrier can only be overcome by working in collaboration with the industry. The market needs, however, dictate the companies' interests to produce reliable manufacturable ILD's, which have no overlap with NASA interests to assess the low-k technology for use in space environments. Therefore, a basis that can be used for information exchange must be found.

Acknowledgments

The research described in this paper was carried out at the Jet Propulsion Laboratory, California Institute of Technology, under a contract with the National Aeronautics and Space Administration.

References herein to any specific commercial product, process, or service by trade name, trademark, manufacturer, or otherwise, does not constitute or imply its endorsement by the United States government of the Jet Propulsion Laboratory, California Institute of Technology.

References and bibliography

1. Technology trends: The International Technology Roadmap for Semiconductors (ITRS), 2001 Edition, International SEMATECH (http://public.itrs.net/)
2. Overview: Proceedings of the Ultra-Low-K Workshop 2002 (available from International SEMATECH)
3. Recent overview: IEEE spectrum, February 2003
4. NEPP report (includes references): M.P. Petkov, "Preliminary reliability evaluation of commercially available low-k interlayer dielectrics for space applications"
5. Radiation damage: M.P. Petkov et al., *IEEE Trans. Nucl. Sci.*, vol. 49, p. 2724 (2002).
6. Radiation effects: R.A.B. Devine at al., *IEEE Trans. Nucl. Sci.*, vol. 49, p. 2729 (2002).