Effect of Scaling on Space Radiation Sensitivity of Advanced CMOS Devices

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Outline

Scaling Projections

Radiation Test Results for Microprocessors (epitaxial substrates)
  - Registers and cache (SRAM technology)
  - General functional errors

Soft-Error Results from Industry

Summary
Mainstream Technologies for the Near Term

SIA Roadmap Overestimates Scaling Progress
- Highest performance devices are for very specialized applications
- Realistic scaling projections require different tradeoffs
  On-off ratio must be between $10^4$ and $10^6$
  Power supply voltages for logic will plateau at 1 volt
- Next technology node is 90 nm

Benchmarks:
- Commercial microprocessors
- High-density memory technology

SOI Is Becoming a Mainstream Technology

Advanced Bulk CMOS for the Year 2008: $L = 25$ nm

- 50 nm lithography
- “Super-halo” doping to control short-channel effects
- $\sim 20$ mV threshold voltage fluctuation (1 $\sigma$)
- Adaptable to partially depleted SOI
Design Features of Power PC-Series Microprocessors

<table>
<thead>
<tr>
<th>Device</th>
<th>Feature Size (µm)</th>
<th>Die Size (mm²)</th>
<th>Core Voltage (V)</th>
<th>Max. Operating Frequency (MHz)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Motorola MPC750 (G3)</td>
<td>0.29</td>
<td>67</td>
<td>2.5</td>
<td>350</td>
</tr>
<tr>
<td>IBM MPC750</td>
<td>0.22</td>
<td>40</td>
<td>2.0</td>
<td>533</td>
</tr>
<tr>
<td>Motorola MPC7400 (G4)</td>
<td>0.20</td>
<td>83</td>
<td>1.8</td>
<td>500</td>
</tr>
</tbody>
</table>

Microprocessor Testing Issues

“Flip-Chip” Bonding Generally Requires Irradiation from Back of Device
- Tests done on “thinned” samples
- Substrate thickness reduced to 100 to 200 microns

Test Methods Are Complex
- “Short-loop” register tests
- More complex operational software
- High-frequency operation

Special Diagnostic Methods Are Required
- Register tests often assume that core operations in processor don’t change
- “Hangs” and “crashes” occur during testing
- Various hardware methods can be used
- Software with embedded diagnostics
Test Results for Power PC Microprocessors

Scaling Trends for Heavy-Ion Cross Section
Scaling Issues for Single-Event Upset

1 - Critical Charge

2 - Collected Charge

3 - Circuit Effects

Charge from alpha particles or neutrons


Feature Size (L, μm)

Charge Multiplication in Partially Depleted SOI Devices

Errors/Hour/Byte from Alpha Particles

Lateral gain = 4

Lateral gain = 0.1

Feature size = 0.25 μm

(From Mistry, et al., ED, 1999)
Single-Event Upset in Advanced Twin-Well Process

SOI CMOS Structure
3-D Modeling of the Effect of Junction Area on Charge Collection from Alpha Particles

Lines correspond to model
Points are for 3-D simulation
Trench isolation (0.3 micron)

Dependence of Neutron Soft Error Rate on Scaling

SRAM test structures from digital processes
SER measured in Los Alamos WNR

S. Hamland, et al. 2001 VLSI Symposium
Permanent Damage from Single Particles

Microdose Effects in DRAMs or Low-Power Logic
- Continues to be an issue, even for devices with thinner gates
- Mechanisms in storage capacitors may be a factor

Microdose Effects in Flash Memories
- Charge pump and high-voltage logic
- Cell errors in multi-level storage technology

Permanent Damage in Oxides
- Probably not an issue for conventional oxides and circuits
- May still be a factor for storage arrays used in long-duration space missions

Conclusions

Scaling Appears to Decrease SEU Upset Sensitivity for Mainstream Technologies
- Decreased charge collection efficiency
- Influence of "hardening" commercial devices for atmospheric radiation
- Transients and "crashes" are secondary issues for 0.13 – 0.18μm technology

Future Trends Are Difficult to Predict
- "Most likely" 2008 device will probably follow current trends
- Commercial SOI processes reduce sigma, but not LET\_thresh
- Very low voltage or low power technologies may be more sensitive to SEU

Complex Device Architecture and Circuit Design Are "Wildcards"
- Processors
  - High-speed device design is quite involved (dynamic logic)
  - Changes in cache design may affect error rate (e.g., partial use of DRAMs)
- DRAMs
  - Architecture for high-speed devices
  - Storage capacitor design continues to evolve
  - Novel designs that work at low voltage