Process and Pixels for High Performance Imager in SOI-CMOS Technology

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We present the pixel and process design and test-results from imager pixels implemented in SOI-CMOS technology. While bulk-CMOS foundries have made various alterations in their process flow to integrate a CMOS imager front-end with high performance processors, and spectacular progress has been made in making large format imagers, several major challenges remain. These pertain to obtaining low and anomaly-free dark-current, low cross-talk, high linearity, good response uniformity and high dynamic range. Non-planarity in the junction area, resulting from LOCOS or STI isolation, high doping, and high electric fields cause problems for dark current reduction, while simultaneously obtaining small depletion widths for deep sub-micron FETs and large depletion widths around the photodiode junction cause problems for cross-talk and quantum efficiency.

In recent years, SOI-technology has matured considerably, and is considered to have significant advantages for high-speed (RF), high-density VLSI. In the SOI technology, the MOSFETs are implemented in a thin (50-400 nm) SOI-device layer, that is separated from a low-doped substrate (handle-wafer) by a buried oxide (BOX), as shown in fig. 1a. A vast reduction of photon absorption in the skinny SOI layer prevents efficient photodiode implementation. We implement high-response photodiodes in SOI technology, by etching the BOX in the diode area, and implementing the photodiode in the handle-wafer, as shown in fig. 1b. The handle-wafer diode is connected to the MOSFETs in the SOI-layer during metallization. Since the handle-wafer doping is low (~ $1x10^{13}/cm^3$), excellent photo-response and low cross-talk can be achieved. Since the readout and the detector are implemented in separate silicon layers, they can be independently optimized, without introducing significant process complexities.

For implementation of high-quality photodiodes, two additional implants are needed, as shown in fig. 1b. These are: (i) Pinning implant: a p-implant under the BOX, and (ii) Surface-passivation implant: a n or p implant in the BOX-cut area. These implants hold Si-SiO_2 interface in equilibrium to eliminate interface-related dark current generation. The surface implant also prevents a tunneling between heavily-doped areas, and reduces the surface electric field. The n^+ and the p^+-implants needed in the handle-wafer for photodiode and ground-contact are carried out at the same time as the SOI FET S/D implants, as shown in fig. 2. The pinning implant is carried out first through the BOX, except in areas where there will be BOX-cuts. Following the SOI island formation, the BOX layer is etched, and the surface implant is applied. After this, the process-flow is the same as that of a conventional SOI, except that the BOX-cut area receives appropriate n^+ and p^+ implant during subsequent S/D implants.

We implemented small arrays of test-pixels in a 10, 15, 20, and 23.6 μm pixel pitch using a 0.8 μm partially-depleted SOI-CMOS process (3.3V V_{dd}). Each test-array pixel consists of a conventional "3-T" photodiode pixel: a photodiode buffered by an n-channel switched source-follower. The handle-wafer doping was ~ $2x10^{13}/cm^3$, and the wafers were built using a smart-cut process. In this process, the wafer-bonding takes place between two thermally grown oxide surfaces (which form the BOX), preserving both oxide and Si-SiO_2 interface quality. Since, a partially depleted SOI process was used, in-pixel FETs were laid out using different body-tie methods, as shown in fig. 3, in order to eliminate floating-body effects. The effect of floating-body on imager performance (lag, linearity, and response time) and viability of the body-tie techniques will be presented in the paper.

Pixel designs with different pixel geometry and implant placements were carried out to investigate the effects of process and pixel layout on photon response and dark current. Fig. 4 shows the measured spectral QE of the baseline pixel. The pixel responds all the way to 1100 nm, and with a peak QE~70% at 900 nm. The spectral response is also much flatter than that of a bulk-CMOS imager, the increased response being indicative of a large depletion width (estimated to be ~16 μm) arising from reduced substrate doping. Table 1 summarizes an initial comparison between different SOI pixels. The dark current was small, being < 2 nA/cm^2 for a 15^2 μm pixel, almost all dark electrons being generated in the large depletion volume. The baseline pixel with pinning and surface implants provided the lowest dark current, while the pixels without the surface implant showed a 3x increase in dark-current, and the pixels without the pinning implant did not work at all. In the paper, we will discuss the dependence of pixel layout and implant placements on imaging performance. In conclusion, responsivity, cross-talk, and dark-current of SOI-CMOS imager pixels will result in high-performance imager implementation.

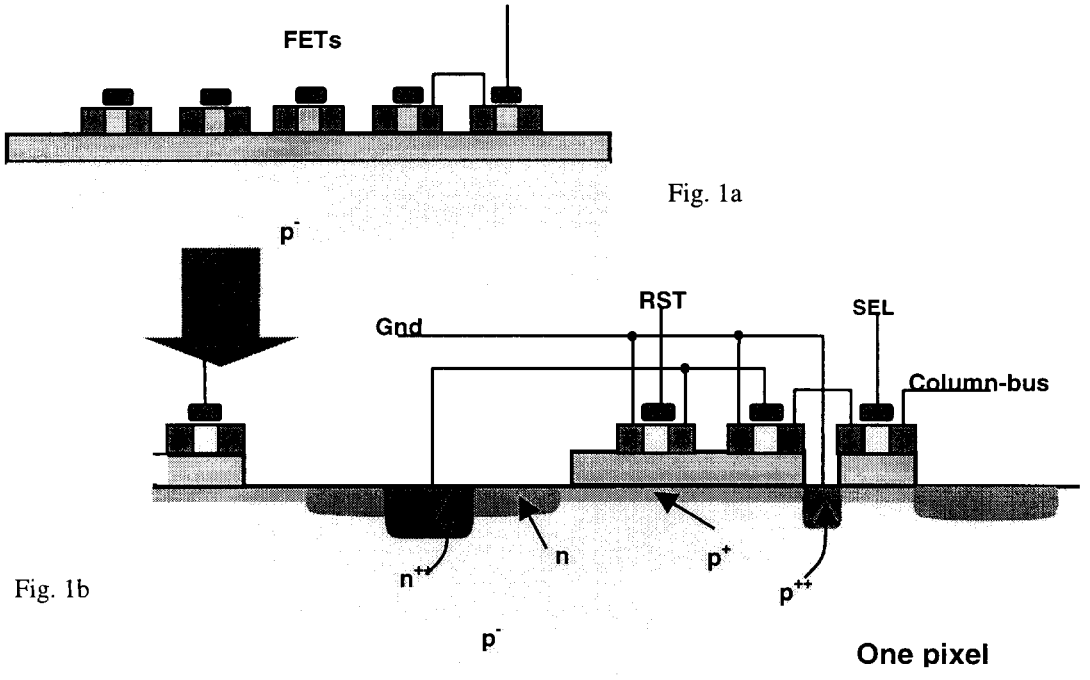

Figure 1: Evolution of a SOI-CMOS imager pixel cross-section (fig. 1b) with photodiode in the handle-wafer from a conventional SOI cross-section (fig. 1a)

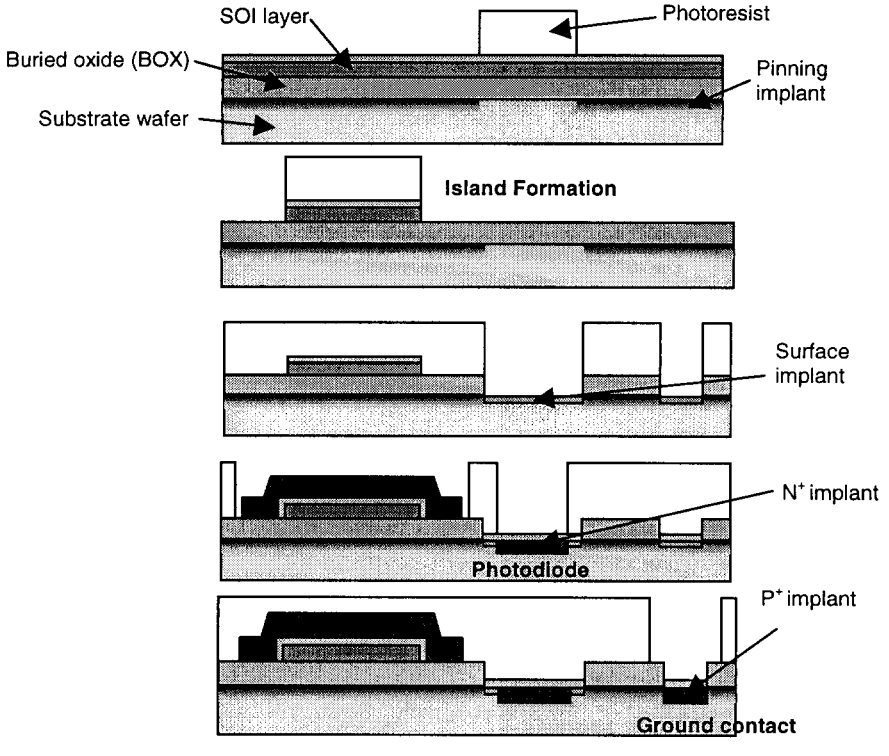

Figure 2: SOI-CMOS imager key process flow steps

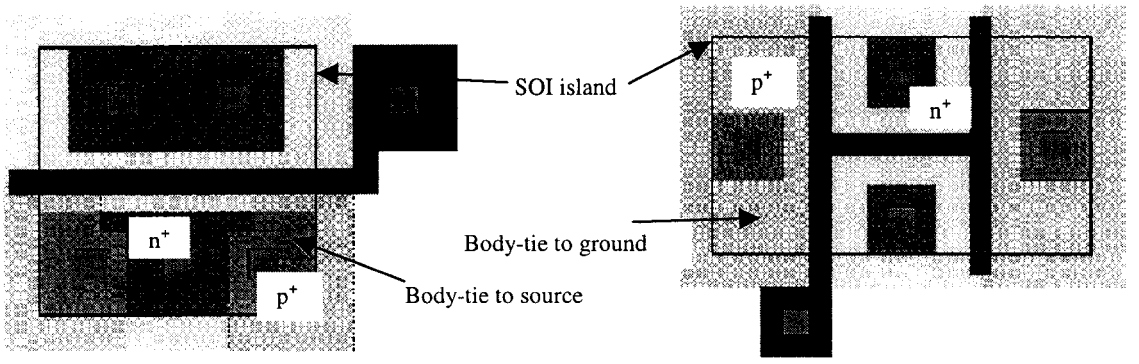

Figure 3: Layout of in-pixel FETs with different body ties Evolution of a SOI-CMOS imager pixel cross-section (fig. 1b) with photodiode in the handle-wafer from a conventional SOI cross-section (fig. 1a)

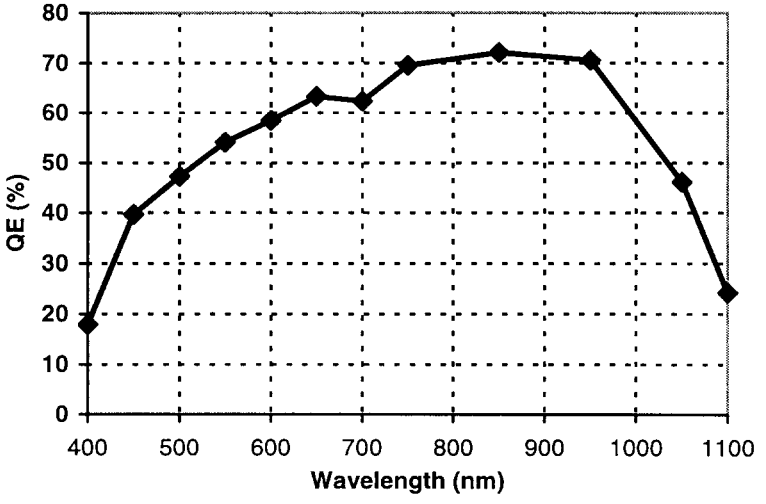

Figure 4: Measured quantum efficiency of an CMOS imager pixel

Table 1: Comparison of SOI imager pixel performance

Characteristics	Pixel 1	Pixel 2	Pixel 3	Pixel 4
Description	N^+, SI, PI	N^+, SI, PI	N^+, No SI, PI	N^+, no PI
Pitch (μm)	15	20	15	15
Responsivity (μV/ph)	22.3	13.8	23	Didn't work
QE (%)	70	72	73	X
Dark-rate (nA/cm^2)	2.1	2.0	7.0	X
Full-well (ke)	49	90.6	44	X