

Issues Concerning the Replacement of Lead in Hi-Rel Electronic Applications

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Abstract—Because of its toxicity and adverse effect on human health, pressure is mounting on the electronics industry to replace lead (chem. symbol Pb) in solders. Lead solders have been used for many years. Recently, several alternatives have emerged. This paper examines some of these alternative solders for their suitability in replacing tin/lead solder in high-reliability applications.

1. BACKGROUND

Historically, eutectic tin-lead (Sn63Pb37) or near-eutectic tin-lead (Sn60Pb40) solders have found wide application in the electronics industry for many years. Eutectic tin-lead solder has a fixed melting point (183°C) that lends itself to reasonably facile production methods to join electrical and electronic components to printed wiring boards. The chief purpose of a solder joint is, of course, to create a mechanical and electrical interconnection between components and the printed wiring board on which they are mounted. Billions of solder joints have been created on countless printed wiring boards using this material. In addition, the mechanical and electrical properties are well understood, and the reliability of solder joints created using eutectic tin-lead or near-eutectic tin-lead solders has been established and is well understood.

It has been recognized for many years that lead (chemical symbol: Pb), like other heavy metals, has toxicological properties that can have a direct impact on human health. Over the years, lead has been banned in a variety of products because of this concern. Two chief examples spring readily to mind: tetraethyl lead was finally and completely banned as an antiknock additive in gasoline in 1987, and lead pigments in paints were banned in 1977.

There now exists a serious movement to ban the use of lead in electronics and electronics products. The concern is that many of these products, especially commercial electronics products, will eventually end up in landfills and that the lead contained within the solder joints will eventually end up in ground water. It has been repeatedly

pointed out that the amount of lead in the environment that might arise from electronics is miniscule. Nevertheless, the political reality is that lead is perceived as a threat to the environment and to human health—which is true—and that lead arising from electronic applications and products is producing a significant amount of lead in the environment—this is moot. Because of this concern, there is now a movement that has international support to ban the use of lead in electronics products.

The situation is different in different parts of the world. In Japan, various companies have made the elimination of lead from their products a quality policy. In Europe, various countries are proposing legislation that would seriously curtail the use of lead in electronic products. In the US to date there is no legislation curbing the use of lead in electronics. However, US companies are now operating in a truly international global climate. Many feel that it would be expedient to comply with the elimination of lead in their products so that they are not perceived as reactionary in regard to environmental and health issues.

Because of the adverse climate and the serious issues facing the continued use of lead, the US electronics industry is facing the prospect of the elimination of lead in electronic products. This leads to a number of serious issues that the electronics industry must face if this phaseout is to be successful. Some of these issues are:

1. Political issues: Will the use of lead eventually be legislated so that it will be very difficult, or impossible, to continue using it? There is some analogy to the phaseout of ozone depleting substances, especially the popular electronic cleaning and defluxing solvents based on 1,1,2-trichloro-1,2,2-trifluoroethane (popularly known by its DuPont trade name Freon[®]). The production, but not its use, was banned by the signatories of the Montreal Protocol. The same could well happen to tin-lead solders.
2. Psychological-sociological issues: It the perception exists that lead in tin-lead solder constitutes a serious

health risk, then pressure will mount on companies to curtail or eliminate lead from their products regardless of whether lead is actually curtailed or banned through legislation. In addition, pressure can mount on legislators to take positive action to curtail or eliminate lead.

3. Supply issues: (1) The production alone of tin-lead solders could be halted, or (2) both the production and the use of such solders could be stopped. If either is the case, are solders based on other elemental compositions easily accessible? What will be the costs of these new materials and how will these costs be borne? Will new supplies be adequate to meet the demand?
4. Technical issues: If the production of tin-lead solders, or both the production and the use of such solders, is curtailed or forbidden either by legislation or forced by social perception, what solders can be used as potential replacements and what are the technical issues in finding suitable replacements?
5. Human health and environmental issues: Some of the proposed replacement solders for tin-lead also contain heavy metals, such as bismuth, antimony, and silver, all of which have known adverse toxicological effects. What are the benefits and drawbacks of such materials if they find widespread use in electronics as opposed to the continued use of lead?

These are some of the serious issues that must be addressed in finding a suitable replacement. Very often, R&D has focused more strongly on only the fourth issue, the technical one. However, all are important, and a failure to appreciate the other four and factor them into finding a replacement is ultimately detrimental.

2. HI-REL ELECTRONICS APPLICATIONS

The high reliability electronic applications market is just a niche of the overall electronics market. Nevertheless, it is a very important niche. High reliability applications presume that the electronics as manufactured must perform in its intended service environment and function as intended on demand. Generally, failure is not an option since it entails the loss of human life and/or the loss of a very expensive and often irreplaceable piece of hardware. Because of these demands, hi-rel manufacturing methods and materials are often difficult to subject to change unless each contemplated change is thoroughly documented and proven. The resulting risk of making a change is very high.

Almost all viable lead-free candidate alloys have melting points greater than 200°C but below that of pure tin, which has a melting point of 232°C (449°F). A little over a year ago, the National Aeronautics and Space Administration (NASA) funded a project to begin searching for suitable candidates under the aegis of the NASA Electronic Parts and Packaging (NEPP) program.

Four lead-free solder pastes were selected based on an extensive search of the literature. These are given below in Table 1 along with advantages and drawbacks of each.

3. OBJECTIVES

The overall task is presently composed of two phases. Each phase has its own particular objective.

Objective of Phase I

Ensure that the four lead-free pastes listed in Table 1 could be successfully assembled.

An important issue was whether printed wiring boards (PWBs) and components could be processed at the higher process temperatures (30°-35°C greater than for eutectic tin-lead). This was the key objective of the first year of the project (Phase I). Eight PWBs (two PWBs per paste) using the four different solder pastes per Table 1 were assembled. Two PWBs per solder type were assembled using the four different solder pastes resulting in total of eight assemblies. See Figures 1 and 2, showing the bottom and top view respectively of the test PWB used in the Phase I investigation.

The PWBs were assembled in the SMT Laboratory at JPL. A bench-top reflow unit (on loan) + a perfluorinated liquid were utilized in assembling the PWBs. Except for the BGAs, the leads of the components used were tinned with Sn/Ag bar solder. Scanning acoustic microscopy analysis performed on test boards and components was utilized for ascertaining if damage occurs to boards during processing. The boards themselves processed satisfactorily at the higher temperatures. However, some of the plastic BGAs were revealed to have experienced delamination, indicating the necessity of baking them prior to reflow. See Figures 3 and 4, showing the bottom and top view respectively of the test PWB assembled using the lead-free paste having the composition Sn95.5Ag3.8Cu0.7.

Table 1 Lead-free solder alloys for Phase I processing

Composition	T _m (°C)	Advantages	Potential issues
1) Sn96.5Ag3.5 (eutectic)	221	a) Good wetting characteristics and superior joint strength compared to Sn-Pb solder b) Long history of use	a) May exhibit structural weakness at solder connections b) High T _m
2) Sn95.5Ag3.8Cu0.7	217-218	a) Recommended by NEMI b) Virtually no plastic range c) Rapid solidification avoiding formation of cracks d) Formation of intermetallics Cu ₆ Sn ₅ and Ag ₃ Sn provide greater strength and fatigue resistance than Sn-Pb solder	a) High T _m
3) Sn96.2Ag2.5Cu0.8Sb0.5 (Castin [®])	217-218	a) Addition of antimony (Sb) improves thermal fatigue b) Solder coating offers flatter pads and uniform coat c) Works well with Ni/Au Ag/Pd and OSP boards d) Antimony slightly reduces melting temperature and refines grain structure	a) Antimony trioxide may exhibit toxicity at higher temperatures b) High T _m
4) Sn77.2In20.0Ag2.8 (Indalloy 227 [®])	175(T _S)- 187(T _L)	a) Compatible T _m to Sn-Pb b) Good ductility, strength and creep resistance c) Low dross in wave solder	a) Supply and cost may be prohibitive factors in its use b) 118°C eutectic point may deteriorate mechanical properties of solder joints c) Large plastic range



Figure 1 Bottom view of the test PWB



Figure 2 Top view of the test PWB

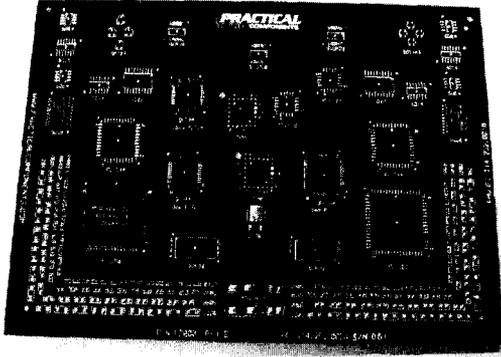


Figure 3 Bottom view of the test PWB assembled using Sn95.5Ag3.8Cu0.7

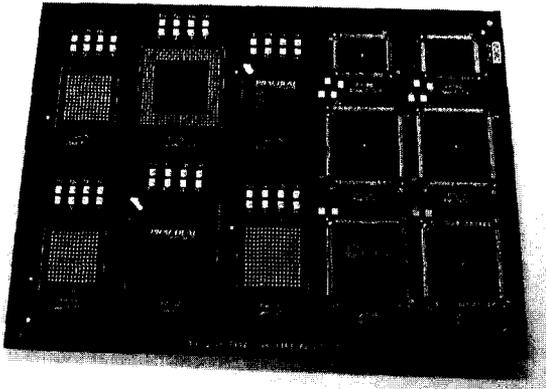


Figure 4 Top view of the test PWB assembled using Sn95.5Ag3.8Cu0.7

Objective of Phase II

During the second phase, four (4) PWAs per paste will be assembled along with using eutectic Sn/Pb (Sn63Pb37—183°C T_M) as a control. The resulting assemblies will be thermal cycled and microsectioned at selected regions to perform microstructural analysis.

Four PWBs per paste (2 pastes) will be assembled and thermal cycled. The exact thermal cycle is still to be determined. In addition, four PWBs produced with eutectic tin-lead paste will be assembled and thermal cycled as a control lot. Assembling these twelve PWBs, thermal cycling them, and assessing the solder joint reliability is the principal objective of the second year of the project (Phase II). Microsections will be taken at the sites of the largest and smallest solder joints before, during, and after thermal cycling.

At this point, the particular thermal cycle to be used in Phase II has not yet been decided upon. There are several

types of thermal cycles being used depending upon the product and the industry.

These are described in IPC-9701. Some of them are:

- JPL Cycle: -55°C to 100°C;
- Military Cycle: -55°C to 125°C;
- Commercial: 0°C to 100°C.

At present, the thermal cycle that appears most suitable is the Military Cycle: -55°C to 125°C.

4. PERTINENT PROCESS INFORMATION

The following JPL process information is pertinent to the discussion. In general, low volume surface mount technology (SMT) manufacturing methods pertaining to high reliability printed wiring assemblies (PWAs) were employed.

Rosin-based Fluxes and Pastes

Rosin-based fluxes and pastes are used to produce all electronic hardware. Using the terminology of Mil-F-14256, the classification of these products is rosin mildly activated (RMA).

Semi-automated Screen Printing

The solder paste is applied using a semi-automated screen printer ensuring that the paste is deposited in a uniform and consistent manner. Only stainless steel stencils are used in conjunction with a stainless steel squeegee. All boards are visually inspected for proper paste deposition after the stencil operation. A laser-based solder paste height and width measurement system is used with a resolution of 0.0001 inch (2.5 μm). This system provides real time information on the uniformity of solder paste deposition. All boards are subjected to this measurement prior to the reflow operation.

Automated Placement Machine

An automated placement machine is used to place parts on the printed wiring board (PWB).

Batch Vapor Phase Reflow Machine

A batch vapor phase reflow operation was used to create the solder joints of the SMT PWAs. The SMT PWAs are thermally profiled using a M.O.L.E.[®] A thermocouple was attached to the PWB and to the M.O.L.E., which is a microprocessor-based data logger attached to a computer. Thermal profiling was done to eliminate thermal shock during preheat and reflow. This operation consisted of a vapor phase reflow machine using a constant boiling

perfluorocarbon material—under a proprietary name with b.p. 240°C—for soldering the lead-free SMT PWAs. The PWAs were preheated to remove paste volatiles and to initiate the activation stage of the paste. The reflow liquid, since it boils at a constant temperature, minimizes the possibility of overheating the PWAs during reflow and ensures that the vapor blanket performs a uniform and consistent soldering operation. Because of the melting points of eutectic tin-lead paste and Indalloy 227 (see Table 1), the standard 3M Perfluorocompound® FC-5312 having a boiling point of 216°C was used.

5. EXPERIMENTAL

Packages Used on Test PWBs

Double-sided test PWBs with footprints for various chip components and integrated circuit (IC) packages, including ball grid arrays (BGAs), were assembled. Figures 1 and 2 depict the bottom and top side respectively of the bare test PWB. Figures 3 and 4 depict the bottom and top side respectively of PWA001, assembled with Sn95.5Ag3.8Cu0.7. See above. The BGAs were daisy-chained. The various component package types used and the number of each per PWB were as follows:

- Chip resistor, 0603 package (24 each per board);
- Chip resistor, 1206 package (18 each per board);
- Small outline transistor (SOT) 23 package (2 each per board);
- Small outline integrated circuit (SOIC) 20 package, 50 mil pitch (2 each per board);
- Plastic leaded chip carrier (PLCC) 68 package, 50 mil pitch (1 each per board);
- Quad flat pack (QFP) 100 package, 25 mil pitch (1 each per board);
- Quad flat pack 208 package, 20 mil pitch (1 each per board);
- Ball grid array (BGA) 225 full array package, 1.5 mm ball pitch (1 each per board);
- Ball grid array 352 area array package, 1.27 mm ball pitch (1 each per board).

Pre-assembly Inspection and Test

Prior to assembly, all the BGA pads on the PWBs were checked to ensure the daisy-chain integrity, and in addition, all BGA components were checked to ensure the daisy-chain integrity. All eight PWBs and one sample of each component were examined with scanning acoustic microscopy (SAM) to obtain a signature prior to assembly.

PWB Cleaning

All PWBs were cleaned in a centrifugal cleaner using an aqueous-based chemistry. This chemistry consists of a 20% solution of a proprietary blend of alcoxipropanols and amine compounds in DI water (Vigon A200 solution) with 1% corrosion inhibitor and 0.1% defoamer. The cleaning cycle and its parameters were as follows.

- Purge the wash chamber with nitrogen gas for one minute;
- A wash cycle of 5 minutes duration using Vigon A200 solution heated to 50°C;
- A rinse cycle of 10 minutes duration using DI water heated to 50°C;
- A dry cycle of 5 minutes duration using air heated to 180°C;
- A vacuum oven bake cycle for 8 hours at 100°C.

Screen Printing

PWBs were screen printed with four different pastes. See Table 2.

Table 2 Four Pb-free solder pastes used

Item	Paste composition	PWB serial number
1	Sn95.5Ag3.8Cu0.7	PWA001; PWA002
2	Sn96.2Ag2.5Cu0.8Sb0.5 (Castin®)	PWA003; PWA004
3	Sn96.5Ag3.5 (eutectic)	PWA005; PWA006
4	Sn77.2In20.0Ag2.8 (Indalloy 227®)	PWA007; PWA008

Printing Parameters

The printing parameters were as follows:

- Stencil Type—Stainless steel with foil thickness of 7 mils;
- Squeegee Type —metal blade;
- Squeegee pressure setting — 5.6 kg;
- Squeegee speed— 15 mm per second. Paste height was measured using 3-D a laser-based measurement system.

Component Placement

Components were placed on side 1 (top side) using an automated placement machine. A split-vision rework system was used for component placement on side 2 (bottom side).

Solder Paste Reflow

Two types of vapor phase reflow systems were used to reflow the solder pastes. Both consisted of an infrared preheating zone followed by a constant temperature boiling vapor zone. Pastes 1–3 (listed in Table 2) were reflowed using a bench top vapor phase system containing the perfluorocarbon material with a boiling point of 240°C. Paste 4 was reflowed using a stand-alone system containing a perfluorocarbon material with a boiling point of 216°C. A thermal profile was generated for each system. Assemblies were preheated to approximately 158°C at the rate of 0.88°C/sec followed by vapor phase reflow. The dwell time above liquidus was 62 seconds.

Post Reflow Cleaning

All PWAs were cleaned in the centrifugal cleaning system using the cleaning cycle and cleaning chemistry described in *PWB Cleaning* above.

Cleanliness Testing

After processing, all PWAs were tested for their ionic contamination level using a suitable ionic contamination tester. The cleanliness levels achieved per PWA are presented in Table 3 below. The results are presented in microgram per square centimeter ($\mu\text{g}/\text{cm}^2$).

Ionic Cleanliness Cutoff Limit

The ionic cleanliness cutoff limit per JPL specifications is $1.55 \mu\text{g}/\text{cm}^2$. All assemblies must have a contamination level less than this; otherwise, they must be recleaned and tested. These processes are repeated until the ionic cleanliness level is less than $1.55 \mu\text{g}/\text{cm}^2$.

Processing After Cleanliness Testing

After cleanliness testing, all PWAs were baked in a vacuum at 70°C for 30 minutes.

Table 3 Ionic contamination levels

S/N	Solder paste composition	Amount of ionic cont. $\mu\text{g}/\text{cm}^2$
S/N001	Sn95.5Ag3.8Cu0.7	0.050
S/N002	Sn95.5Ag3.8Cu0.7	0.051
S/N003	Sn96.2Ag2.5Cu0.8Sb0.5 (Castin [®])	0.008
S/N004	Sn96.2Ag2.5Cu0.8Sb0.5 (Castin [®])	0.008
S/N005	Sn96.5Ag3.5 (eutectic)	0.040
S/N006	Sn96.5Ag3.5 (eutectic)	0.029
S/N007	Sn77.2In20.0Ag2.8 (Indalloy 227 [®])	0.260
S/N008	Sn77.2In20.0Ag2.8 (Indalloy 227 [®])	0.198

Visual Inspection and X-Ray

All PWAs were inspected under a microscope at 12X magnification. The observations made were as follows:

- The solder flow generally appeared good except that the lead-free solder joints appeared grainier compared to Sn-Pb solder joints.
- The solder joints containing indium were even more grainy than the other three lead-free types of joints.
- There was one solder bridge at the corner on S/N 008. Other than that, there was no bridging.

Scanning Acoustic Microscopy

All PWAs were examined with a scanning acoustic microscope to reveal the post-assembly signature of the boards. No delamination due to the higher processing temperatures was noted.

6. CONCLUSIONS

The following conclusions can be drawn.

- A longer delay was required for the first three pastes—the ones with a higher processing temperature—during the reflow process.
- No problems were encountered during the printing process with the lead-free pastes. The printing was uniform for all PWBs.
- Although the solder fillets looked good, the solder joints appeared grainier than those formed by Sn63Pb37 solder.
- The ionic cleanliness levels of all assemblies processed with lead-free pastes were well below the $1.55 \mu\text{g}/\text{cm}^2$ acceptability limit.
- The daisy-chain continuity measured after reflow was the same as that prior to the reflow, indicating there were no opens after reflow.

Overall Conclusion

No problems were encountered during the manufacturing process with the lead-free pastes.

Phase II was initiated in October of 2002.

7. SUMMARY

The use of lead-free pastes to assemble PWBs seems feasible from a process point of view. However, new QA criteria will have to be devised for lead-free solder joints due to the grainy nature of their appearance.

8. ACKNOWLEDGEMENTS

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J.K. "Kirk" Bonner has twenty-five years experience in the electronics industry, with special emphasis on the industrial processes for manufacturing printed wiring boards and printed wiring board assemblies. Dr. Bonner has an in-depth knowledge of critical cleaning issues, especially those dealing with electronics. In January 1991, he was appointed a member of the United Nations Environmental Programme (UNEP) Solvents, Coatings, and Adhesives Technical Options Committee. Presently, he is a senior engineer at the Jet Propulsion Laboratory

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L. Del Castillo works as a Materials Scientist/Engineer in the Electronic Packaging and Fabrication Section at the Jet Propulsion Laboratory. She has been involved in several projects, including the development of a flip chip packaging program, heterogeneous integration of a MEMS neuro-prosthetic system, investigations of embedded passives and lead free solders, as well as MEMS fabrication, including microinductor fabrication and, most importantly, nanosize exclusion chromatograph fabrication. She received her Ph.D. in materials science and engineering from the University of California, Irvine in 2000, where she worked primarily on the development of light-weight, spray-deposited aluminum alloys for aircraft applications.

A. Mehta has over thirty years experience in electronic and electromechanical manufacturing of printed wiring assemblies. Mr. Mehta was responsible for setting up fully automated through hole and SMT lines in several different manufacturing environments—both high volume commercial and medium to low volume high reliability military/aerospace. He also set up and documented assembly processes and carried out continuous process improvements through daily monitoring of yield. He has extensive experience in troubleshooting and solving process problems. He has trained manufacturing engineers and technicians on assembly processes and on equipment operation. In addition, he has actively participated in DfM (design for manufacturability) efforts and enhanced the producibility of products. He has worked for numerous companies, such as Perkin-Elmer, General Dynamics, Western Digital, Interstate Electronics and Xerox. He currently works at the Jet Propulsion Laboratory as a senior engineer where he manages the SMT Laboratory. He is very active in SMTA, and he is the vice president of the LA/OC SMTA chapter. He is a member of the IEEE. He holds a B.S. degree in mechanical engineering from the University of Bombay and an M.S. in mechanics from the State University of New York at Stony Brook.