SEU Mitigation of Xilinx Virtex II FPGAs for Critical Flight Applications

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Abstract

The speed, I/O count, and reconfigurability of SRAM-based FPGAs make them attractive for flight applications. However, critical designs require effective upset. Measurements of the effectiveness of configuration control and TMR during heavy-ion irradiation are reported.

INTRODUCTION

The increasingly advanced technologies of field-programmable-gate arrays (FPGAs) in the commercial sector has resulted in higher speed and lower core voltages, improving both integration and allowing for better power consumption. In addition, the decreasing costs and development time needed to implement FPGAs compared to designs with discrete logic devices has made programmable logic devices favorable in space and avionic applications as well. They offer flexibility for changing requirements, in-system and on-orbit programmability as well as potential recovery of in-flight failures. The Xilinx Virtex II is a re-configurable SRAM-based FPGA that also has the ability to conduct partial configuration or, write to the configuration memory post-configuration while in operation. However, while SRAM-based memory in the FPGA is useful for reconfiguration, the static memory elements and combinatorial logic paths are susceptible to upset from heavy-ion particles in interplanetary space. The Virtex II has been selected for the present study because several variations of the Virtex FPGA are currently or expect to be implemented in various missions. Many studies have been carried out on SRAM-based FPGAs [1]-[4]. They have also shown that with proper mitigation, SEU induced failures can be properly controlled [5]. Static test results on the configuration memory of the Virtex II XC2V1000 along with projected upset rates have been reported at MAPLD, 2002 [6]. These results are used as a comparison and baseline for data collected from two recent mitigated dynamic tests. A future test with an in-depth triple modular redundancy design will be conducted by the Xilinx Consortium, comprised of members from Xilinx, Aerospace Corp., Sandia National Labs, SEAKR Engineering and JPL. Final results will be analyzed and considered for implementation in future space based applications.

EXPERIMENTAL DETAILS

The device chosen for this study is the *Virtex II* XC2V1000. The device was procured in a commercial 256-pin wire-bond standard ball gate array (BGA) package. It is fabricated on a 0.15μm / 0.12μm CMOS 8-layer metal process and includes 40 block RAMs, 432 maximum I/Os, and 4.1M configuration bits. The XC2V1000 is ideal for SEU characterization as it is the only member of the Virtex II family that has a face-up die, suitable for heavy ion penetration.

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Following the static tests on the configuration memory, two basic dynamic tests have been performed to study the behavior of the configuration memory cells while undergoing irradiation with heavy ions. The test vehicle and methodology of the two experiments are identical. Both continuously check for errors but the latter test includes a mechanism to correct the errors as they are detected. The design configured into the DUT is a shift register utilizing a "checkerboard" type pattern. The Virtex II XC2V1000 is chemically etched to expose the die and is situated on a Xilinx development board (Fig. 1). Alongside the XC2V1000 is another FPGA, the XCV100, an on-board service FPGA used to count SEUs and send them to the user interface. Errors in the configuration memory are detected and counted through the use of readback, a feature of Xilinx FPGAs that allow users to read from the memory post-configuration. The number of counts is then sent to a user interface titled Configuration Monitor; a custom Visual Basic program used to configure the DUT as well as record and display the configuration memory upsets as they occur. Once errors are detected, the second test proceeds to correct the upsets through partial re-configuration. This process, also known as "scrub", will cause the configuration memory to be partially re-configured by reloading only the crucial segment of the configuration bitstream [7]. A custom C++ software application was also available at the end of each beam run to read back the number of errors that accumulated in the configuration logic block (CLB) frames, block RAM cells and configuration control registers. The custom software is named FIVIT for Fault Injection Verification Tool and communicates with the device-under-test via the SelectMap or JTAG interface. By combining the efforts and knowledge gained through these initial experiments, the next test will apply mitigation schemes such as triple module redundancy to determine the effectiveness and usage in space.

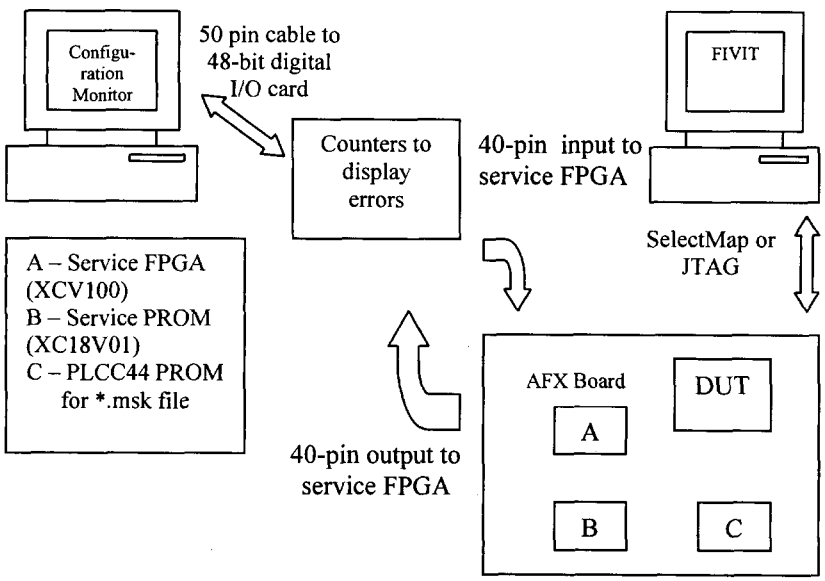


Fig 1. Diagram of dynamic test setup.

TEST RESULTS

A. Dynamic Test

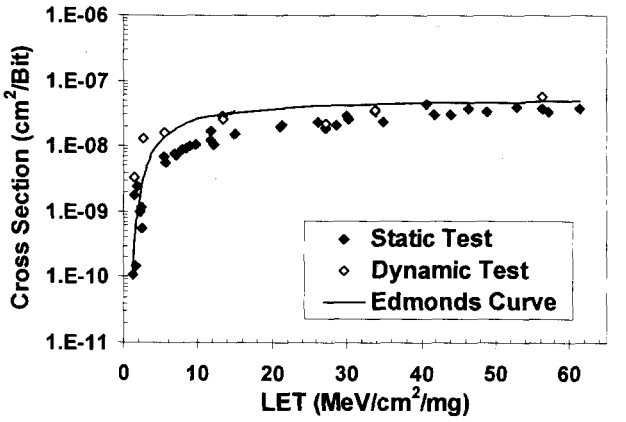
The first of two dynamic tests performed measured and recorded SEUs in the configuration memory and block RAM as they occurred. The final number of errors at the end of a given fluence was used in the upset rate calculations that follow. The configuration memory and block RAM upsets from earlier static tests have been combined and compared with these dynamic results (Fig. 2). From the graphs, very little difference in results is observed between the two tests, verifying the validity of the dynamic test method. Fig. 2 and following graphs are fitted to a physically based model developed by Edmonds [8]. The equation used to fit the data is

$$\sigma = \sigma_{sat} \exp(-(L_{1/e}/LET)) \qquad (1)$$

where σ_{sat} (a fitting parameter) is the saturation cross-section and $L_{1/e}$ (another fitting parameter) is the LET at which the cross section is 1/e times the saturation cross-section. To add a measure of conservatism, the fits have been adjusted upwards slightly to enclose as many data points as possible.

Using the calculated (σ_{sat}) saturation cross- section and $L_{1/e}$ values, upsets rates were calculated for galactic cosmic rays in interplanetary space shielded by 100 mils of aluminum during the solar minimum time period. The rates were calculated using the RPP model to incorporate the response to ions impinging at all angles. An aspect ratio of 1/5 (for lateral dimension to collection depth) was used. Sensitivity analysis showed the result changed only slightly for other assumed aspect ratios. Thus, "cosine law" response gives about the same rates. These upset rates are for heavy ions only and do not account for SEUs resulting from proton radiation.

Fig 2. Cross section vs. LET for configuration and block RAM bits combined. The upset rate for this curve is 5.7E-7/bit-day, slightly higher than the upset rate of 4.4E-7/bit-day for configuration logic block (CLB) frames and 1.1E-6/bit-day for block RAM cells from static test results.

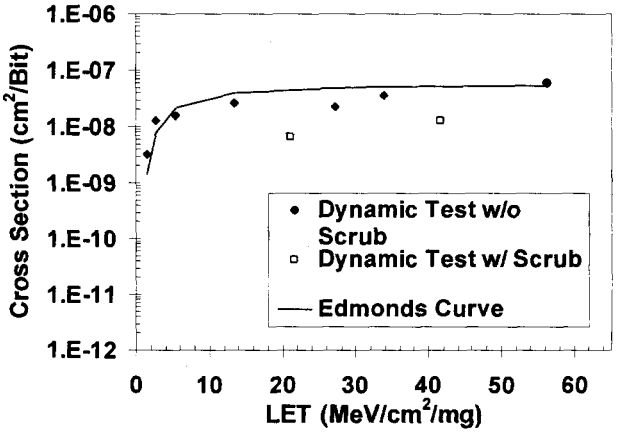


B. Dynamic Test with Partial Re-configuration

The second dynamic test closely mimics the previous test but an algorithm in the service FPGA design enabled scrubbing in the configuration memory as well. Detected upsets were mitigated by reconfiguring the device with the original bitstream at 20 MHz, the maximum allowable frequency set by driver and receiver circuits on the 20 feet cables between the user and the DUT in the ion chamber. The total number of detected

upsets for a given fluence is compared with the previous dynamic test and shown in Fig. 3. This total is also a representation of the number of upsets that would have been accumulated without the continuous scrub. In Fig. 3, the cross section of the second dynamic test is slightly lower than the first, perhaps a result of the low statistical samples obtained. However, it should be noted that the number of upsets at any given time during the experiment was at least two orders of magnitude lower, verifying the efficacy of scrubbing or partial reconfiguration of the device.

Fig. 3. Cross section vs. LET for combined configuration and block RAM bits for both dynamic tests. This graph illustrates the results of scrubbing through the SelectMap interface. Scrubbing through the JTAG interface was also attempted and some attenuation of communication disruption such as a SelectMap or JTAG SEFI was observed.



Two single-event-functional-interrupts (SEFI) were observed, notably, the power-on-reset (POR) and Select Map SEFI. Heavy ions altering the logic states of the power-on-reset circuitry and SelectMap port either disabled the communication between the FIVIT software or reset the device. A re-initialization of the device was needed to bring the device to operational level again. The SEFI results from both the static and dynamic test are compared in Fig. 4 and 5. Although data points for the dynamic test are few, at the LET of 21.1 MeV-cm^2/mg) both POR and Select Map graphs show similar cross sections. This may suggest that mitigated configuration upsets have little effect on the probability of SEFI events, limiting the effectiveness of the mitigation approach.

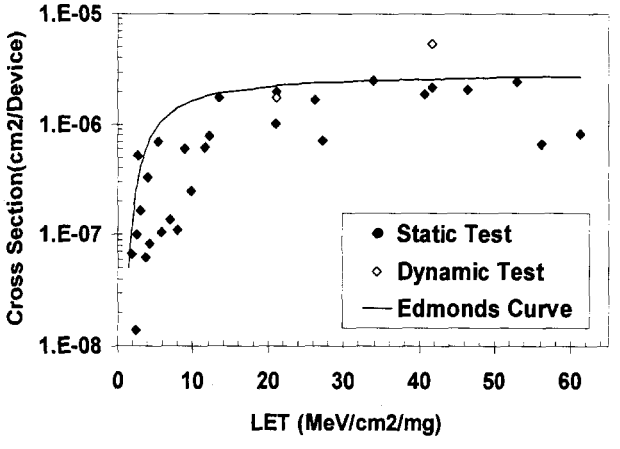


Fig. 4 Cross section vs. Let for Select Map SEFI.

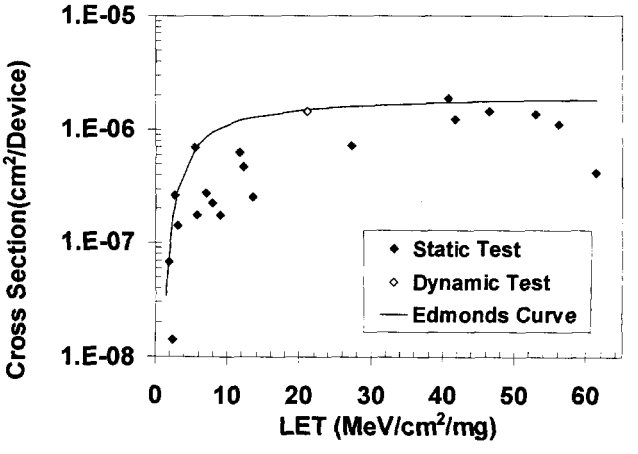


Fig. 5. Cross section vs. LET for POR SEFI.

CONCLUSION

The cross-section results from both static and dynamic tests for configuration memory are in agreement with each other, demonstrating a valid dynamic test vehicle for mitigation of SEU induced faults in the configuration memory. In addition, SEU in the configuration memory and block RAM seem to be alleviated by at least two orders of magnitude through the use of partial reconfiguration or scrubbing in the second dynamic test. SEFI data however, seem unaffected by enabling scrub but more data over a wider span of LETs is needed to fully corroborate the initial tests. A test has been planned for further dynamic testing of the Virtex II with the objective to incorporate triple module redundancy (TMR) within a user design with previous partial reconfiguration capabilities to make this device radiation-hardened for space usage. This data will be included in the final version of the paper.

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