

The Single Hard Error Mechanisms and Response in SDRAMs

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Abstract

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The phenomenon of stuck bits in SDRAMs are studied. Previous work demonstrated this effect is linear with fluence, and is due to reduction in RC time constant of stuck cells. Particular emphasis is placed on variations in cell structure that affect sensitivity. The exact mechanism of a stuck bit is predicted.

INTRODUCTION

As integrated circuit technology continues to scale toward higher density, small volume radiation effects will present an ever-growing problem. The feature size of memory has passed below the radius of charge generated so that effects to the whole bit or multiple bits become a certainty. SRAM and DRAM technologies are equally problematic due to the smaller amount of charge required to maintain the bit information. Since SDRAM is one of the smallest current memory technologies, it should be the most vulnerable. Small volume radiation effects, specifically SEE and microdose, have been and will be a major radiation issue for SDRAMs.

Stuck bits have been studied in various contexts and approaches [1-11]. The linear response of stuck bits with fluence for initial stuck count has been demonstrated [1-3]. Previous to that relationship between RC time leakage failure and microdose was examined [4-6] and Duzellier et al. described stuck bits as a function of total dose [7-11].

This paper investigates the dominant mechanism of the stuck bit. The issue of whether the gate oxide or storage capacitor oxide is the dominant function is examined. In addition to ion LET dependence, the various modes of operation of the SDRAM will be examined to determine the most vulnerable conditions in various space environments.

THEORY

To analyze the device physics of single hard errors (SHE) in SDRAMs, several SEM images were taken of the devices. The 256Mb Samsung device, and the 256Mb IBM-Toshiba-Seimens devices were both prepared and imaged in a similar way. A single cut was made off of a major axis, to be able to see structural features of both axes in the SDRAM's rectangular cell.

Figure 1 shows the cross section of the Samsung device. The structure is stacked to provide headroom for future scaling and has been discussed elsewhere [12]. For this study the primary emphasis is on the geometric layout. For this device the capacitor is a short tube above, and the access transistor is buried underneath.

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In contrast to the Samsung device, the IBM-Toshiba-Seimens SDRAM uses large aspect ratio trench capacitors that are underneath the access transistors. Figure 2 contains the SEM image of this device. The capacitor is about 300nm wide, and 6um deep. This structure is one of the common cell designs from the 64Mb generation [13].

Given the extreme architecture of a modern SDRAM cell, the charge deposition function is expected to be highly dependent on irradiation conditions, including LET charge profile, angle of incidence, and electric field. A SHE hard error in a SDRAM exhibits a significantly reduced retention time of the of the capacitor-resistor circuit that makes up the SDRAM bit. Explicitly,

$$t_R = RC \quad (1)$$

where R is the effective leakage resistance of the MOSFET channel and C is the capacitance of the storage capacitor. A reduction in either the capacitance or the resistance of the will reduce the retention time. If the retention time is reduced below the refreshed time set by the SDRAM, an error will occur. Both the capacitor and the transistor exhibit lingering effects from ion hits and, therefore, will contribute to a SHE in an SDRAM.

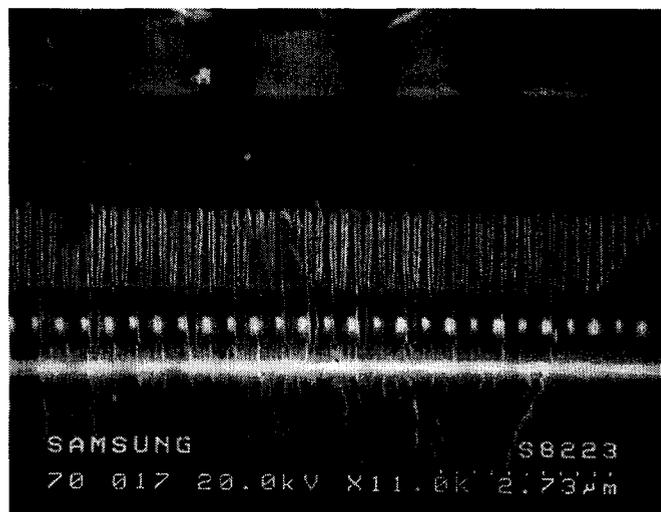


Figure 1a. SEM cross section of the Samsung SDRAM.

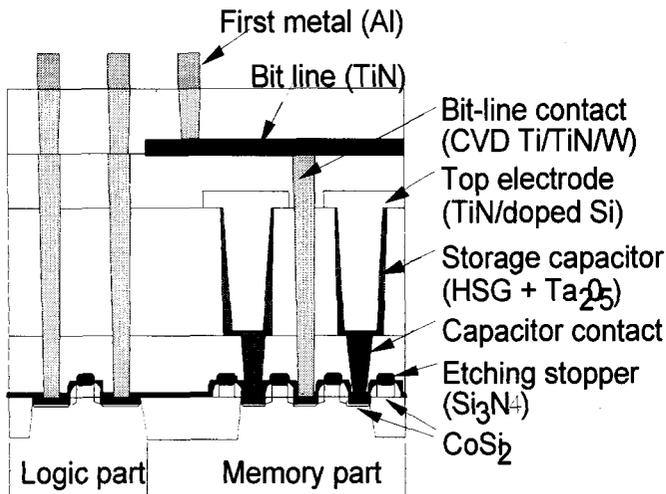


Figure 1b. Graphic cross section of the Samsung SDRAM.

The access transistor in an SDRAM is typical of a CMOS or NMOS technology transistor. Radiation will affect both the thin gate oxide and the field oxide, especially around the bird's beak structure. The current, and therefore the resistance, is given by

$$I_{DS} = \frac{\mu CW}{L} \left((V_g - V_t) - \frac{m}{2} V_{DS} \right) V_{DS} \quad (1)$$

V_g , V_t , and V_{DS} are the gate, threshold, and drain source voltages, respectively. μ , C , L , W , and m are constants set by device design. Due to the multiple volumes of oxide in these transistors that retain charge after irradiation, it not currently know what ionization effect causes the increase leakage. In any case, the following basic model given below should apply:

$$\Delta V = \frac{Q_{trapped}}{C_{ox}} \quad (2)$$

$Q_{trapped}$ is the trapped charge, and C_{ox} is the capacitance of the oxide. But the voltage shift introduced in Eq. 2 will not be typical of irradiated MOS capacitors. Indeed, charge trapping and recombination effects will depend greatly on the location of the ion strike in the access transistor. Ma and Dressendorfer discuss this directly as being the high-density limit of the ion strike charge deposition profile. This is referred to as the columnar model and is described by the diffusion equation. No solution currently exists for the complex boundary conditions given by the gate oxide to bird's beak to field oxide transition regions.

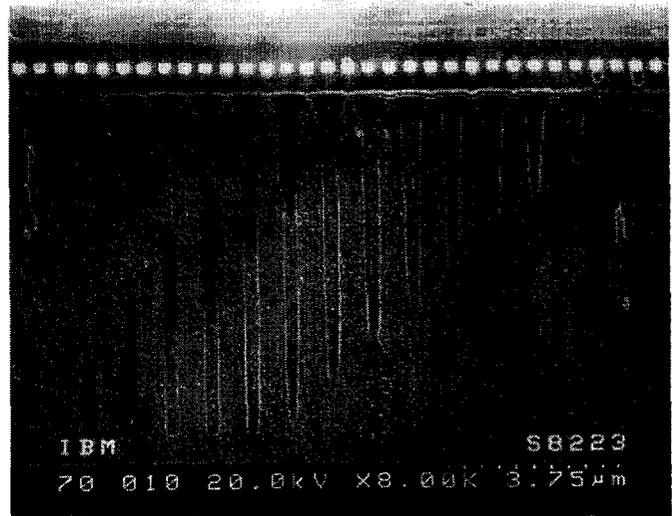


Figure 2a. SEM cross section of the IBM SDRAM.

Because of the large aspect ratio, the capacitor structure will be described by a different set of boundary conditions and effects. The vertical architecture of the SDRAM capacitor presents a steep field gradient not present in most other devices. The charge trapped during an ion strike will depend on both the presence of a field across the capacitor and the angle of incidence. One assumption is that the oxides in the SDRAM capacitor are thin enough that charge injection from an ion strike can be considered a perturbation to the steady state solution of the diffusion equation. If that is the case,

$$Y(E) = \left[1 + \left(\frac{\pi}{2} \right)^2 \frac{N_0 q}{4 \epsilon \epsilon_0 b E \sin \theta} \right]^{-1} \quad (3)$$

should apply concerning the yield of the recombination [10]. In Eq. 3, N_0 and b are factors of a gaussian profile used to describe the initial charge density of the track. Also, a modified cosine law should apply to deposition in the capacitor due to its large aspect ratio. That is, the energy deposited in the structure goes as the \sin^{-1} of the angle of incidence since path length is reduced for off-axis strikes. This means that a SHE in a SDRAM due to damage in the capacitor should be strongly dependent on angle.

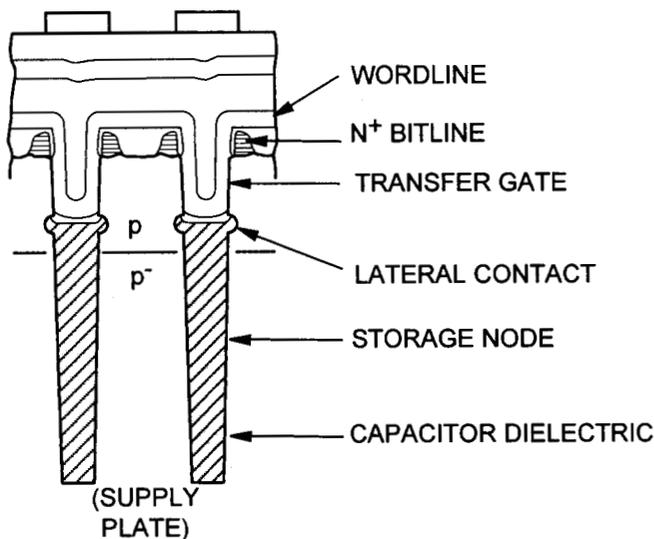


Figure 2b. Graphic cross section of the IBM SDRAM.

The long aspect ratio of the stage capacitor in a SDRAM cell also indicates that the range of the ion, due to the both angle and energy, will effect SHE phenomena. The range of an ion follows from the definition of LET:

$$L = \frac{1}{\rho} \frac{dE}{dx} \text{ or } R = \int_{E_i}^E \frac{1}{\rho L(E)} dE. \quad (4)$$

Three important effects can be inferred from Eq. 4 for the SDRAM vertical capacitor structure. First, since LET varies quadratically with atomic weight, particles with equivalent ranges but different atomic weights should damage bits as a function of the square of the atomic weight. Second, since the end of range of ions can be tuned fairly well, irradiation with ions at different energies, should produce measurable effects since ions at the end of range are very damaging. Third, since the effective range of an ion depends on its angle, angles that cause an ion to stop in the capacitor "forest" will induce effects at very small angular changes.

One important condition for an ion experiment for SHE in SDRAMs is highlighted by the SEMs images shown above. The IBM has its access transistors between the storage capacitors and the device surface while in the Samsung device the opposite is true. This allows the segregated irradiation of device structures in both types of DUTs. That is, the access transistor or the storage capacitor can be irradiated without irradiating the other.

SHEs in SDRAMs generally have been described in the same terms as SEUs in SDRAMs. This is conceptually valid except for one difference between the two phenomena. SEU are transitory and deal with charge collection in a few microseconds in a reverse biased diode structure. SHE phenomenon is a dose effect on a very small scale and the charge is trapped, not collected. This contrast begs the question whether or not a critical charge concept is reliable for SHE. If an SHE requires a critical charge before an SHE occurs, then the SHE cross section should be linear with LET. Earlier studies on DRAM retention time, however, have shown that the magnitude in shifts in retention time are not clearly linear with LET [3,11].

SETUP AND PROCEDURE

The test equipment was comprised of two PCs, a power supply, and a specially designed test board. A dedicated PC controlled the test circuit board designed specifically for SDRAM testing. The address of a failure and the value at that address were recorded in a file for each run, allowing for any structure in the SEEs or predilection for certain pattern failure or type of SEU to be observed. Operational mode testing was done at Brookhaven National Laboratory. The SDRAMs used there were 256 Mbit Samsungs. The devices were exposed to radiation by milling all but 100 microns of packaging and silicon from the back of the device. This allowed for lighter ions at Brookhaven to reach the sensitive volume of the SDRAMs. Additional testing has been done with the Samsung device type as well as a IBM-Toshiba-Seimens 256 Mb device. Some of the additional testing was carried out at JPL, though it is not directly reported on here.

The time between refresh commands of a SDRAM cell is a key metric in the stuck bit phenomenon. If a SDRAM is allowed to sit idle for a time much longer then the specified maximum refresh time, the bits of the SDRAM will drain into the relaxed state. This pattern generated by the un-refreshed SDRAM is immune to SEU since the un-refreshed bits will only upset into this pattern [11]. This is called the "bleed down pattern." The inverse is loaded for SEU tests to get maximum response, which is an important factor to monitor during any single event studies in SDRAMs.

Previous studies have been inconclusive concerning the part-to-part variation of the response of stuck bits []. To assure consistency, each device is used as its own control by establishing a baseline with one set of operational parameters. In this case, it was an inverse bleed down pattern of midrange refresh time. After the typical linear trend for the part is established, the part is exposed with one operational parameter changed. The device is read out for stuck bits in the same manner as the baseline, but only during the exposure are operational parameters changed. Operational modes that were tested were no refresh at all (to augment field across the channel), ultra fast refresh (to augment gate field), and device off (to disregard fields).

RESULTS

The first radiation data comes from the Samsung device. It is the result of varying bias conditions on the cell structure, and looking for the effect on stuck bit susceptibility. The fact that radiation sensitivity can vary widely on commercial parts required the use of each DUT as its own control. The control condition was chosen to be the stuck bit sensitivity at 4s refresh interval at room temperature while the device was programmed with its "inverse bleed down" pattern.

The radiation data presented here is from separate sample DUTs for each bias condition. The data was taken between irradiations with 1.4 LET (MeV-cm²/mg) Carbon at Brookhaven National Laboratory.

The first condition shown here is the reduction of the refresh interval. The first 1.5x10⁹ cm⁻² particles established the control response. Then the device was programmed at the maximum speed of the test apparatus. This condition kept the stored charge in the cells as high as possible, and hence the differential bias conditions as high as possible. The response is plotted in figure 3, and shows that the shortened

refresh interval results in a higher susceptibility for stuck bits.

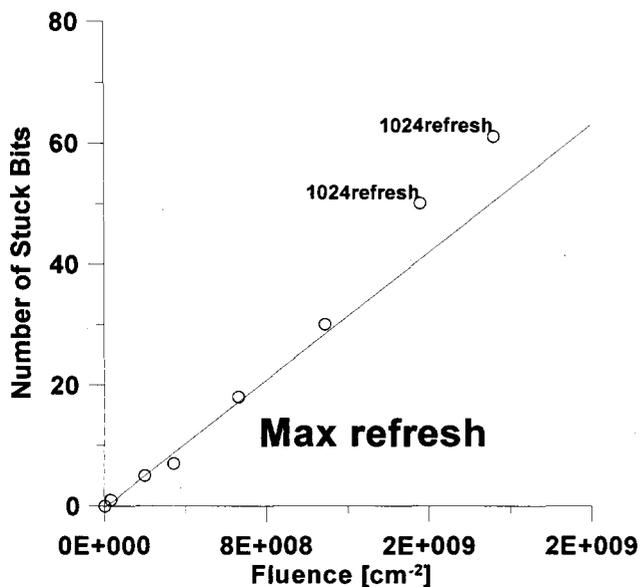


Figure 3. Stuck bit dependence on increased cell bias.

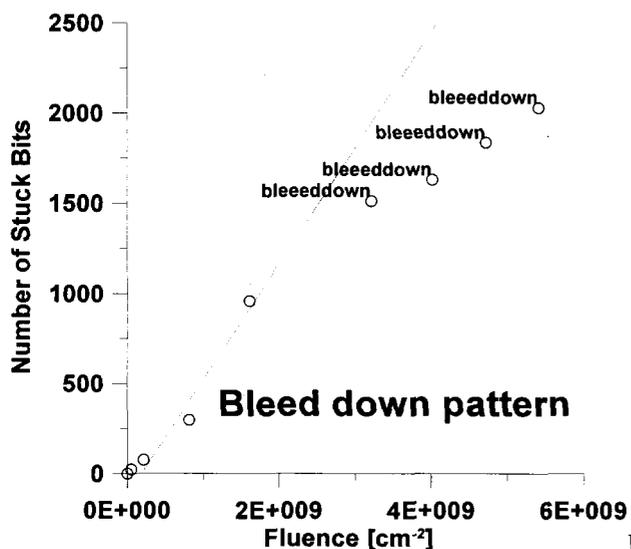


Figure 4. Stuck bit dependence on inverting cell bias.

Another condition tested was to invert the bias on all the cells. Any bit that was programmed as a "1" in the control setup would be programmed to "0" in the modified setup. This doesn't guarantee a particular bias, but it does guarantee inversion of the bias. The test control was again established with the first 1.5×10^9 cm² of Carbon. The results are in figure 4. The trend, with inverted bias, is lower stuck bit sensitivity.

The result of the final bias condition presented here is shown in figure 5. The device was simply left unpowered in the non-control irradiations. Here the control is the first 7×10^8 cm² particles. The device shows an increase in stuck bit sensitivity.

Preliminary work has studied the relationship between stuck response and LET. The stuck bit response of the devices to different LETs has observed, but not rigorously

studied. Anecdotal results show that stuck bits are linear with LET, and have about four orders of magnitude difference between sensitivity at LET=1 MeV-cm²/mg, and LET = 100 MeV-cm²/mg. This information will be expanded, for the involved DUT types, in the full paper.

Due to the nature of the anecdotal evidence introduced above, radiation testing with alpha particles has been done at JPL. This testing was done using a Po-208 source with air as a degrader. Investigating the stuck bit response as a function of alpha penetration depth has led to some evidence of varying sensitivity as a function of depth on the Samsung device. The IBM-Toshiba-Seimens device has not been tested. The preliminary results show very good evidence for stuck bits as a result of alpha irradiation. The first order cross section for stuck bits with alpha particles is 3×10^{-5} cm². More data on alpha susceptibility will be developed for the full paper.

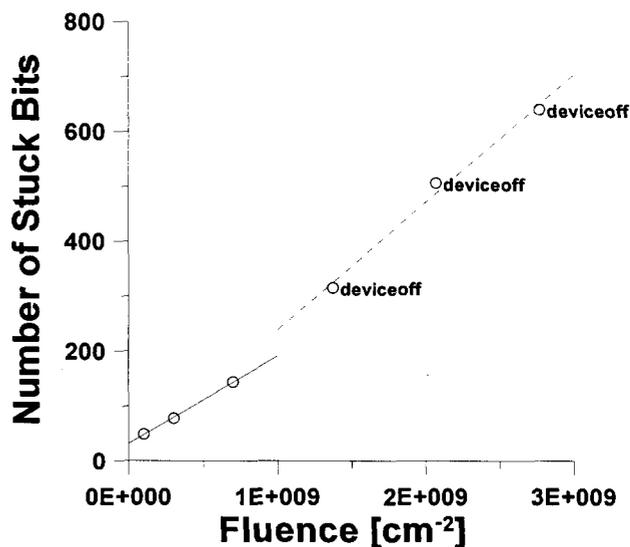


Figure 5. Stuck bit dependence on device power status.

DISCUSSION

The data presented demonstrates the relationship between bias conditions and stuck bits in a qualitative way. Increasing the bias results in more stuck bits, due to greater charge separation. Removing the bias results in more stuck bits. But inverting the field results in fewer stuck bits. With the proper assumed conditions on the components of each cell, these results should be consistent.

The stuck bit dependence on LET is important in two ways. (1) Stuck bits are present at LETs below the threshold for upsets. This can sometimes cause problems because stuck bits that anneal quickly can appear to be single bit upsets. (2) Stuck bit linearity with LET would lead to better understanding of the dose mechanism involved.

However, logical storage to actual bias conditions are not readily available. The data so far are not complete enough to make a full connection between the cell structure, the stuck bit, and the biases applied. These will be connected for the full paper. Experiments exploring energy, range, and angular effects will be carried out for the full paper. These

experiments will be matched with modeling using the ISE code on the device structures found through the SEM photos, which will provide the link necessary to isolate the source of stuck bits.

CONCLUSION

The phenomenon of bits that will not reprogram is seen to depend on the operational mode in which the device is run during irradiation with heavy ions. Stuck bits are seen to have very low thresholds, and their cross sections are linear with LET. Stuck bits are expected to be a result of SDRAM cells that have retention shorter than the refresh interval of the device. The full paper will investigate the exact radiation effects and mechanism of the stuck bit for other bias conditions as well as different LETs, since the varying track structure will allow for small volume effects associated with stuck bits.

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