

On-chip Evolutionary Synthesis of Reconfigurable Analog Computing Circuits

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Abstract

The paper presents a Field Programmable Transistor Array (FPTA), developed as an experimental platform for implementing flexible, reconfigurable analog computing. Parasitic effects of imperfect switches interconnecting transistors deteriorate the performance of conventional designs when mapped to the FPTA. However, working design solutions can be obtained through a search procedure guided by evolutionary algorithms. An example of evolutionary design is illustrated using a stand-alone board-level evolvable system (SABLES) in which the evolutionary algorithm is implemented with a DSP. SABLES can automatically configure the FPTA in tens to hundreds of seconds, time in which evaluates ~100,000 circuit candidate solutions. The paper details several examples of evolutionary synthesis of analog circuits on the FPTA. Evolved circuits include rectifier circuits, reconfigurable analog filters and reconfigurable fuzzy logic circuits.

1. Introduction

Analog circuits refuse to disappear under digital takeover attacks – in fact, analog is making a comeback propelled by recent imperative needs for lower power and higher speed solutions. As with digital, great benefits could be obtained from being able to reconfigure the analog hardware, for total change of function or for adaptation. This paper presents ideas on reconfigurable analog computing, and supports them with experiments on a device reconfigurable at transistor level, which can map both analog and digital circuits. The particular implementation of a desired functionality is determined through an evolutionary algorithm-driven search, in which candidate designs/configurations are downloaded to the chip, and the response of the chip is measured and evaluated. A stand-alone board-level evolvable system (SABLES) built at JPL integrates a Field Programmable Transistor Array in which the analog circuits can be configured and a DSP which implements the evolutionary algorithms. SABLES can automatically reconfigure the FPTA and evaluate candidate designs hundred of thousands of times in tens to hundreds of seconds. SABLES achieves approximately 1-2 orders of magnitude reduction in memory and about 4 orders of

magnitude improvement in speed compared to systems evolving in simulations, and about 1 order of magnitude reduction in volume and 1 order of magnitude improvement in speed (through improved communication) compared to a PC controlled system using the same FPTA chips. Details of SABLES appeared in [2].

The paper is divided in five sections. Section 2 describes the reconfiguration mechanism for circuit evolution. Section 3 overviews the components of SABLES, including the FPTA-2 chip and the DSP system. The evolution of a half-wave rectifier circuit is presented to illustrate how the system functions. Section 4 describes other reconfigurable analog circuits synthesized through evolution, such as filters and fuzzy logic circuits. Section 5 concludes the work.

2. Reconfiguration Mechanism

The idea behind evolutionary circuit synthesis/design and Evolvable Hardware (EHW) is to employ a genetic search/optimization algorithm that operates in the space of all possible circuits and determines solution circuits that satisfy imposed specifications, including target functional response, size, speed, power, etc.

The genetic search in EHW is tightly coupled with a coded representation that associates each circuit to a “genetic code” or chromosome. The simplest representation of a chromosome is a binary string, a succession of 0s and 1s that encode a circuit. However, circuits can also be represented using integer or real strings, or parsing trees [6]. First, a population of chromosomes is randomly generated. The chromosomes are converted into circuit models and their responses are compared against specifications, and individuals are ranked based on how close they come to satisfying them. In preparation for a new iteration, a new population of individuals is generated from the pool of best individuals in the previous generation. This is subject to a probabilistic selection of individuals from a best individual pool, followed by two operations: random swapping of parts of their chromosomes, the *crossover* operation, and random flipping of chromosome bits, the *mutation* operation. The process is repeated for several generations, resulting in increasingly better individuals. Randomness helps to avoid getting trapped in local optima. Monotonic convergence (in a loose Pareto sense) can be forced by unaltered transference to the next generation of the best individual from the previous generation. There is no theoretical

guarantee that the global optimum will be reached in a useful amount of time; however, the evolutionary/genetic search is considered by many to be the best choice for very large, highly unknown search spaces. The search process is usually stopped after a number of generations, or when closeness to the target response has reached a sufficient degree. One or several solutions may be found among the individuals of the last generation.

3. SABLES

SABLES integrates an FPTA and a DSP implementing the Evolutionary Algorithms. The FPTA has transistor level reconfigurability, supports any arrangement of programming bits without danger of damage to the chip (as is the case with some commercial devices). Three generations of FPTA chips have been built and used in evolutionary experiments. The latest chip, FPTA-2, consists of an 8x8 array of reconfigurable cells. Each cell has a transistor array as well as a set of other programmable resources, including programmable resistors and static capacitors. Figure 1 provides a broad view of the chip architecture together with a detailed view of the reconfigurable transistor array cell. The reconfigurable circuitry consists of transistors connected through switches and is able to implement different building blocks for analog processing, such as two- and three-stage OpAmps, logarithmic photo detectors, or Gaussian computational circuits. It also includes capacitors and programmable resistors. Details of the FPTA can be found in [5].

The evolutionary algorithm was implemented in a DSP that directly controlled the FPTA, together forming a board-level evolvable system with fast internal communication ensured by a 32-bit bus operating at 7.5MHz. Details of the EP were presented in [2]. Over four orders of magnitude speed-up of evolution was

obtained on the FPTA chip compared to SPICE simulations on a Pentium processor (this performance figure was obtained for a circuit with approximately 100 transistors; the speed-up advantage increases with the size of the circuit). The evaluation time depends on the tests performed on the circuit. Many of the evaluation tests performed required less than two milliseconds per individual, which for example on a population of 100 individuals running for 200 generations required only 20 seconds. The bottleneck is now related to the complexity of the circuit and its intrinsic response time. SABLES fits in a box 8" x 8" x 3".

The following experiment illustrates an evolution on SABLES. The objective of this experiment is to synthesize a half-wave rectifier circuit. The testing of candidate circuits is made for an excitation input of 2kHz sine wave of amplitude 2V. A computed rectified waveform of this signal is considered as the target. The fitness function rewards those individuals exhibiting behavior closer to target (using a simple sum of differences between the response of a circuit and target) and penalizes those farther from it. After evaluation of 100 individuals, they are sorted according to fitness and a 9% portion (elite percentage) is set aside, the remaining individuals undergoing first crossover (70% rate), either among themselves or with an individual from elite, and then mutation (4% rate). The entire population is then reevaluated. In this experiment only two cells of the FPTA was allocated.

Figure 2 displays snapshots of evolution in progress, illustrating the response of the best individual in the population over a set of generations. The first caption shows the best individual of the initial population, while the subsequent ones show the best after 5, 50 and 82 generations. The solution, with a fitness below 4,500 is shown on the right.

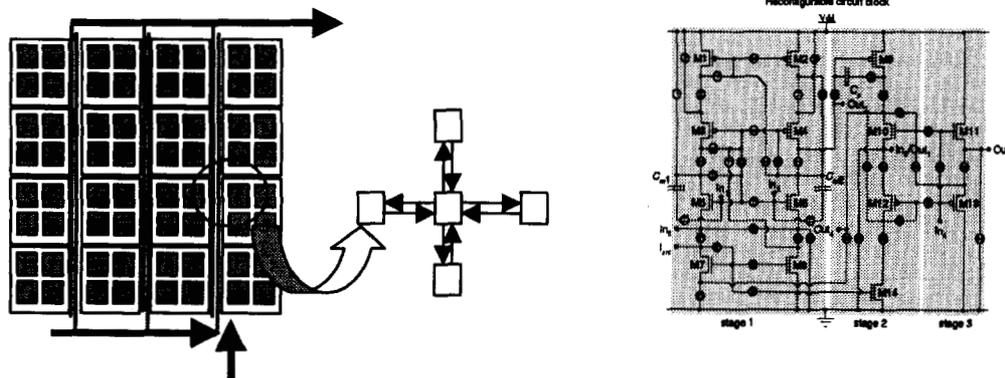


Figure 1. FPTA 2 architecture (left) and schematic of cell transistor array (right). The cell contains additional capacitors and programmable resistors (not shown).

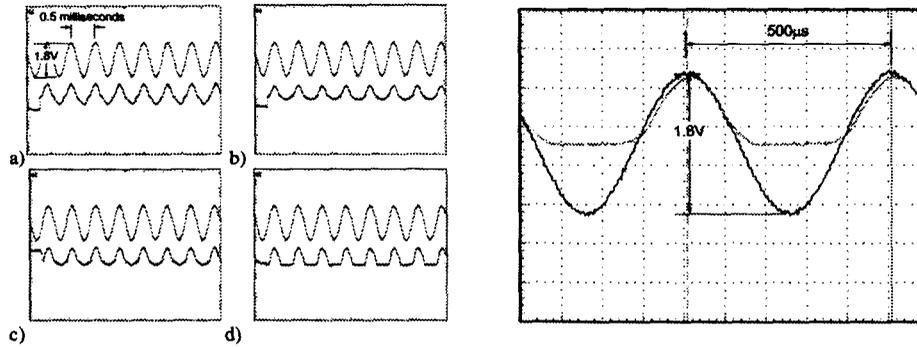


Figure 2. Evolution of a halfwave rectifier showing the response of the best individual of generation a) 1, b) 5, c) 50 and finally the solution at generation d) 82. The final solution, which had a fitness value less than 4500, is illustrated on the right.

4. Other reconfigurable analog computing circuits obtained by evolution

The Field Programmable Transistor Arrays are devices on which one can program circuits at the lowest granularity and achieve the highest control of the topology, i.e. by reconfiguration at the transistor level. An example of a reconfigurable multi-functional circuit mapped on programmable array is shown in Figure 3, where it is shown the response of narrow band-pass filters with center frequencies at different locations (5 and 25kHz). The reconfigurable circuit can map a variety of filters. Evolution is used to synthesize several filters based on the same set of available resources. An extra optimization step that can be added is to minimize the number of architectural changes, i.e. the number of switches needed to be changed from topology to another. This would reduce the time to reconfigure since usually the bits are changed serially (at least for larger devices) or in clusters (which can be the subject of minimization procedure as well). As shown in Figure 3, the reconfigurable chip used in this experiment is an earlier version than the FPTA-2 shown in Figure 1, with a smaller number of switches per cell [4].

From the perspective of fuzzy computational platforms, these devices are versatile/malleable architectures on which one can rapidly instantiate the desired fuzzy circuitry. Second, these are adaptable and can be used to implement systems that change the operators from one processing stage to the other; i.e. one can start with MIN-MAX logic and change later to another as needed. Third, the FPTA are platforms for fuzzy configurable computing in the same way FPGAs are for conventional/digital computing. In an ASIC version the whole processing described by an algorithm is mapped at once in a fixed circuitry, with building blocks corresponding to various stages of the algorithm. In an FPGA / FPTA implementation, only a part of the algorithm is mapped first in an instance of the processing machine, after which the chip reconfigures itself to become the blueprint for the next step, and so on. The fourth aspect is related to the use of FPTA to evolve fuzzy circuits directly in hardware. This not only is rapid, but also real, i.e. valid without doubts, unlike the case of evolution in simulations which may lead to results that may differ when tested in reality due to modeling approximation and fabrication effects. In other words evolution on real chips takes in

consideration and adapts to account for effects of fabrication, temperature of operation, etc.

Evolutionary algorithms (EA) have proven to be powerful search mechanisms able to automatically find novel circuits / topologies that satisfy desired functional and implementation / efficiency-related requirements. In particular EA can be applied to determine circuits that implement operators such as conjunctions and disjunctions modeled by triangular norms, which is a central element for fuzzy systems.

While circuits implementing simple t -norms / co-norms, such as min, max, product and probabilistic sum, have been explored quite early, more complex t -norms, such as parametric t -norms (e.g. Frank's t -norms explored in [1]), while shown valuable both in theoretical studies as well as in practical applications (such as in the fuzzy controllers by Gupta *et al.* in the early 90s, see [3]) are still lacking circuit solutions. The reasons are that such circuits (referring here to analog circuits – computing the functions digitally or storing tables in memory being computationally expensive solutions in terms of power / time / area of silicon) are hard to design. Each such circuit would practically mean a new patent, and one may need many of them, one for each value of the parameter of the t -norm (unless of course one designs a parametric circuit, which would be an even harder task).

Evolutionary techniques have proven efficiency (and proficiency) in creating such new designs for implementation of parametric t -norm circuits. Several such circuits are presented in [4] and will we show here for illustration the evolved circuit for a t -norm with $s=100$ (Figure 4) and its response (Figure 5).

5. Conclusions

This paper presented an analog device reconfigurable at the transistor level, demonstrating that it can be used to synthesize a variety of analog circuits, such as multi-functional filters and circuits for Fuzzy Logics. Additionally the paper presented a stand-alone board-level evolvable system (SABLES) and illustrated its performance with the evolution in seconds of a halfwave rectifier circuit. To date this is the fastest, most flexible and most compact stand-alone evolvable system for both analog and digital circuits.

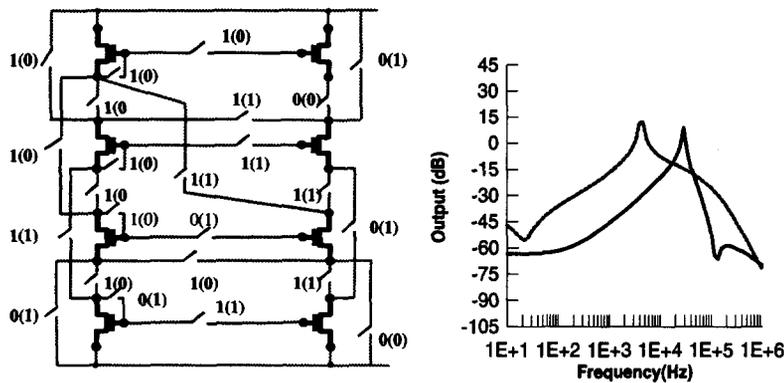


Figure 3. Filter on re-configurable circuit. Simplified architecture at the left and response at the right. (capacitors omitted in the figure). The binary state of the switches is represented next to the respective switch for the two filters, filter 2 between brackets. Filter 1 presents a gain of 11dB at 5kHz and roll-off about -30dB/dec . Filter 2 presents a gain of 9dB at 25kHz and roll-off about -40dB/dec for the lower band and -70dB/dec for the upper band.

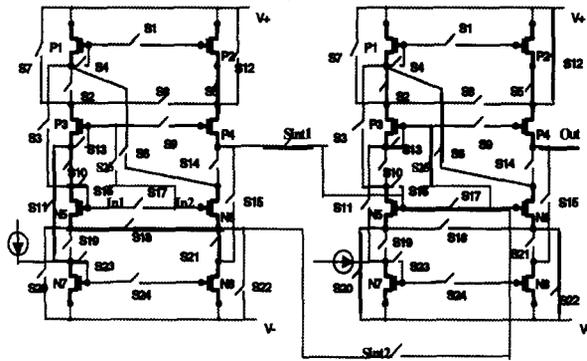


Figure 4 Evolved circuit implementing the fundamental T-norm for $s=100$ (with the response in Figure 5).

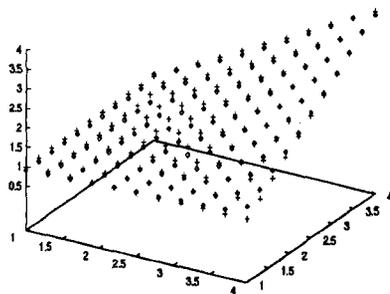


Figure 5 Response of a circuit implementing the fundamental T-norm for $s=100$ (\circ). Target characteristic shown with (+).

6. Acknowledgements

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8. Bibliography

Adrian. Stoica received his PhD in Electrical Engineering and Computer Science from Victoria University of Technology, Melbourne, Australia. He is currently the Principal Investigator for several tasks on evolvable hardware. His interests include adaptive and learning hardware for autonomous systems. He received the Lew Allen Award for his research in evolvable hardware.