

# X2000 Advanced Avionics Project

## Development of a New Generation of Avionics for Space Applications

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*Abstract*—The X2000 Advanced Avionics Project has developed a new generation of avionics building block modules for use by multiple deep space missions, including future missions to Europa, Mars, and a comet. The key developments of the X2000 Avionics are a high performance flight computer, solid-state mass data storage, high-speed system I/O, solid-state power distribution, and power regulation and conversion. These components enable a modular and scalable design approach that results in a wide variety of avionics system architectures to meet diverse mission requirements and environments. The X2000 Avionics have been developed for use in extreme radiation environments such as those at Jupiter. The use of commercial standard interfaces and buses throughout the X2000 Avionics allow system designers to add functionality and further customize spacecraft architectures. This paper will describe the system architecture, the avionics components, the key performance and reliability requirements, and the current development status of the X2000 Avionics.

### 1. INTRODUCTION

Starting in 1997, NASA's Outer Planets Program initiated the development of a new generation of complete avionics building block modules for use by multiple deep space missions, including planned missions to Europa, Pluto, and Mars. This general-purpose avionics system architecture is defined by the following driving attributes:

*Next generation flight computer technology module*—NASA has traditionally been on the forefront of developing single board flight computers. Notable examples developed for space applications are:

Cassini GVSC 4-chip CPU flight computer using 80 s technology

Mars Pathfinder: RAD6000, VME single board flight computer 90 s technology

X2000: PowerPC 750 or RAD750, CompactPCI (3U) single board computer 2000 technology

*Use of exclusively commercial (COTS) interfaces and buses*—A broad survey conducted in 1997-98 led to the selection of several commercial interfaces that currently define the X2000 architecture, including a high performance local computer bus (PCI), a scalable high performance serial bus, (IEEE-1394), and low power, low performance bus, I<sup>2</sup>C. All interfaces are taken at their logical level and then implemented at the physical level using technologies that are resilient to space environments.

*Modular and Scalable Design Approach*—As a general-purpose architecture, X2000 had to address the various needs of multiple missions. Thus, the design had to be modular and scalable in multiple ways. The high-performance serial bus, 1394a at 100 Mbps, is two orders of magnitude higher in performance compared to the current technology commonly in use, the MIL-STD-1553 bus at 1 Mbps. This high-speed bus allows multiple computers and scientific instruments to connect into a single local area network. Moreover, the commercial standard PCI bus provides another dimension of scalability within a local computer node. The basic configuration of a computer node consists of a Single Board Computer (SBC), a Non Volatile Memory module (NVM), and a System I/O module (SIO). However, one easily inserts additional memory modules, SBC, or I/O modules to the PCI Bus to expand the capability of the computer node. In the Power Subsystem Electronics (PSE), the number of switching elements per load, pyrotechnic firings and valve drivers can be scaled depending on mission needs. The switching elements can be distributed or centralized and can switch voltages between 0 and 40V. Moreover, the PSE has the capability to add slices to increase the total number of power switches, which can be added in groups of 16 per slice. All PSE slices use the same system I<sup>2</sup>C data bus, which facilitates the addition of more slices.

*Avionics Integration*—Advanced miniaturization of all spacecraft subsystems has always been seen as an essential enabling aspect for deep space exploration. Advanced avionics integration of all avionics elements into an integrated packaging and assembly approach has been an important element of X2000. Whereas new innovative (and non-standard) approaches were designed, developed and qualified by X2000, eventually, a less ambitious but standard approach to avionics integration was chosen, based on the CompactPCI mechanical standard. The fully integrated, dual redundant computer subsystem for a Europa mission includes a total of 17 3U-cards. A fully redundant power subsystem for the Europa Orbiter mission, which includes functionality for firing pyros and driving valves, occupies 31 3U-cards.

*Advanced Power Electronics*—In addition to developing new digital avionics components and modules, X2000 has focused on the development of power electronics, mixed-signal and power ASIC technology, power management and switching modules. New packaging technology is also used here to increase the density of the units. The dual switching elements are packaged individually and act as independent circuit breakers for each load. The Power Switch Slice (PSS) contains sixteen of these switching elements. The PSS provide telemetry and fault protection for each load and is also designed to actuate valves and fire pyrotechnic devices. The Power Control Slice is a slightly modified version of the PSS that is designed to provide regulation of the primary power bus.

*Power Aware System Design*—The architecture allows system components to be powered off whenever they are not needed. Computer or controller nodes on the 1394 bus can be turned off without affecting the communication of the other nodes through the bus. If it is necessary, the nodes of an entire section of the 1394 bus can be put into a sleep state. Redundant data buses can be turned off without noticeable effect on the fault detection and recovery.

*Exploration of Extreme Radiation Destinations*—The major driver for X2000 environmental requirements was the exploration of Jupiter's moon Europa, which has a very severe radiation environment. This requirement has been the primary consideration in the selection and qualification of components and the choice of semiconductor technologies that are able to tolerate Single Event Effects (SEE), and large Total Ionizing Dose (TID). For commercial components that can not tolerate large exposures to ionizing dose, radiation shielding techniques have been developed and implemented.

*Scalable and Distributed Architecture*—One of the early objectives of X2000 was to enable a highly distributed and symmetric architecture that allows for scalability and thus be applicable to other missions that have various performance requirements. The selection of the 1394 bus enables multiple computer nodes to be connected in a distributed fashion. Whereas other buses can be used as well, at the time, 1394 had the best power to bandwidth ratio, and also is a growing commercial standard as well. In a similar approach, the lower power and lower bandwidth, fully redundant I<sup>2</sup>C data bus provides access to all of the PSE slices from any computer node.

## 2. X2000 COMMAND AND DATA HANDLING SUBSYSTEM ARCHITECTURE

The X2000 Command and Data Handling (CDH) subsystem architecture is a distributed, symmetric system of multiple computing nodes and devices that share a common redundant bus architecture. All of the buses used in the X2000 architecture are based on commercial standards. The local computer bus in each node is the Peripheral Component Interface (PCI) bus. Interconnects between computing nodes are made with the system buses, the IEEE 1394 bus and the I<sup>2</sup>C bus. There is an additional, separate "subsystem" I<sup>2</sup>C bus for sensors and instruments control. The X2000 avionics architecture is shown in Figure 1.

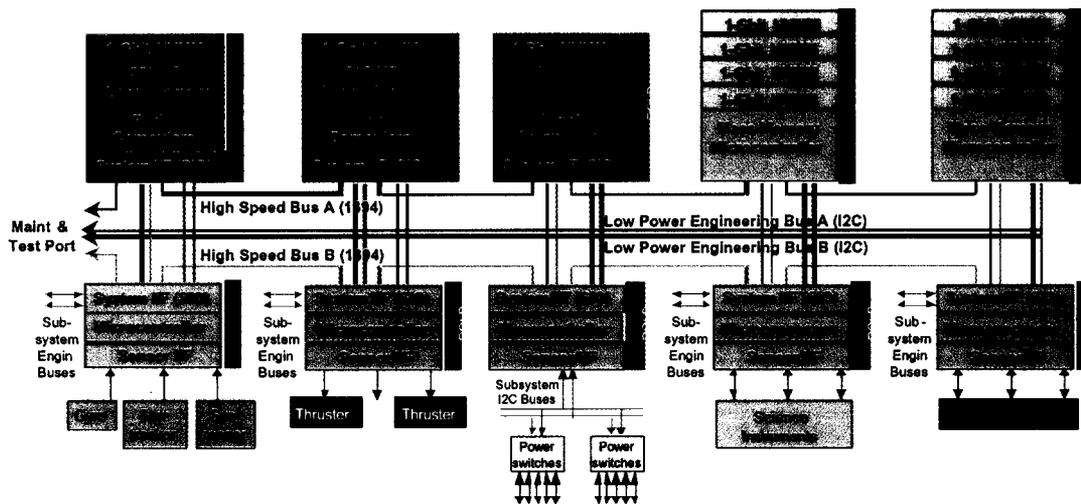


Figure 1: X2000 Command and Data Handling Subsystem Architecture

The CDH subsystem architecture is comprised of a number of PCI based nodes inter-connected by a set of fault-tolerant system buses. Individual nodes can be configured for different functional characteristics by changing the cards within each local PCI element. For example a node could be configured as a mass storage element by adding additional Non-Volatile Memory slices, or as a parallel computing element by adding System Flight Computers. The modularity and scalability of the architecture presents the system designer with a wide variety of choices to meet unique mission requirements. Since standard commercial electrical interfaces and protocols of the COTS buses are used throughout the architecture, assemblies complying with the bus interfaces can be added to the system without impacting the basic architecture.

### 3. X2000 POWER SUBSYSTEM ARCHITECTURE

The X2000 Power Subsystem is based on a direct energy transfer architecture in which the battery voltage is the same as the power bus voltage. The Power Control Slice (PCS) maintains control of power bus regulation and battery charge. The PCS is programmable allowing for different charge algorithms depending on the requirements of the

battery chemistry. Three PCS slices use majority-voting to provide single fault tolerant, power bus regulation function. The three PCS slices have a total of 24 switching elements identical to the design employed on the Power Switch Slice (PSS). These switches can be arranged in different configurations for shunting or series switching of solar array strings or for shunt regulation of radioisotope power sources. Power control capability ranges from 10 Watts to 2000 Watts depending on configuration and system requirements.

The power distribution function is provided by the Power Switch Slice, which has 16 power switches. Each switch has a 3A steady state rating and a 5A transient rating up to 20ms. Over-current protection, and in-rush current control are provided for each load. The PSS has been designed to switch electronic loads, actuate valves and fire pyrotechnic devices. The flexibility of the PSS eliminates the need for additional designs for these common spacecraft functions. The switches support any configuration of high or low, series or parallel combinations. Each PSS is connected to the I<sup>2</sup>C interface for communication with the CDH processing elements.

The X2000 Power Subsystem uses the 3U CompactPCI form factor to enable a common chassis design with the Command and Data Handling subsystem.

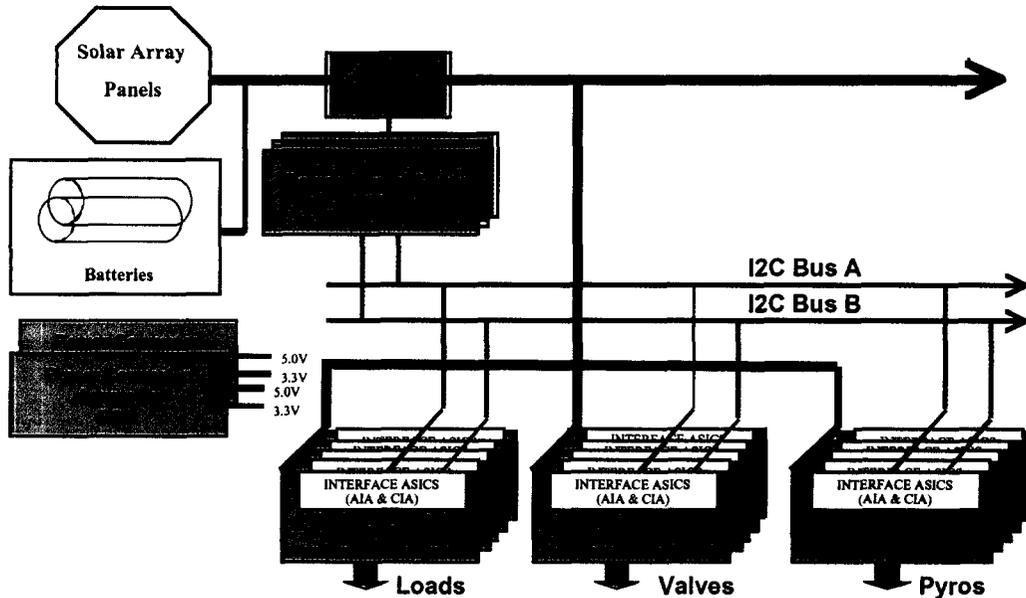


Figure 2: X2000 Power Subsystem Architecture  
(AIA = Analog Interface ASIC, CIA = Command Interface ASIC)

#### 4. X2000 DATA BUS TRADE STUDY

A very detailed trade study was conducted at the beginning of the X2000 Project to select the buses used in the X2000 architecture. At the end of the study, the IEEE 1394 bus was selected because of its high data rate (100 Mbps), multi-master capability, moderate power consumption, strong commercial support, relatively deterministic latency, and the availability of commercial ASIC cores (referred to as Intellectual Properties or IPs in industry). The advantages of IPs are that they are reusable and can be integrated in ASICs, which are fabricated by rad-hard foundries to meet the harsh radiation requirements. The I<sup>2</sup>C bus was selected because of its very low power consumption, multi-master capability, and availability of ASIC IPs. The I<sup>2</sup>C bus has adequate data rate (100 kbps) for low speed communications, a simple protocol, and strong commercial support.

*IEEE 1394 Bus*—The IEEE 1394 bus is the main artery of the system and it is capable of transferring data at 100 Mbps. The use of 1394 represents an improvement of 100 over the widely used 1553 bus. The IEEE 1394 bus has two distinct modes of data transactions for increased efficiency, the isochronous transaction and the asynchronous transaction.

The isochronous transaction guarantees on-time delivery but does not require acknowledgment, while the asynchronous transaction requires acknowledgment but does not guarantee on-time delivery. Isochronous messages are sent through channels and any 1394 node can talk on or listen to more than one isochronous channel. Once every isochronous cycle, every 125 microseconds, each active isochronous channel has to arbitrate for the bus. The channel is guaranteed a time slot during the isochronous cycle to send out its isochronous messages. At the beginning of each isochronous cycle, the root sends out a cycle start message. The isochronous transactions will follow during the cycle.

Unlike the isochronous transaction, an asynchronous transaction is not guaranteed to be completed within a single isochronous cycle. Therefore, a 1394 node may have to wait a number of isochronous cycles before its asynchronous messages can be sent out. The asynchronous transaction employs a fair arbitration scheme, which allows each node to send an asynchronous message only once in each arbitration cycle. An arbitration cycle can span many isochronous cycles, depending on how much of the bus bandwidth is consumed by the isochronous transactions and how many nodes are arbitrating for asynchronous transactions.

During the bus startup or after a reset, the bus will go through an initialization process in which each node will get a node ID. In addition, the root, the bus manager, and the isochronous resource manager will be elected. The root mainly is responsible for sending the cycle start message and acts as the central arbitrator for bus requests. The bus manager is responsible for acquiring and maintaining the bus topology. The isochronous resource manager is responsible for allocating bus bandwidth to isochronous nodes. The root, bus manager, and isochronous resource

manager are not pre-determined, so that any nodes can be elected to take these roles as long as they have the capability.

*I<sup>2</sup>C Bus*—The I<sup>2</sup>C bus is a simple serial bus with a data rate of 100 kbps and a more traditional multi-drop topology. The I<sup>2</sup>C bus has two open-collector signal lines: a serial data line (SDA) and a serial clock line (SCL). Both signal lines are normally pulled high when the bus is inactive. When a bus transaction begins, the SDA line is pulled down before the SCL line. This constitutes a start condition. The address bits follow, which is followed by a read/write bit and then an acknowledgment bit. The target node can acknowledge the receipt of the data by holding down the acknowledgment bit. After that, eight bits of data can be sent followed by another acknowledgment bit. Data can be sent repeatedly until a stop condition occurs, where the source node signals the end of transaction by a low-to-high transition on the SDA line while holding the SCL line high. There are two applications of the I<sup>2</sup>C bus in this architecture. At the system level, it is used to assist the IEEE 1394 bus to isolate and recover from faults. At the subsystem level, a separate I<sup>2</sup>C bus is used to collect engineering data from sensors and send commands to power switches or other equipment.

#### 5. RELIABLE DESIGN

*Radiation Survivability*—The X2000 system was designed to meet the extreme radiation requirement encountered during a proposed Europa Orbiter (EO) mission. To put the EO mission requirement into perspective, at Europa, an astronaut inside an EVA suit would receive a lethal dose in 12 minutes. The primary radiation requirements for this mission on the avionics system are as follows:

The total dose inside the proposed spacecraft structure is 6.5 MRAD.

The total dose requirement for the X2000 Avionics at the part level is 1 MRAD.

All parts must have a LET of 75 MeV/g-cm<sup>2</sup>, be latch-up immune, and immune to burn out or gate rupture due to single event effects.

Electronics parts are selected and shielded to obtain a radiation design margin of 2.

The JPL approach to meet the radiation environmental requirements is based on three methods; use of radiation hardened parts, use of radiation tolerant parts, and use of commercial parts. The details of these approaches is as follows:

*Radiation Hardened components (> 1 MRAD)*—The majority of the X2000 Application Specific Integrated Circuits (ASICs) are fabricated on a radiation hard foundry at Honeywell Solid State Electronics Center. Other rad-hard components used in the design are screened to verify they will survive the environment with a minimum level of shielding.

*Radiation Tolerant Components (> 100 KRAD)*—If a radiation hard component is not available or if other critical performance requirements could not be achieved with a radiation hard device, radiation tolerant components are selected. An example is the RAD750 processor used on the X2000 flight computer that is fabricated on a radiation tolerant 0.25-micron line. Radiation tolerant devices typically have a total dose capability of 100 to 300 Krads. The parts are then shielded to meet the required radiation levels.

*Commercial components (<100 KRAD)*—Commercial parts are used only when absolutely necessary due to unavailability of rad-hard or rad-tolerant parts, or again when use of such parts would seriously preclude achieving target system performance, schedule, or cost. The best example where commercial parts have been used in the design is memory technology: Synchronous DRAM are used to achieve high computer performance, and high density Flash Memory devices (128 Mb per device) are used to support non-volatile storage of software and data. The use of this commercial components requires extensive parts screening, testing, and system shielding. An example here is the local board level shielding and radiation vault required for the NVM flash components in the Europa environment.

*Electronic Parts Selection*—JPL maintains a world class electronic parts organization and parts selection has always been a key component for reliability in JPL planetary missions. The X2000 program requires all electronic components to be procured to the most stringent standards possible, QML-V, Class S, or Class H for hybrids. Parts that can not be procured to these levels must undergo an extensive screening program to verify their acceptability. No exception is made to the parts reliability program for cost or performance reasons.

*Long Life and Reliability*—JPL has a long established track record for highly reliable and long life missions. With a typical deep space mission life of 6 to 8 years and no options for in-flight servicing, high reliability is the primary requirement for all JPL components. For X2000 avionics, this requirement is met by the parts selection processes described above and by using these parts well below their stated ratings. Extensive analysis is performed to verify that the circuit design takes all worst case electrical, thermal, dynamic, and radiation environment conditions into account and that all parts have significant operating margins. Each X2000 card must also pass a rigorous qualification test program that subjects the assembly to a harsher environment than it will be exposed to in-flight to verify the design margin. An extensive integrated test with the flight software is conducted throughout the development cycle to verify all aspects of system performance and establish an un-paralleled level of system reliability. An example of the success of these processes is the Voyager mission, which recently celebrated the 25th anniversary of its launches.

*JPL's Approach to Fault Tolerance for X2000*—The X2000 Avionics is a fault tolerant system based on commercially available technologies. An important benefit of a COTS

based system is reduced development cost. By taking advantage of available designs, intellectual properties, existing software, and commercial test equipment a system can be developed in a shorter time frame. For example, the use of the CompactPCI interconnect bus allowed the use of a COTS bus analyzer during the development and test of the system. Commercially developed components usually have much higher performance than custom designed flight components because of competitive pressure in commercial markets. On the other hand, COTS components are not specifically developed for highly reliable applications such as long-life deep-space missions. The challenge of using COTS technologies is to enhance their reliability for space applications

In order to achieve the required reliability, JPL has developed a multi-layer fault protection methodology to achieve high reliability in COTS-based avionics systems. This methodology has been applied to the bus architecture that uses the COTS bus interface standards IEEE 1394 and I<sup>2</sup>C.

*A Multi-Level Fault Protection Methodology for COTS-Based Systems*—To compensate for COTS technologies weakness in fault tolerance, X2000 has employed a multi-level fault protection methodology to achieve high reliability. The methodology is applied to the X2000 bus architecture by using four levels of fault protection mechanisms.

Level 1: Native Fault Protection—Most of COTS bus standards have some limited fault detection capabilities. These capabilities are exploited as the first line of defense.

Level 2: Enhanced Fault Protection—Additional layer of hardware or software can be used to enhance the fault detection, isolation, and recovery capabilities of the native fault containment region. This layer contains a small amount of custom logic. Examples are watchdog timers or additional layers of error checking in the protocol. These fault tolerance mechanisms are designed in such a way that they do not affect the basic commercial standard functions. These mechanisms have been added to X2000 system interfaces.

Level 3: Fault Protection by Component Level Design Diversity—Many COTS components have fundamental fault tolerance weakness that cannot simply be removed by enhancing the native fault protection mechanisms. These weaknesses usually are related to single points of failures. One example is the tree topology of the IEEE 1394 bus. When a failed node isolates a bus, no watchdog timer or extra layer of protocol can reconnect the bus. In order to compensate for such fundamental weaknesses, different types of buses may be used to complement the IEEE 1394 bus. Specifically, the I<sup>2</sup>C bus, which has a multi-drop bus topology, is used to assist the IEEE 1394 fault isolation and recovery in the X2000 architecture. The coordination between these two buses requires custom software.

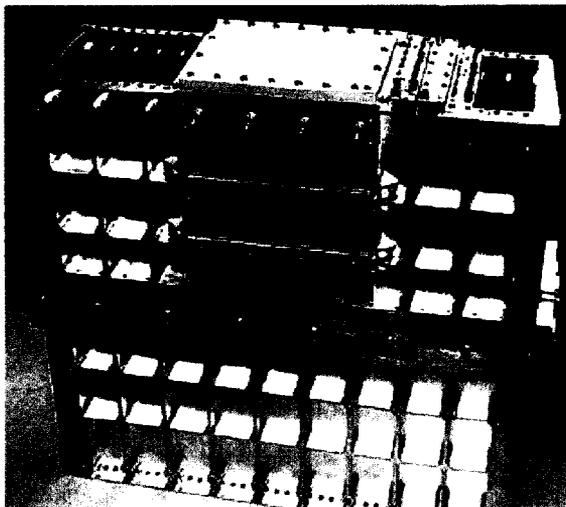
Level 4: Fault Protection by System Level Redundancy—Stand-alone functional assemblies are replicated by adding additional redundant nodes for system level fault recovery. To further enhance the effectiveness of the system level

redundancy, system diversity is also employed in this level. For example, the X2000 design implements the redundant IEEE 1394 buses with different topologies, such that any branch node in primary bus set is a leaf node in the backup bus set and vice versa. In other words, there is no node that is a branch node for both buses. Hence, a failed node can only partition the bus in which it is a branch node. The redundant fault containment regions can be either in ready or dormant states, depending on the recovery time and other system requirements. If they are in ready state, voting or comparison of outputs among the regions will provide one more level of fault detection. In either case, the redundant regions are necessary resources for the fault recovery process.

## 6. X2000 BUILDING BLOCKS

The X2000 Avionics have been developed to be configurable and scalable in a variety of architectures to accommodate the diverse requirements of spacecraft computation, data storage, and power distribution. This flexibility is accomplished by employing commercial standard interfaces and mechanical configuration standards throughout the design. In particular, the use of 3U CompactPCI data bus for all of the computing and data handling components enables the X2000 elements to be used as building blocks for a variety of system designs. These X2000 building blocks enable system solutions for diverse applications with high data processing, large data storage, and I/O intensive applications. The building blocks are as follows:

1. System Flight Computer SFC
2. System Input/Output SIO
3. System Interface Assembly SIA
4. Nonvolatile Memory Slice NVM
5. Power Converter Assembly PCA
6. Power Switch Slice PSS
7. Power Control Slice PCS



*Low Manufacturing and Operations Cost*—A primary advantage of using the X2000 Avionics in a system design is the large investment made in bringing a comprehensive set of commercial technologies to a level of reliability suitable for space applications. By funding the non-recurring costs of these developments, X2000 enables mission designers to develop systems that utilize existing components from industry. This represents a tremendous savings and risk reduction to the user mission. The use of commercial standards facilitates development and improves operability by the use of commercially available development tools. In addition, by using widely accepted commercial standards, a mission can more readily find the technical expertise needed to test and verify the system design and is not required to maintain a set of technical experts skilled in a narrow custom point design.

*Mechanical Packaging*—The circuit board assemblies developed by the X2000 project all have a 3U CompactPCI form factor. The standardized packaging technique is a key component of the modularity and scalability of the X2000 architecture. The major requirements the packaging design had to address are:

A completely conductive thermal design with 70°C at the slice interface

A dynamic environment of 0.2 g<sup>2</sup>/Hz vibration at the mounting surface of the chassis

Extensive design, analysis, and developmental testing have been conducted by X2000 to provide a packaging design with adequate safety margins to the requirements. An example of the chassis, with the radiation shielding vault required for the proposed Europa Orbiter spacecraft is shown in Figure 3.

*Thermal Management*—A key component to the X2000 design is the fact that the thermal system is entirely passive. The use of a passive thermal system is a standard for JPL. The cooling system is based on conductive cooling and therefore requires no moving parts and requires no scheduled

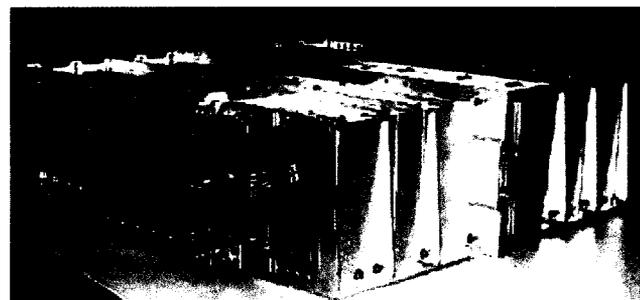


Figure 3: X-2000 CompactPCI Chassis

service. The heat is all conducted from thermally conductive cards to the chassis. The heat is then conducted through to the thermal plate of the X2000 chassis. For the Europa Orbiter design, once the heat was conducted to the thermal plate it was sent to radiators on the spacecraft body.

The CompactPCI cards are constructed to the standard footprint with the addition of wedge-lock devices. These devices provide for a low thermal resistance from the card to the chassis. The current thermal resistance of this interface is 1.1°C/Watt /cm.

The X2000 thermal design is based on two key components: Thermal conductive cards; and thermally conductive chassis. The X2000 thermal design results in an overall 25°C temperature rise with regard to the baseplate for a worst case X2000 card dissipation of 12W for the System Flight Computer.

**System Flight Computer (SFC)**

The System Flight Computer development was sponsored by the X2000 project at BAE Systems of Manassas, Virginia, to provide NASA and the aerospace industry with a high performance, space qualified computer able to survive severe environments. The driving environmental requirements were based on the extreme radiation exposure for the Europa Orbiter mission. The result is a CompactPCI computer based on a radiation hardened version of the PPC750 processor. The SFC provides a factor of ten improvement in processing power from existing space qualified computers in a compact 3U form factor. Currently in production at BAE, the SFC will be a standard computer for future space applications.

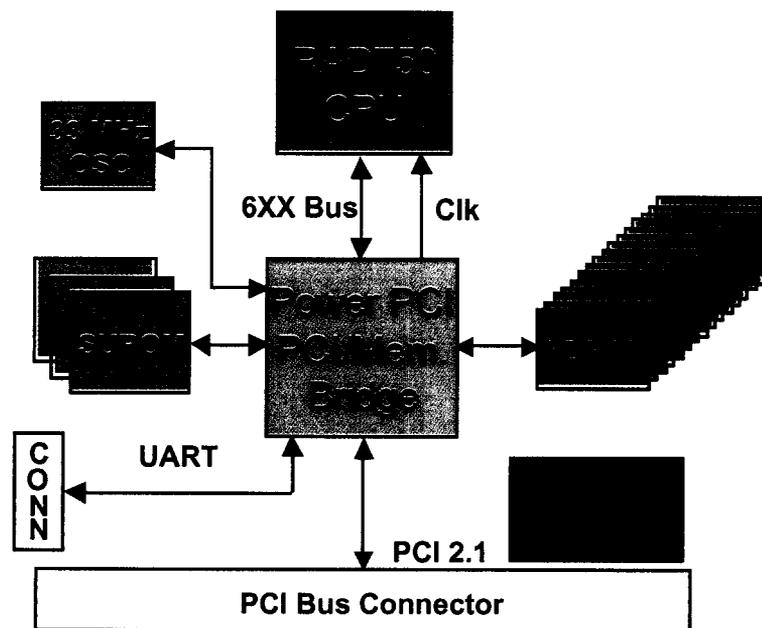
The SFC design contains:

- The 133 MHz radiation hardened RAD750 processor
- A custom designed PCI bridge chip
- 128 Mbytes of SDRAM
- 256 Kbytes of EEPROM for startup code.



**Figure 4: X2000 System Flight Computer Engineering Model**

The X2000 SFC design includes a power management technique to enable system designers to trade CPU performance for power consumption. By scaling the processor clock speed the SFC power can be reduced from the peak performance level of 12 Watts to 8 Watts. The overall low power consumption of the SFC allows the board to use conduction cooling only for heat dissipation.



**Figure 5: X2000 System Flight Computer Block Diagram**

The RAD750 CPU was developed by taking the commercial PPC750 and enhancing the circuit design to improve radiation hardness. The RAD750 is capable of full performance after a total ionizing dose of 200 Krad(Si) and is SEU hard to  $1 \times 10^{-10}$  bit-errors/day.

The Power PCI bridge chip provides the interface control logic for the X2000 SFC. Included in the Power PCI are the PCI level 2.2 master and slave interface, a 16550 compatible UART, JTAG, the on board 64 bit interface to the RAD750, and the interface to the SDRAM and SUROM memory buses. The Power PCI also contains the clock control configuration registers for managing the RAD750 power consumption.

### System Input/Output (SIO)

The SIO contains the data bus interfaces to connect the CompactPCI components in the X2000 command and data handling chassis to external devices, sensors, and power control elements. The SIO contains two fully redundant 100 Mbit IEEE 1394a serial buses for high bandwidth communication, four 100 Kbit I<sup>2</sup>C serial buses for engineering and lower speed functions, two RS-422 UART interfaces, and two independent CompactPCI initiators. The design for the bus interfaces on the SIO is implemented in four (two per string) radiation hardened ASICs. Designed at JPL and fabricated by Honeywell Solid State Electronics Center, the Digital I/O (DIO) and the Mixed Signal I/O (MSIO) ASICs contain the logic and driver circuitry for the SIO. The SIO is implemented on a double-sided 3U CompactPCI card.

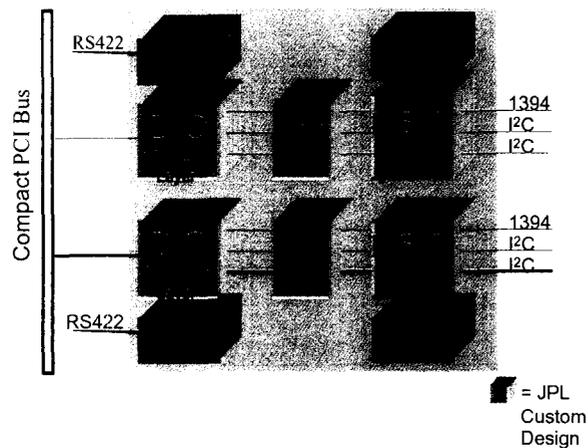


Figure 6: X2000 System I/O Block Diagram

The Digital I/O ASIC contains the logic for the initiator and target CompactPCI interface, the link and transaction layers of the IEEE 1394 bus, two independent I<sup>2</sup>C bus controllers, and two 16550 compatible UARTs. The DIO is fabricated on Honeywell's 0.35 micron silicon on insulator (SOI) line

and is radiation hard to 1 Mrad total dose. A 472 pin Dimpled ball grid array (BGA) ceramic package has been qualified for packaging the DIO.

The Mixed Signal I/O (MSIO) contains the 1394 physical layer, and the physical interfaces for two I<sup>2</sup>C buses. The MSIO circuitry is divided into three separate power domains to provide isolation between the 1394 and I<sup>2</sup>C. The MSIO is also transformer isolated from the DIO allowing the physical bus layers to be completely isolated from the link layer power domains. The isolation design provides a highly reliable, fully independent, dual string communications capability between multiple processing nodes. A block diagram of the dual string SIO card is shown in Figure 6 and a photograph of the prototype version is shown in Figure 7.

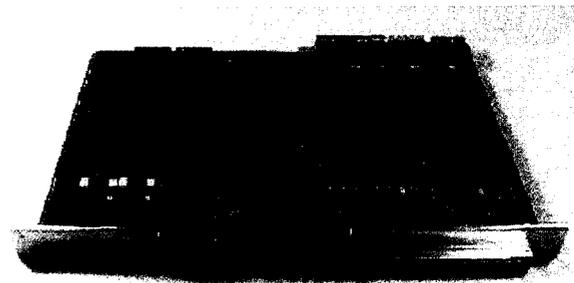


Figure 7: X2000 System I/O Prototype

### System Interface Assembly (SIA)

The X2000 System Interface Assembly was developed at JPL to provide access to science instruments, navigation sensors, and telecommunication devices that do not have 1394 or I<sup>2</sup>C capabilities. The SIA contains:

- a 1553 Bus Controller/Remote Terminal Monitor (BCRTM) interface designed to interface to the Small Deep Space Transponder

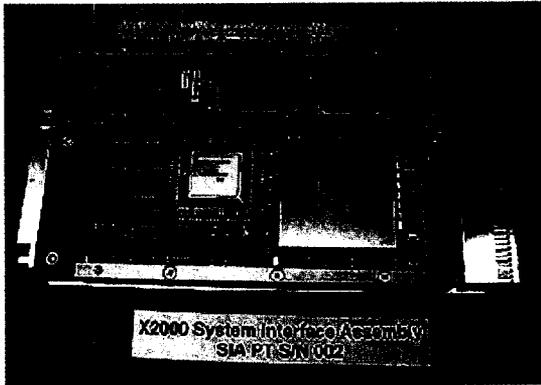
- redundant serial interfaces for command and telemetry of the transponder

- 4 bi-directional high speed (6 Mbps data, 1 Mbps command) serial interfaces for science and navigational instruments

- a serial connection for launch vehicle interface

- 1 MB of SRAM buffer space

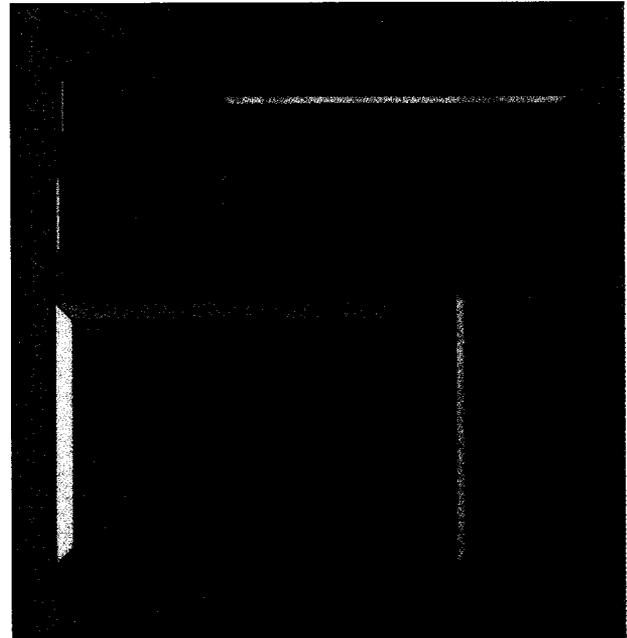
Most of the functionality of the SIA is contained in the SIA ASIC. Fabricated on the Honeywell HX3800 rad hard line, the SIA ASIC provides the bridge between the external interfaces and the PCI bus.



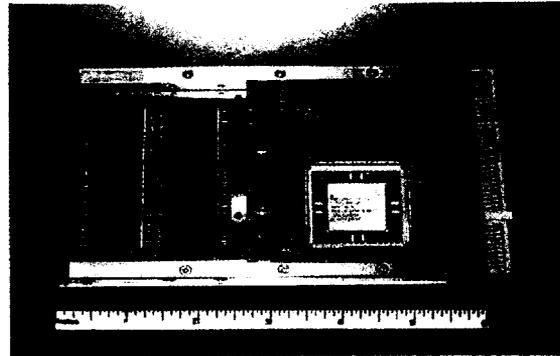
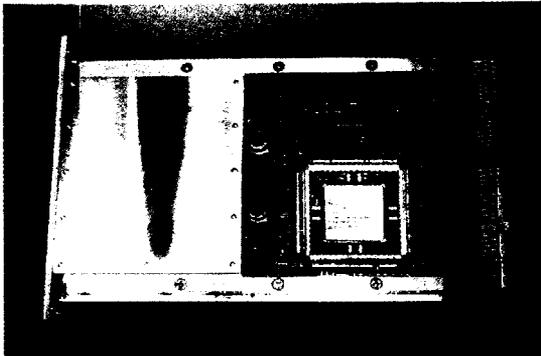
**Figure 8: X2000 System Interface Assembly Prototype**

### Non-Volatile Memory (NVM)

The X2000 Non-Volatile Memory (NVM) card was developed with X2000 sponsorship at SEAKR Engineering in Englewood, Colorado. The NVM provides high density solid state storage for data intensive applications. The NVM uses 20 Samsung 128 Mb Flash memory chips to provide 2 Gb of memory on a 3U CompactPCI card. The memory is



**Figure 9: X2000 System Interface Assembly Block Diagram**



**Figure 10: X2000 NVM Engineering Model (w/ and w/o radiation shield)**

organized into two independently powered banks to lower power consumption when the NVM is not being accessed. The NVM has been designed to accommodate higher density Flash parts for expansion up to 16 Gb of storage. The NVM interface to the PCI bus is implemented in a custom Honeywell radiation hardened ASIC. This ASIC supports a 33MHz PCI data bus clock rate. Another function of the ASIC is Reed-Solomon Error Detection and Correction for the memory array. The NVM is specified at 20 Mbits/second sustained throughput. The NVM has a typical power consumption of 2 Watts, and an unshielded mass of 220 grams.

To provide for a high radiation total dose capability for the Flash devices the NVM can be shielded with a tungsten

clamshell. The shielded version mass is 1.7 kg. Radiation testing has been performed on the Flash components in terms of Proton, SEU, and Total Dose. In terms of SEU, the results are unparalleled. For total dose, the TID capability varies with use up to 40 kRads. The NVM is currently being used on the Deep Impact mission. Flight model NVMs have been delivered to Deep Impact for system test and spacecraft integration.

**Power Subsystem Electronics Building Blocks**

X2000 is developing, with Lockheed Martin CSS in Newtown, Pennsylvania, radiation hardened power subsystem electronics for power distribution, DC power conversion, and primary power bus regulation. The power subsystem cards are implemented on the 3U CompactPCI mechanical form factor to take advantage of the chassis design for the Command and Data Handling Subsystem.

**X2000 Power Switch Slice (PSS)**

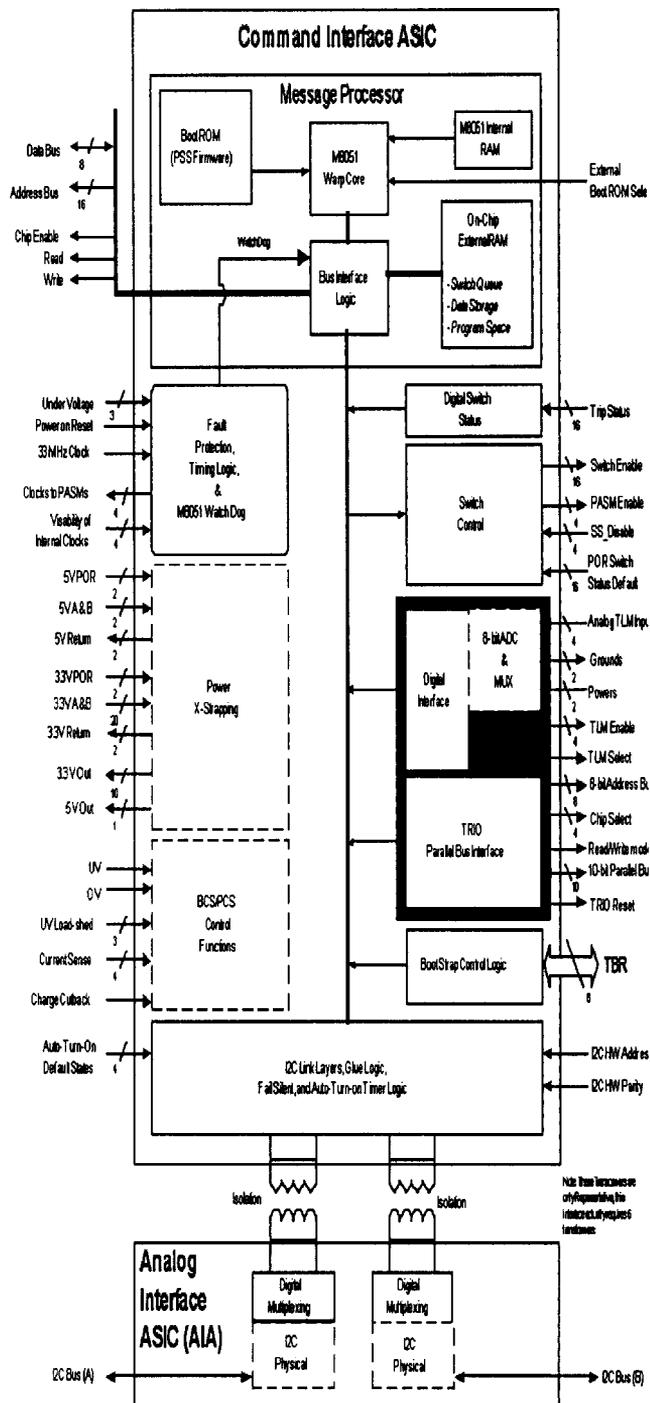
The X2000 Power Switch Slice provides 16 independent solid state switches that are capable of power distribution, propulsion valve actuation, and pyro device initiation. The different functions of the PSS are selected by configuring jumpers in the Power Subsystem Electronics backplane. The PSS is based on the Power Actuation Switching Module developed as a technology demonstration for the DS1 mission. The PSS contains four PASM's, a Command Interface ASIC for switch control and telemetry, and two Analog Interface ASICs to provide power supply isolation of the Power Subsystem. Each switch provides a current trip level of 3 Amps with a 20 msec response time and contains di/dt control. The communication between the PSE and the CDH subsystem is through two redundant I<sup>2</sup>C buses.

**Command Interface ASIC / Analog Interface ASIC**

The Command Interface ASIC (CIA) and Analog Interface ASIC (AIA) are being developed at JPL to provide the circuitry to implement a transformer isolated, fully redundant command and telemetry interface between the CDH subsystem and the PSE subsystem. The CIA includes an integrated 8051 core, an A/D converter, the I<sup>2</sup>C bus logic, and the individual switch command and telemetry functions. The CIA is fabricated on Honeywell's radiation hard mixed signal line.

**Power Actuation and Switching Module (PASM)**

The PASM is a key building block for the X2000 power subsystem architecture. Each PASM contains four solid-state switches and a Switch Control ASIC (SCA) chipset. The SCA has been developed by the X2000 project at JPL to provide a radiation hardened control interface to individual power switches. Using custom designed cells from the Honeywell HX2000 foundry, X2000 has developed a process for building rad-hard mixed signal ASICs that can operate at power system voltage levels. The SCA is currently in the physical design phase and is scheduled to begin fabrication in late 2002. The PASM is fabricated as a multi-chip module at Lockheed-Martin CSS using General Electric's high density interconnect technology. The PASM is scheduled for prototype fabrication in early 2003.



**Figure 11: Command Interface ASIC (CIA) Analog Interface ASIC (AIA) Block Diagram**

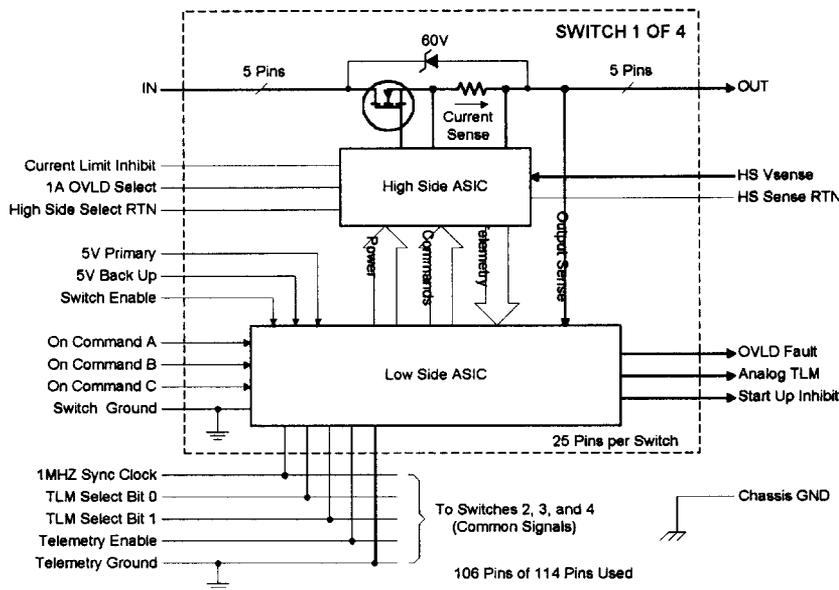


Figure 12: Power Actuation and Switching Module (PASM) Block Diagram

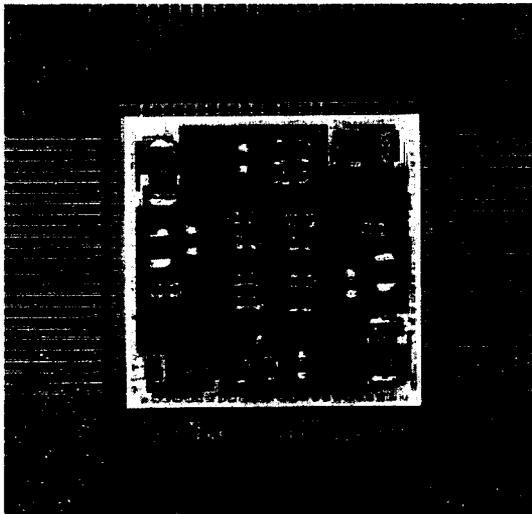


Figure 13: Power Actuation and Switching Module

### Power Converter Assembly (PCA)

X2000, with Lockheed-Martin CSS, is developing a high reliability, high density, power converter for high radiation space environments. The PCA will have two 30 W single forward converters producing output voltages of 3.3V, 5V, or 15V, on a 3U CompactPCI form factor. The PCA is designed such that the outputs of two or more power converters can be connected together to share an output load

greater than 30W. The specified conversion efficiency for a 30 W load is greater than 80%. The PCA is currently in design with the first prototype scheduled for 2003.

### X2000 Device Driver Software

The X2000 device driver software comprises an abstract device model (ADM), a set of device drivers derived from the ADM, a board support package, and start-up ROM code required to boot the X2000 flight computer. The device drivers support the full capability of the X2000 hardware. In addition to providing access to device functionality, the drivers provide a sophisticated repetitive command execution facility, command cancellation, synchronous and asynchronous operation, and the ability to attach user-defined actions that are executed at predefined points in the execution of a device command. The software is supported by a Low-Level Exerciser (LLE) that provides TCL-based access to hardware and software functions. The software is expected to be complete in approximately two years. The performance of the X2000 avionics with realistic test software will be characterized at the end of the project development.

### Conclusion

NASA has made a significant investment in advanced, high-performance, highly reliable, and radiation tolerant avionics for space exploration. The use of commercial interfaces enhanced for space applications has led to a system architecture and a set of building blocks that have wide application over a diverse set of mission requirements.

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