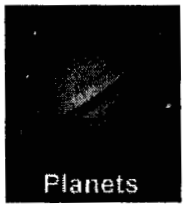
Jet Propulsion Laboratory

National Aeronautics & Space Administration

California Institute of Technology



(Pb free) vs (Pb) Reliability of Advanced Electronic Assemblies

by

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Outline

- Electronic Package Trend
  - Package shrink trends
  - IPC 9701 "SMT Qual"
- Lead Free
  - Current status/issues
  - Package/board
- Assembly Reliability
  - Literature Data
  - Board integrity/solder microstructure after reflows
  - Tin whisker
  - Thermal/Mechanical cycles
- Conclusions

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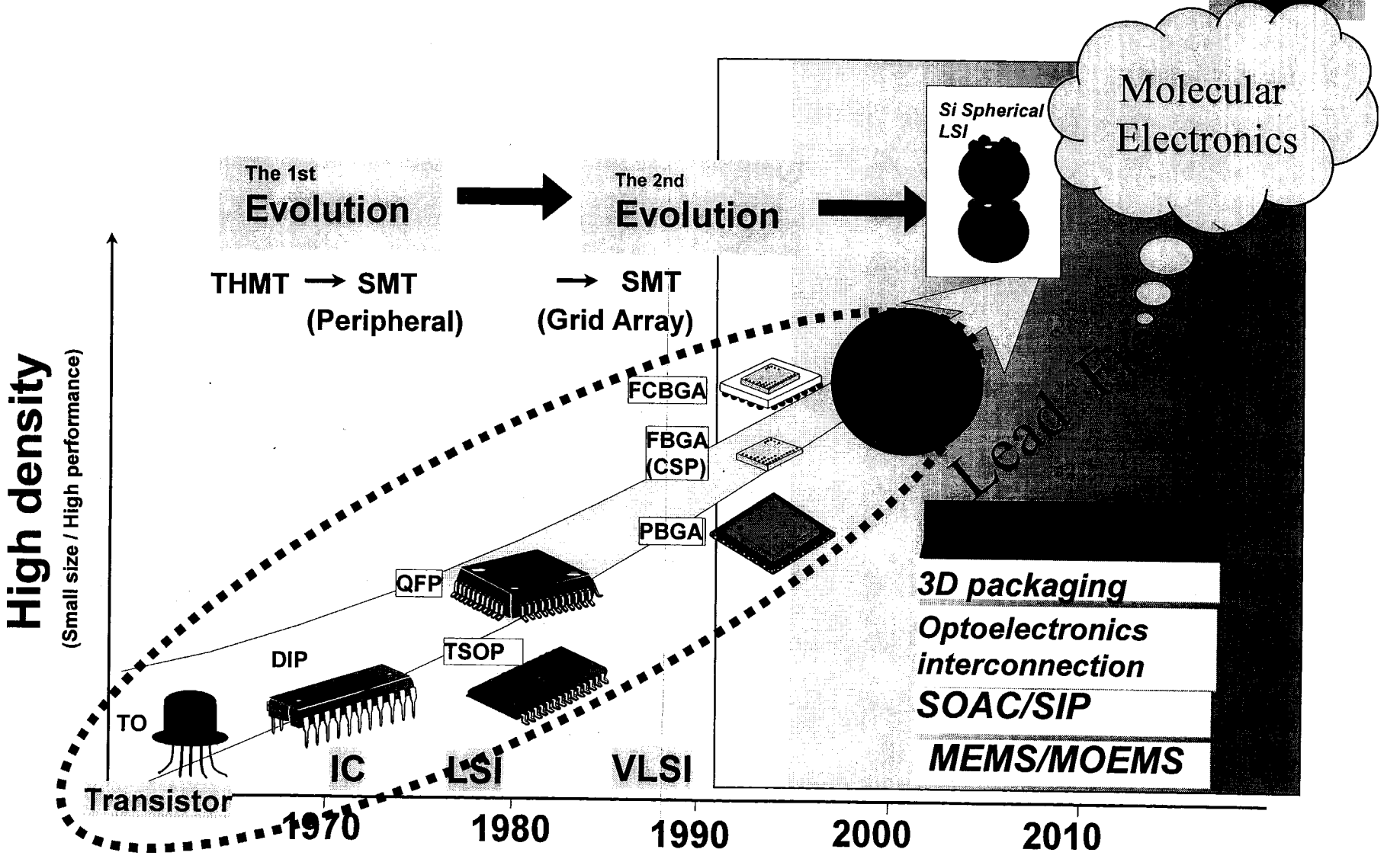
High Density Integration



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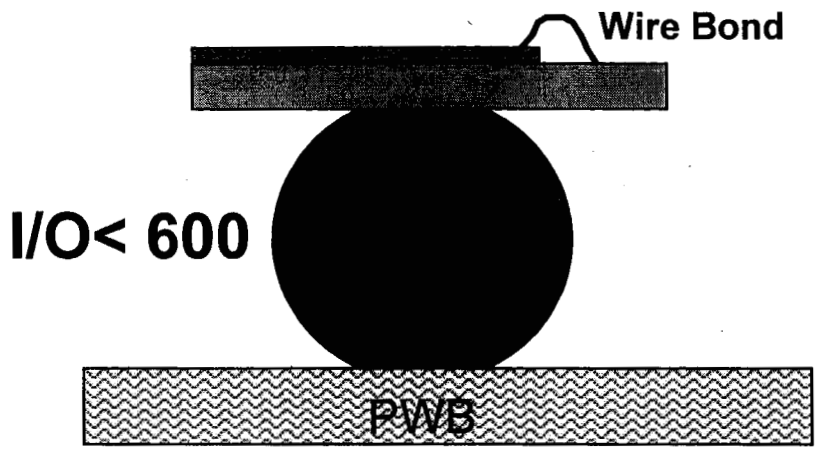
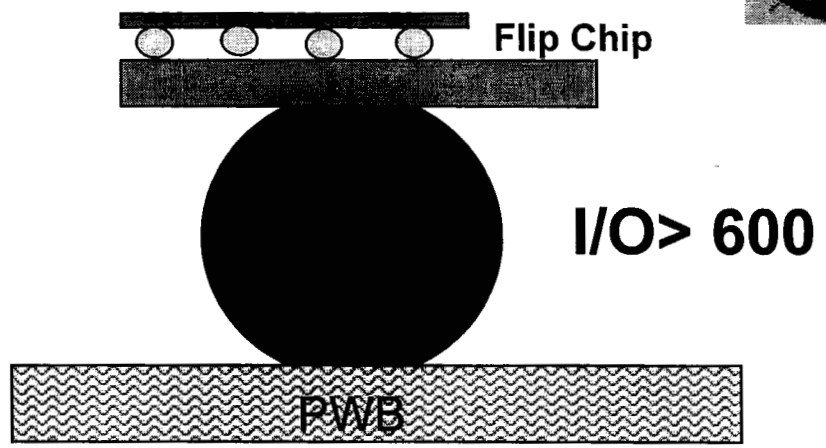
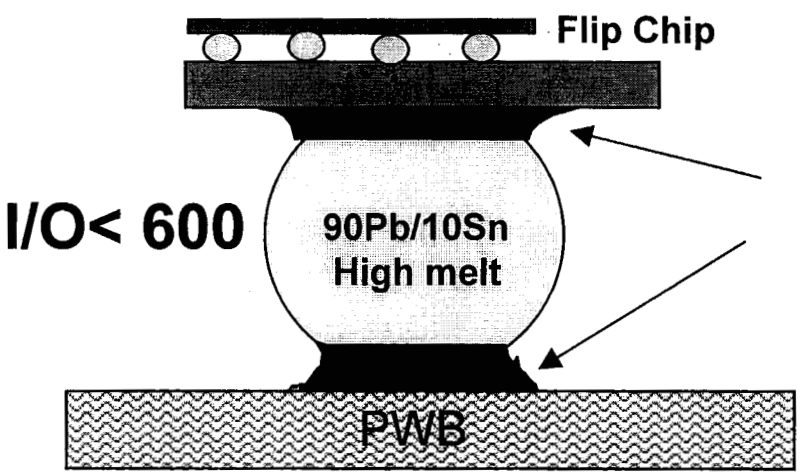
BGA Package Types



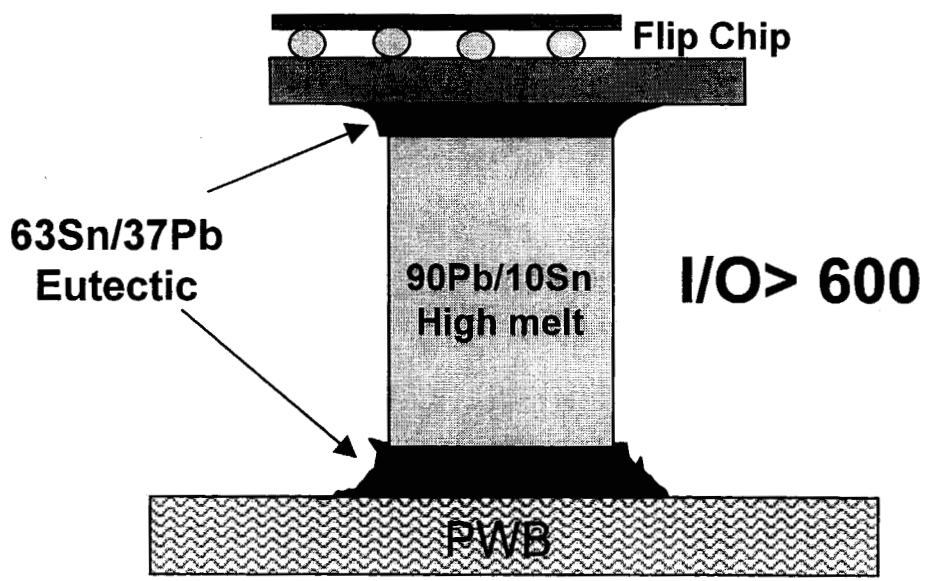
Plastic BGA (PBGA)



Flip Chip BGA (FCBGA)



Ceramic BGA (CBGA)



Column CBGA (CCGA)

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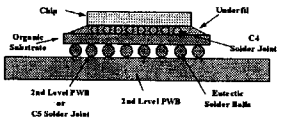
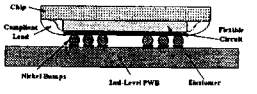
CSPs

Grid Arrays

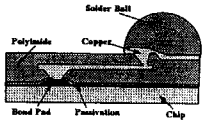
C4



Wire Bond



Wafer

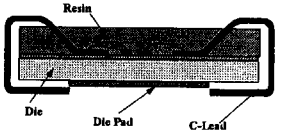


- High I/Os
- Wire bond I/O Limitation
- C4 ceramic, Wafer, Reliability?
- Assembly Robustness

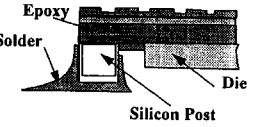
Self Alignment

Leads

Leaded



No Leads



- Low I/Os
- No Leads, Reliability?
- Assembly Robustness?

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References

Coming Soon

CHIP-SCALE PACKAGING FOR MODERN ELECTRONICS

Due mid-2002

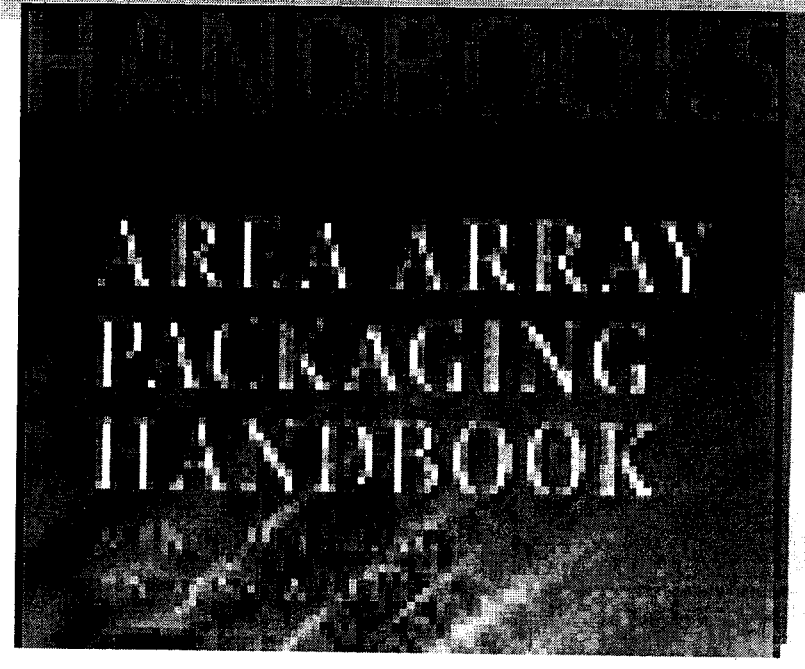
by

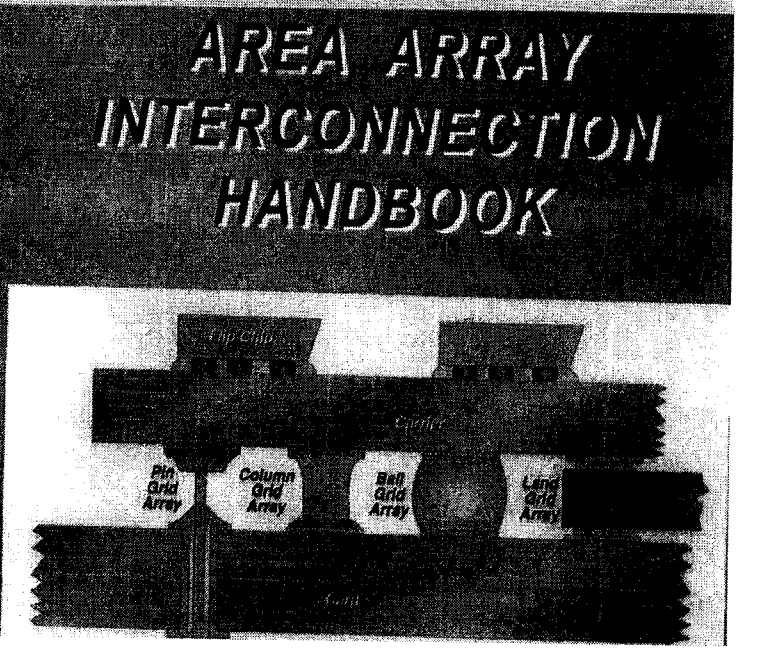
Joseph Fjelstad, Reza Ghaffarian, Young Gon Kim

ode: EP154
BN: 0 901150 43 6
elease Date: Not yet available, expected mid-2002

- Register to be notified when this book becomes available
- Contents - Downloadable PDF file. The full Contents List and the author's Preface (you will need Acrobat Reader to view these pages)

escription





Qualification- IPC 9701

- IPC 9701, Released Jan 2002
  - IPC SM785- Guideline
    - No answer to the question of data for product application
    - Data comparison
    -
  - IPC 9701
    - Details on thermal cycle test and acceptance

- Key Controls
  - Surface finish (OSP, HASL), thickness, 93 mil, NSMD, continuous monitor, etc.
- Five Cycle Conditions
  - Preference 0/100°C
- Five number of thermal cycles
  - Preference 6,000 cycles

IPC 9701- "Performance Test Methods and Qualification Requirements for Surface Mount Solder Attachments"

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IPC 9701 Temperature Cycle Requirements

Table 1 Temperature cycling requirements specified in Table 4.1 of IPC 9701

Test Condition	Mandated Condition
Temperature Cycle (TC) Condition: ***TC1***	***0°C ↔ +100°C (Preferred Reference)***
TC2	–25°C ↔ +100°C
TC3	–40°C ↔ +125°C
TC4	–55°C ↔ +125°C
TC 5	-55 °C<-> 100°C
Test Duration	Whichever condition occurs FIRST: 50% ***(preferred 63.2%)*** cumulative failure (Preferred Reference Test Duration) or
Number of Thermal Cycle (NTC) Requirement: NTC-A	200 cycles
NTC-B	500 cycles
NTC-C	1,000 cycles (Preferred for TC2, TC3,and TC4)
NTC-D	3,000 cycles
NTC-E	***6,000 cycles (Preferred Reference TC1)***
Low Temperature Dwell	10 minutes
Temp. tolerance (preferred)	+0/–10°C (+0/–5°C) [+0/–18°F (+0/–9°F)]
High Temperature Dwell	10 minutes
Temp. tolerance (preferred)	+10/–0°C (+5/–0°C) [+18/–0°F(+9/–0°F)]

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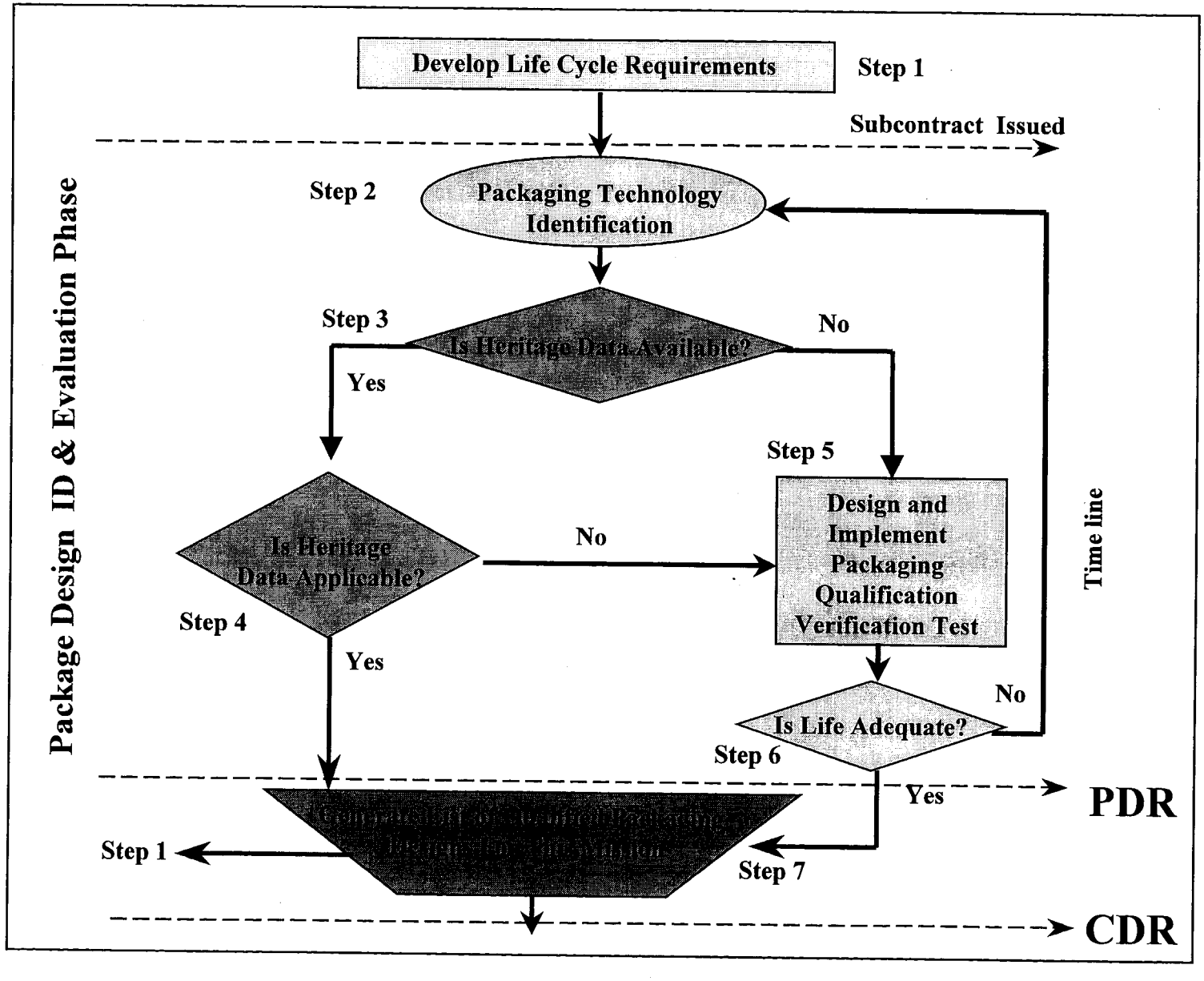
PQV-Package Qualification and Verification-I



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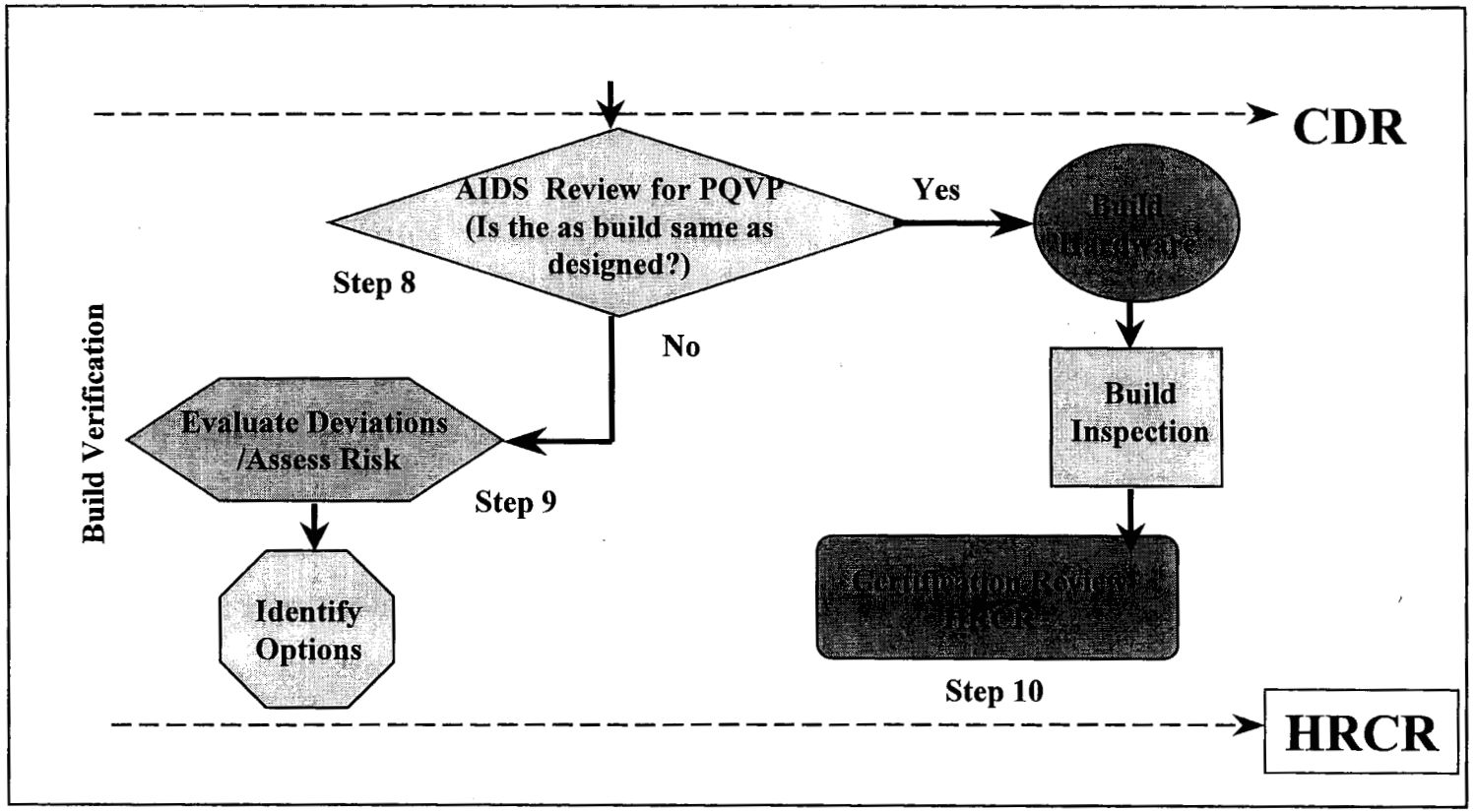
PQV-Package Qualification and Verification-II



NHB 5300.4 (3A-1), 200 cycles –55/100°C

NHB 5300.4 (3A-2), Do the right qualification test

Number of cycles = 3 * (ground + mission)

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Pb Free: Current Status

- Why?
  - "Green" Marketability/Reputation Advantage
  - WEE & Other Legislation (Waste from Electrical & Electronic Equipment)
  - 100s products worldwide
- Lead Free SAC (Sn 3.9Ag0.6Cu)
  - Min reflow temp 235°C (240-260°C)
  - Much info on properties
  - Relatively minimum issues with exiting package/assembly
  - Package issues being addressed
- Package Finish Issue (Tin Whisker)
  - Matte tin (low organic content, grain>1 μm
- Assembly Reliability
  - Minimum data & scatter
  - Inspection criteria redefinition
  - Mixed Pb free & Pb assembly issues

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JPL Pb Free: Package

- Lead Free require higher temp. reflow (240-260C)
- Tg (glass transition temp.) Is become more critical
- Moisture sensitivity level (JEDEC)
  - At least one level lower
- Isothermal shear strength
  - Longer life for the same damage level
- Termination finish
  - Tin whisker

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Pb Free: Board/Assembly

- Board
  - CTFs varied with surface finish
  - OSP surface finish better than ENIG
  - Multiple reflow (double-sided, rework)
  - Tg for higher reflow exposure
  - Board thickness
  - Microvia integrity/reliability with high temp. exposure
- Assembly
  - Paste print, similar?
  - Solderability is reduced
  - Voids increase specially with tin-Lead components

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Pb Free: Assembly Reliability-I

- CBGA (IBM)
  - Model, SAC about 2.5 times better (0/100C)
  - Test results: depends on type of cycle?
- BGA 324, 1mm pitch (Motorola)
  - -50/150°C, early failure to trace, 1.6 times improvement
  - -40/125°C, no early failure, 1.3 times improvement
  - Failure depends on DNP, not die, thick substrate?
- BGA/CBGA (NEMI)
  - 256 BGA equivalent (-40/125°C)
  - 256 CBGA Better (0/100°C)
- LCC 24 (Swiss Federal Institute)
  - (-20/120°C)- less resistance
- Flip chip with underfill
  - SAC slightly lower, underfill optimization (Auburn)
  - SAC lower (Fraunhofer Institute)

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JPL Pb Free: Assembly Reliability-II

- QFP 208, USMD8, CCSP 224, CSP 308 (Flextronic)
  - Consumer: All assemblies passed (IPC9701), 3040 cycles (0/100C)
  - Telecom (300 cycles, -55/125)
    - QFP 208, CSP 24, no failure 300
    - CSP 308 a few failures
  - OSP performed better than ENIG
  - STD reflow temp (245) better than , shorter time better than 257C
- FlexBGA144, PBGA256 (Amkor)
  - Flex BGA: SAC 25% (-40/125), 60 % (0/100)
  - PBGA : SAC 100% (-55/125)
  - Ball shear (isothermal aging 150C): SAC higher stability (10X to induce interfacial failure)
- CSP 64 I/O Vibration 48 min (Mil-883), 20g
  - All passed 3 axes, Sn 3.5 Ag & eutectic
  - No difference between OSP & Ni/Au

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Pb Free: Assembly Reliability-III

- CSP 144 & 196, 0.8 mm (Sony)
  - No significant in CTFs (-55/125) different surface finish
  - Double-sided lower for both Pb free/Pb
  - Mechanical fatigue on OSP better than Ni/Au
- MAP FPBGA, 179 I/O, 0.8mm (Motorola)
  - Mechanical fatigue: SAC higher CTF
- µBGA® 46 I/O (Tessera)
  - 3,000 cycles (-40/125), no failure. Same as Pb/Sn
  - Effect of high temp exposure on package/board/interface materials need to be considered

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Pb Free: NEMI CONCLUSIONS

- Thermal Cycle Results (-40/125°C, 0/100°C)
  - Lead Free (balls/comp finish-paste alloy) combinations performed equivalent or better
  - Mixed combination
    - Most performed equivalent
    - Two performed worse
    - One better
- Three point bend
  - No differences
- No Electrochemical Migration, IPC-TM-650
- Tin Whisker being investigated
- Many Issues Remains
  - Board ability to withstand higher temp.
  - Component lead finish (tin whisker)
  - Reliability model

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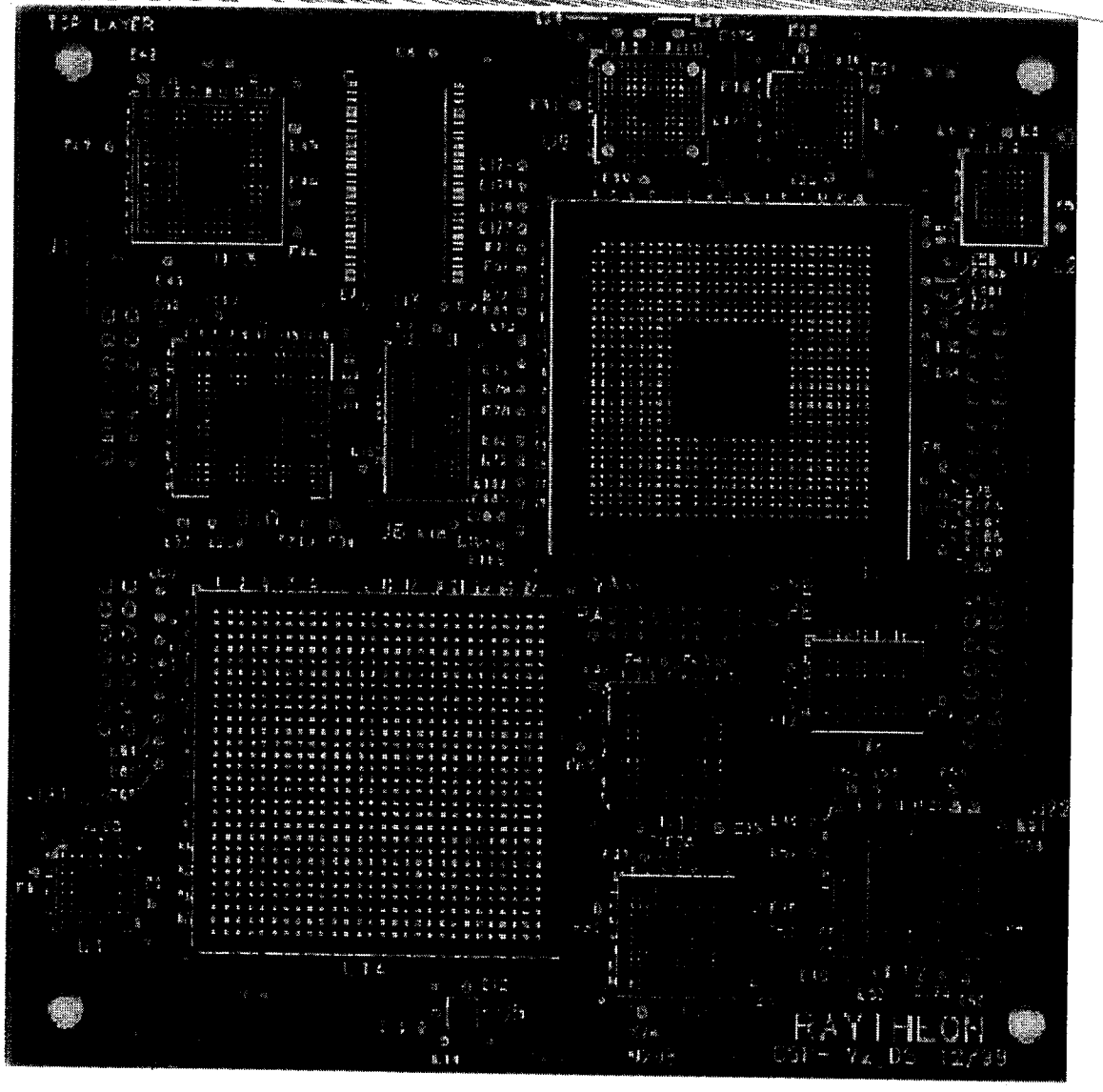
GSP CONSORTIUM

Pb Free & Pb Paste Print/Board Reflow Reliability



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JPL Design of Experiment (DOE)

- Package Pattern from 40 I/O, 10 mil to 50 mil
  - Flip chip, fine pitch, flipchip BGA
- Paste Types: No Lead & No Clean
  - Type III and Type IV
- Stencil Thickness
  - 3 , 4.65, and 5.65 mils
- Squeegee Stroke
  - Forward/Backward
- Total of 48 Runs (Test)

- Reflow Profiles
  - Eutectic & No lead
- Number of reflows
  - 1, 3, and 20

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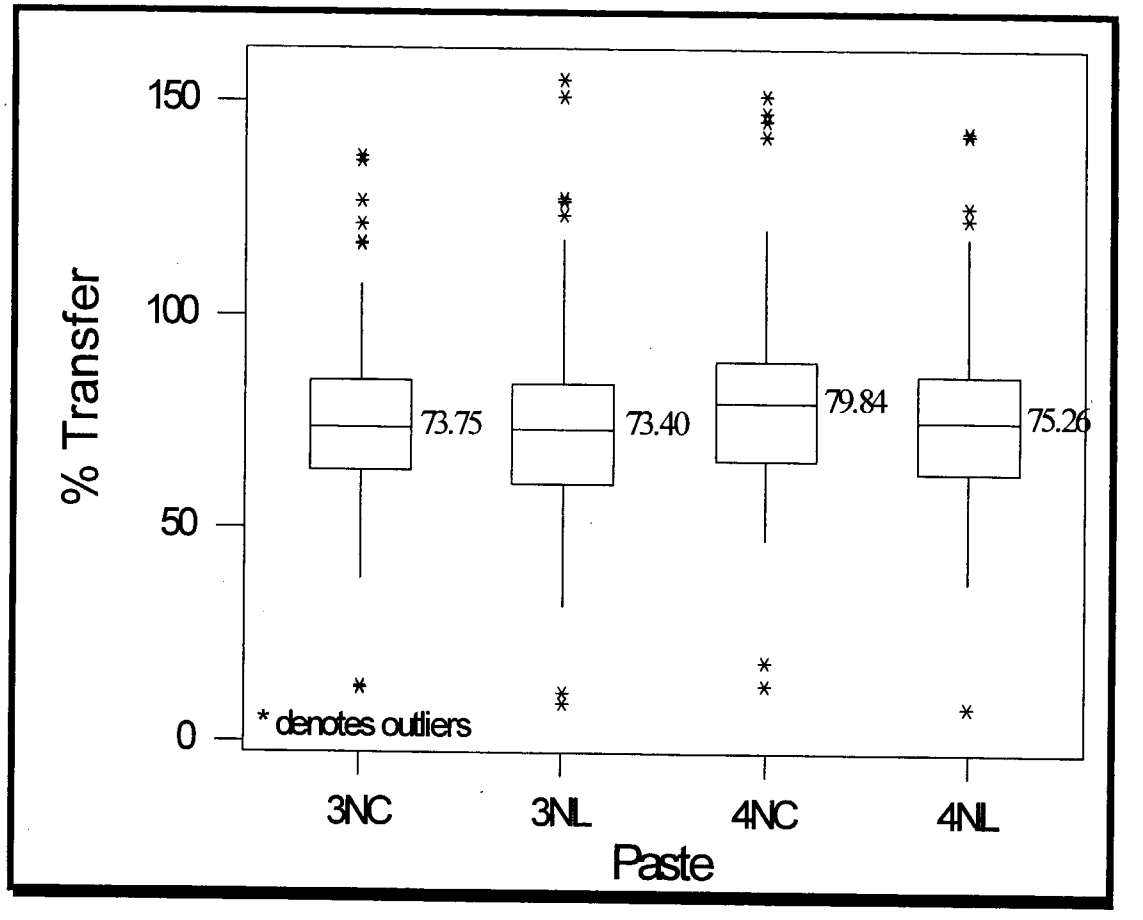
DOE: Paste Print Results



- Paste transfer >60% for all. 3mil stencil is the best.
- No clean slightly better than No lead

Source: JPL CSP/RIT Collaboration

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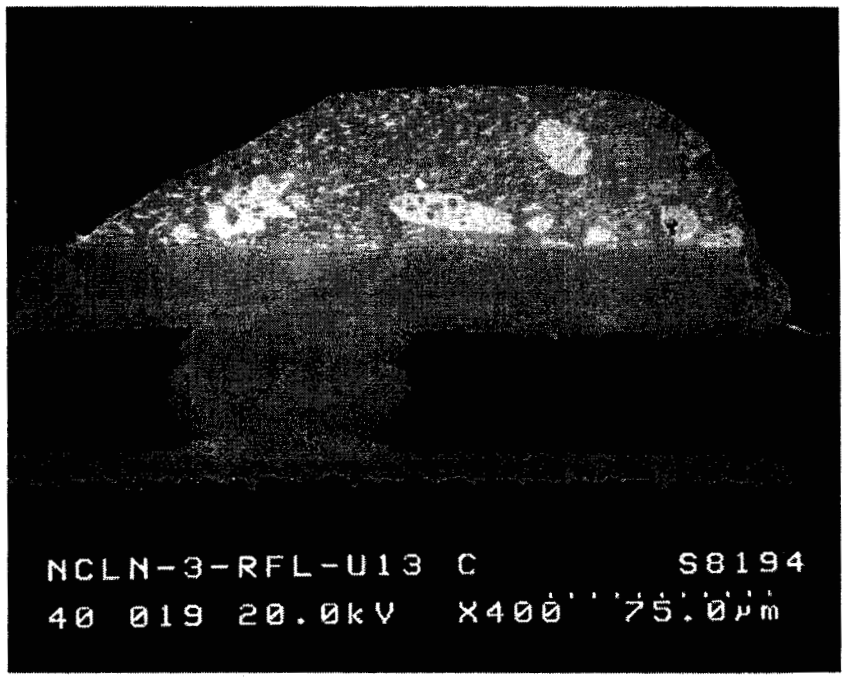
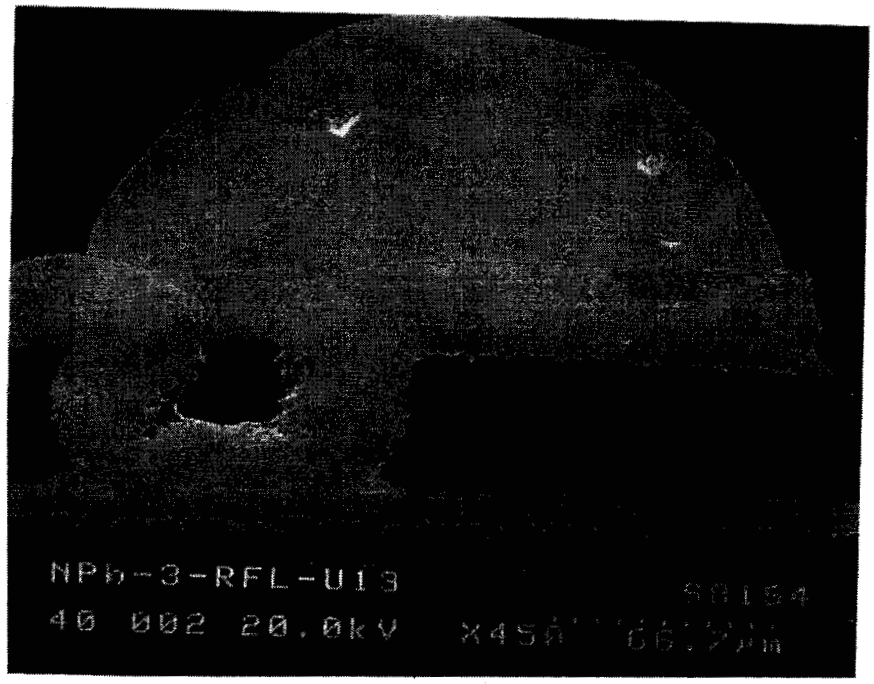
JPL Board Integrity/Solder Microstructure- 3 Reflows

- Slight increase in microvia/PTH daisy chain resistance
- Microstructure change as expected



No Clean (Pb/Sn)



No Lead

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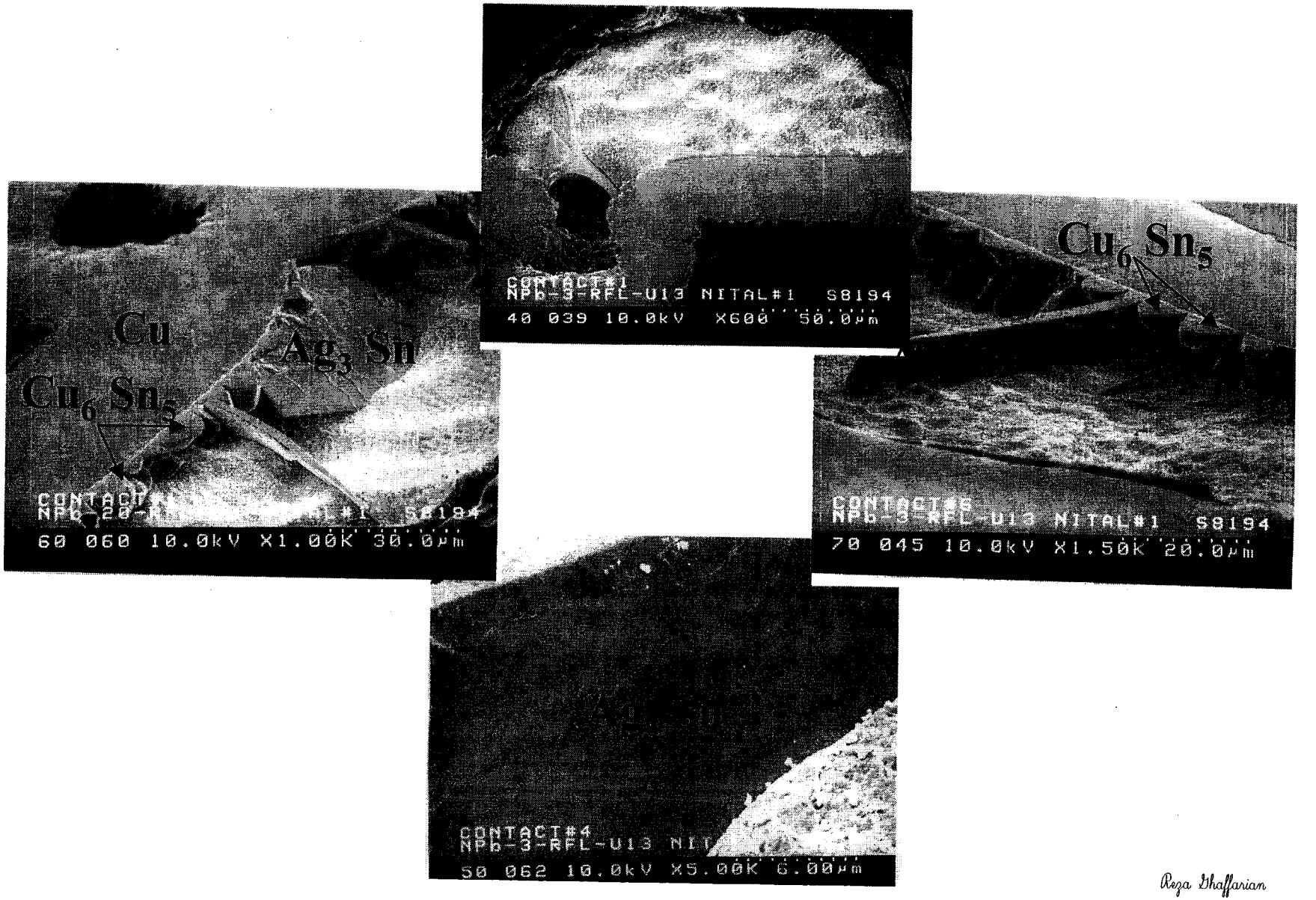
JPL No Lead Solder Composition- 3 Reflows



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CONCLUSIONS

- Commercial Implementation
  - Extensive investigation by industry, consortia
  - Issues: transition period, package thermal resistance, choice of paste, compatibility with underfill, etc.
- High Reliability
  - Limited study
    - NASA Electronic Parts and Packaging Program (NEPP) initiated some activity
- COTS Packages
  - Obsolescence, PEM & higher temp reflow, reworkability, etc.
  - New/old issues, e.g. tin whisker, board finish
- Thermal Cycle Performance
  - Behavior creep density level dependence
- Mechanical performance
  - Extreme mechanical environment
- Quality Assurance
  - Changes in inspection criteria, inspection for area array

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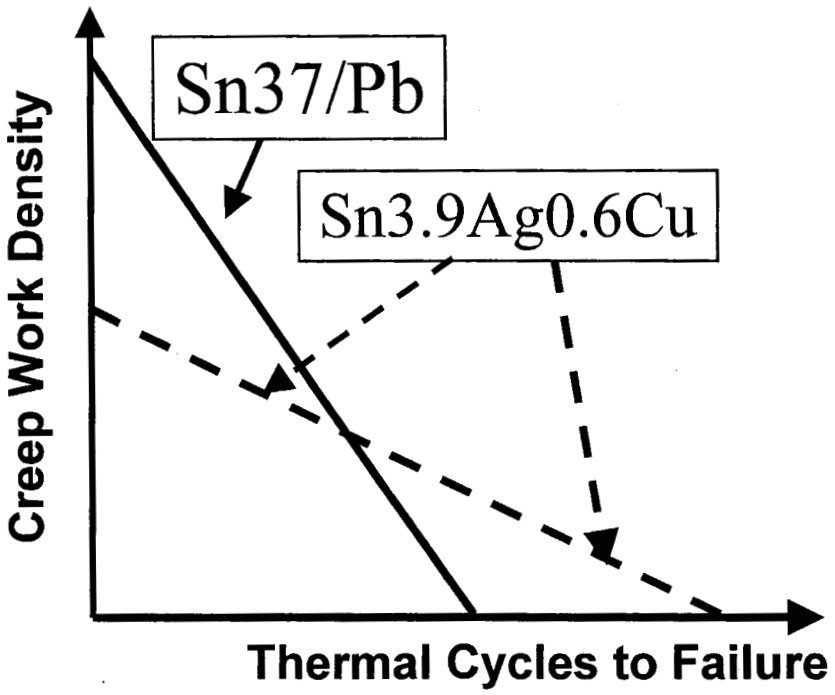
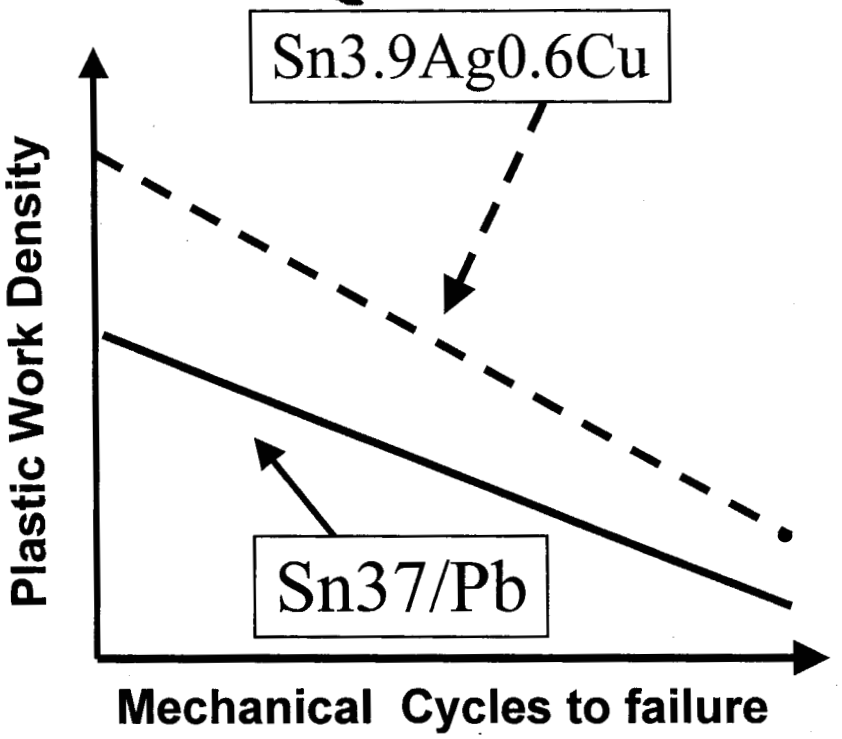
Thermal vs Mechanical Cycles





- Thermal Cycle: Pb-free > Pb only for Low Creep
  - Higher cycles to failure for matched PBGA. Worse for CBGA.
- Mech Cycle: Pb-free > Pb for Most Plastic Ranges

Adapted from NCMS/CALCE/Fraunhofer Institute

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Acknowledgments

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In-kind contributions of team members

CSP CONSORTIUM

Contribution by

RIT University for No Lead Paste Study

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