Virtual Research Presentation Conference

Cell Library Assurance for Strong ASICs

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Program: Strategic Initiative

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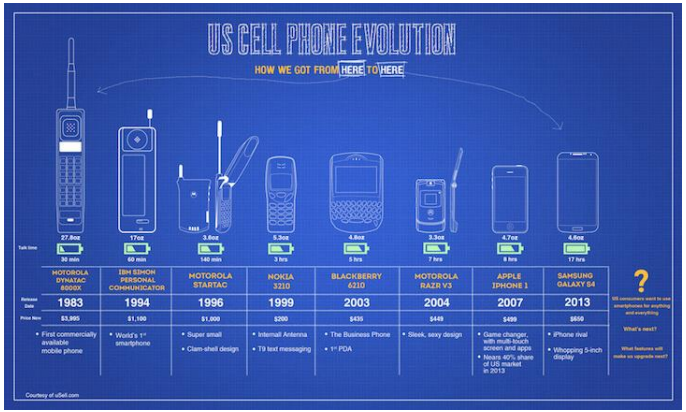
Tutorial Introduction

- Over the last 35 years, we saw miniaturization and automation transforming all aspects of our every day lives with the arrival of cell phones with powerful computing and communication in our hands and smart appliances to handle operations from ordering groceries to water the plants in our homes .
- Such miniaturization and automation (autonomy) can also powerfully transform our space mission, but the commercial electronics underlying commercial miniaturization and automation do not have sufficient reliability and space environmental tolerance to be directly inserted into our systems.
- Our missions are still primarily relying on dated but reliable and space tolerant military grade electronics. The performance gap between the two types of electronics is already orders of magnitude and still growing.
- We have to find ways to bridge that gap.



Problem Description

- The push for miniaturization and autonomy is unachievable with current military grade digital electronics.
  - Performance, package density and power efficiencies (SWaP) is to date only achievable with commercial electronics
  - Reliability and radiation hardness is insufficient
- JPL has a path for high performance processors (HPSC, Snapdragon, RAD 5545), however ~80% of remaining electronics have no viable high performance option.
- This R&TD seeks to prove that JPL can build modern ASIC's in-house by
  - selecting a high performance commercial fab technology with inherently rad tolerant features
  - using existing automotive cell library specifically developed for high reliability and requires longevity of fabrication resources
  - leveraging partnerships with universities, NASA and other government research groups, and commercial design houses to consolidate learning and effort thus increasing likelihood of success

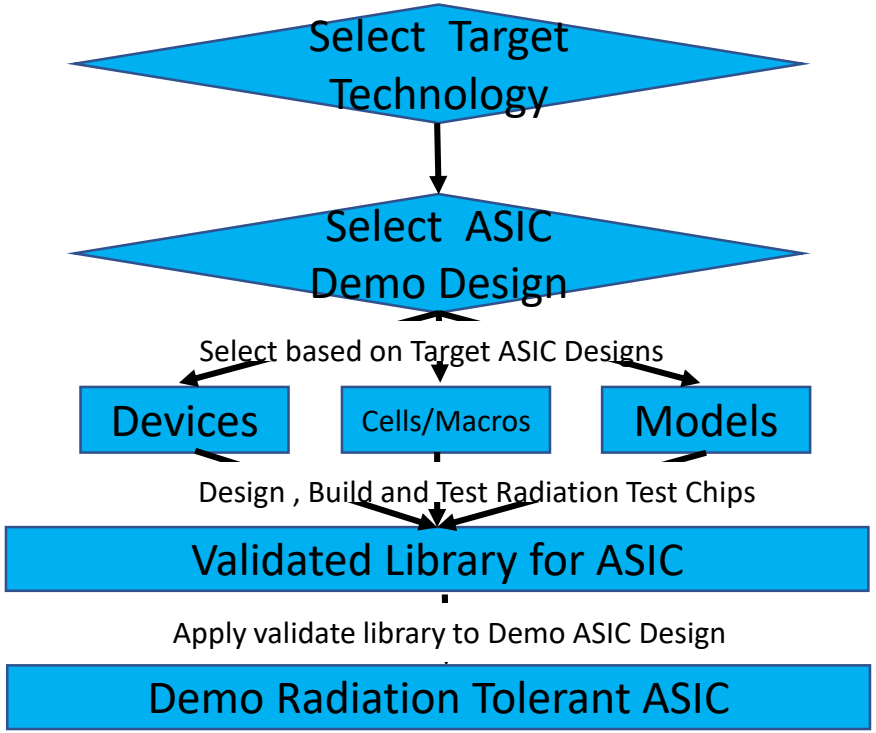
Methodology

To develop an upfront ASIC assurance strategy utilizing standard cells and foundry provided macros

1. A cell and macro library for radiation assurance is to be developed in a contemporary 22nm technology to support digital, analog, mixed signal and RF ASICs.

2. Elements of the library is selected, built and tested to provide baseline data to enable strong radiation tolerant ASIC development in JPL. This effort may require establishing models to enable extrapolation of data from the selected elements to the library as a whole.

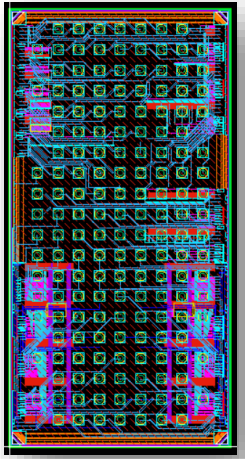
3. The cell library-based ASIC assurance would be demonstrated by the design and test of a radiation tolerant demonstration ASIC based on the validated cell library.



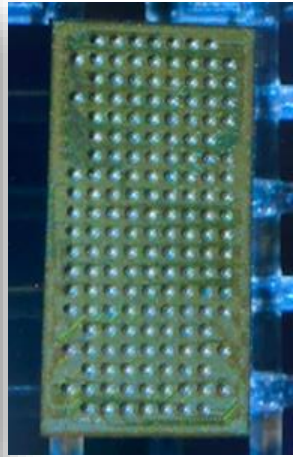
Results

- Selected 22nm automotive technology cell library and installed in JPL servers
- Designed and completed fabrication of a first radiation test chip to evaluate the radiation performance of this technology for JPL
  - Chips contains 13 structures including ring oscillator, inverter chain shift register chain and SRAMs for the investigation of various radiation effects
- Established partnership with multiple universities, government entities, and design houses with interest in this 22nm technology and created information sharing pathways.
- Begun transistor level study of total ionizing dose effects on the technology with university partner

JPL's 22nm Test Chip 1
Area: 3.0 mm x 1.5 mm
167 C4 bump pads



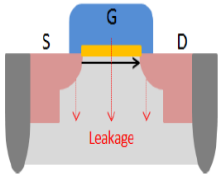
Top Level Design Layout



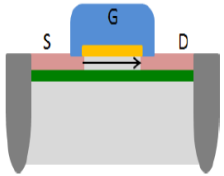
Completed Die With bumps

APPENDIX

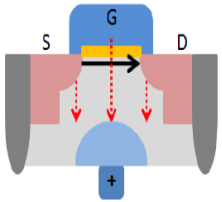
The Benefits of Global Foundry 22nm Node Automotive Library

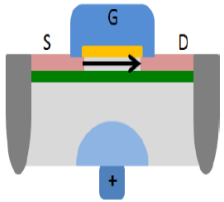


Planar Bulk Transistor



Planar FDSOI Transistor with "green" Insulator layer





Effects of Body Biasing in Bulk Transistor and FDSOI Transistor

- **Performance-** modern technology in full production and capable of supporting high density and high performance digital design, also with mixed signal, SOC, memory, RF and other capabilities
- **Inherent Radiation Tolerance Features-** silicon-on insulator process provides isolation from wells to block vertical latch-up paths and smaller connected silicon volume for single event radiation advantages. Deep submicron transistors also expected to be insensitive to TID
- **Reliability and Longevity-** automotive certified 22FDX - closer to Hi Rel than commercial
  - **Temperature Range** -40C to +125C matching MIL SPEC high temperature
  - **Tighter Process Control** for reduced lot to lot variation, thus reduced radiation performance variation
  - **More Stringent Qualification** resulting in higher baseline reliability than standard commercial libraries
  - **Production Longevity-** typically 10 year or more is required for automotive thus a better match to our longer design cycles