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Small Satellites Demand Innovation in Reliability

The Challenge of too Little Information

- Most COTS components are high quality
- Long term reliability for highly scaled CMOS is a concern
- Radiation data is typically unknown
- Design, process material, construction, etc. Information is useful, but vague
- Heritage rarely applies to COTS
 - No traditional lot traceability, frequent undisclosed design changes

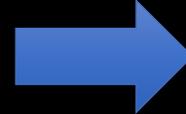
Part Level Information Flow

On a project the size of MSL:
~2000 unique electronic components



Test Data:

- Mil-Std 883
- Data Sheets
- Flight Heritage
- Radiation Tests
- Screening
- Burn-in
- Life test
- Stress tests
- ...



PartList	Act	Rev	PartNum	ProcName	PartDesc	Generic	Package	D	Bur	Cat	SP	Comment	Stat	Qty	Mkt	R	Sp	A	Sp	T	No	Fulfill	Need	Act	
1			CDR01BP1C	CDR01BP Capacitor,	1CDR01	CDR01	C	FL				PIE: 2/26, Res1 12 5 17 16 76 76(0)2014													
2			CDR32BK1C	CDR32BK Capacitor,	1CDR32	CDR32	C	FL				Ords 1 5 6 11 11(0)2014													
3			CDR32BK22	CDR32BK Capacitor,	0CDR32	SM05	C	FL				Ords 6 5 12 42 42(0)2014													
4			CDR33BK47	CDR33BK Capacitor,	0CDR33	SM05	C	FL				PIE: 4/8/1 Ords 12 5 17 77 77(0)2014													
5			CWR09NC2	CWR09N Capacitor,	2CWR09	CWR09-C		FL				PIE: 4/8/1 Ords 23 5 23 138 138(0)2014													
6			JANS1N446	JANS1N4 DIODE, 15V	1N4469	A-MELF,D		FL				Ords 15 5 19 25 100 94(-6)2014													
7			JANS1N632	JANS1N6 11V Zener Di	1N6325	B-MELF,D		FL				PIE: 2/18, Ords 9 5 15 60 60(0)2014													
8			RH1009MH	RH1009P 2.5V Referen	RH1009	TO-46, JU		FL				Res1 3 5 9 24 24(0)2014													
9			10268816-I	Diode, Zene 1N757A	DO213-D			FL				Res1 2												0(-18)2014	
10			JANSR2N75	JANSR2N 100V, P-Cha	IRHN597	SMD-0.1Q		FL				PIE: 4/8/1 Ords 30 5 26 176 176(0)2014													
11			JANSR2N75	JANSR2N 100 Volt, 66	IRHN597.1	SMD-0.1Q		FL				PIE: 4/8/1 Res1 24 5 23 143 193(0)2014													
12			JANSR2N222	JANSR2N TRANSISTOR	2N2222AUUB	Q		FL				PIE: Access Ords 73 5 40 405 405(0)2014													
13			D55342K07	D55342K RESISTOR,	1RM1206	RM1206R		FL				PIE: 2/14, Ords 91 5 44 499 499(0)2014													
14			D55342K07	D55342K RESISTOR,	1RM1206	RM1206R		FL				PIE: 2/14, Ords 22 5 22 132 132(0)2014													
15			D55342K07	D55342K RESISTOR,	1RM1206	RM1206R		FL				PIE: 2/14, Ords 12 5 17 77 77(0)2014													
16			D55342K07	D55342K RESISTOR,	1RM1206	RM1206R		FL				PIE: 2/14, Ords 24 5 23 143 143(0)2014													
17			D55342K07	D55342K RESISTOR,	1RM1206	RM1206R		FL				PIE: 2/14, Ords 12 5 17 77 77(0)2014													
18			D55342K07	D55342K RESISTOR,	1RM1206	RM1206R		FL				PIE: 2/14, Ords 2 5 8 18 18(0)2014													
19			D55342K07	D55342K RESISTOR,	1RM1206	RM1206R		FL				PIE: Part 1 Ords 66 5 38 368 368(0)2014													
20			D55342K07	D55342K RESISTOR,	1RM1206	RM1206R		FL				PIE: Lishe Ords 12 5 17 77 77(0)2014													
21			D55342K07	D55342K RESISTOR,	1RM1206	RM1206R		FL				PIE: Lishe Ords 12 5 17 77 77(0)2014													
22			D55342K07	D55342K RESISTOR,	1RM1206	RM1206R		FL				PIE: 2/14, Ords 2 5 8 18 18(0)2014													
23			D55342K07	D55342K RESISTOR,	1RM1206	RM1206R		FL				PIE: 2/14, Ords 6 5 12 42 42(0)2014													
24			M55342K05	M55342K RESISTOR,	1RM2512	RM2512R		FL				PIE: 2/14, Ords 12 5 17 77 153(0)2014													
25			M55342K06	M55342K RESISTOR,	1RM2512	RM2512R		FL				PIE: 4/8/1 Ords 4 5 10 30 30(0)2014													
26			RH1498MW	RH1498M Micropower	RH1498	GDFP1-HU		FL				Ords 21 5 22 127 127(0)2014													
27			9962R8673	9962R86 Microcircuit,	LM139A	GDFP1-HU		FL				PIE: 2/14, Ords 12 5 17 77 77(0)2014													
28			RH1078MW	RH1078M Micropower	RH1078	GDFP1-HU		FL				Res1 5 5 11 7 32 32(0)2014													
29			D55342K07	D55342K RESISTOR,	1RM1206	RM1206R		FL				PIE: 2/14, Ords 4 5 10 30 30(0)2014													
30			D55342K07	D55342K RESISTOR,	1RM1206	RM1206R		FL				PIE: 2/14, Ords 4 5 10 30 30(0)2014													

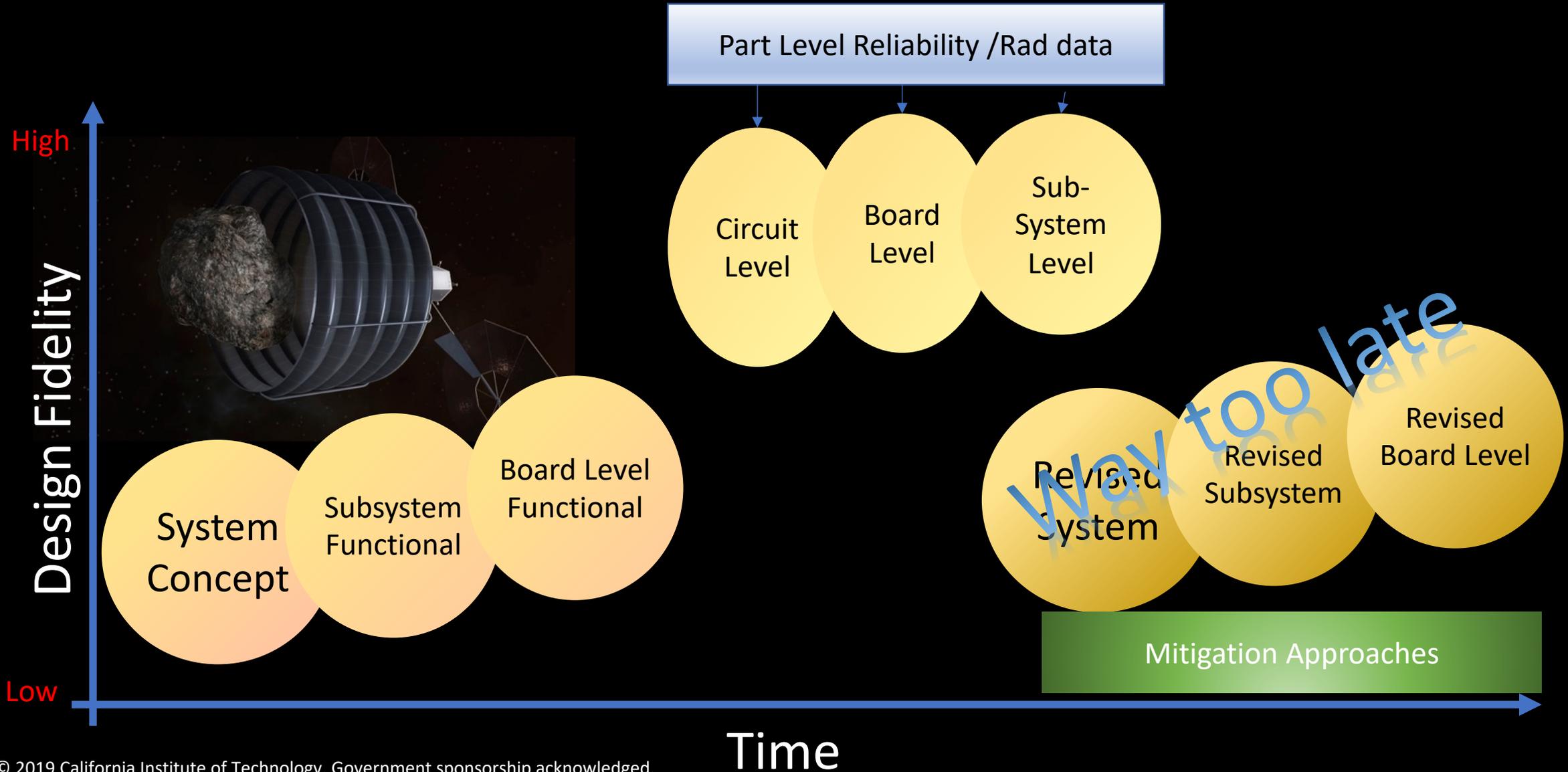
~100's components don't meet Mil-Std



Impact to project?
Likelihood?
Uncertainty?

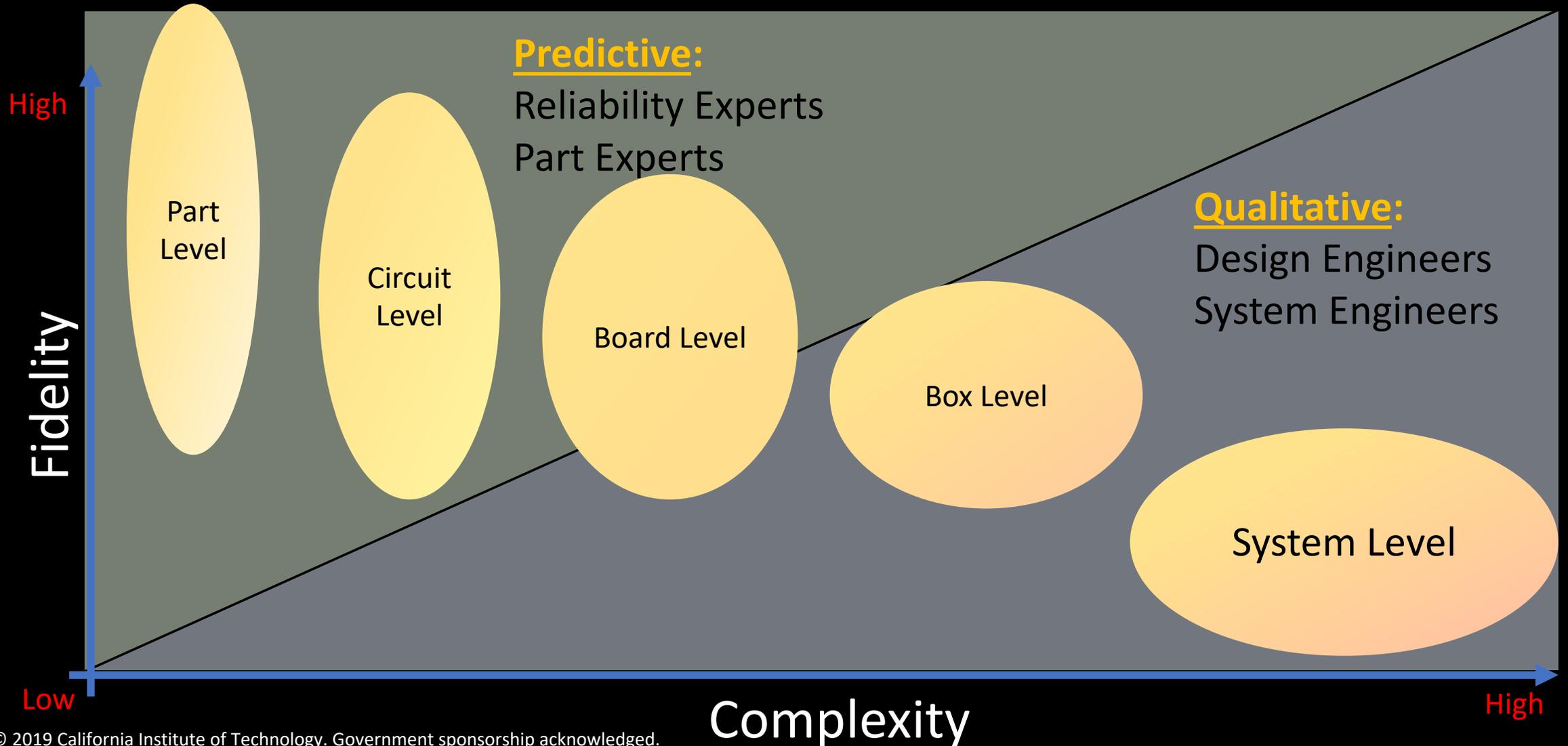
Mission Success is defined as Capabilities at Spacecraft level-
Never by radiation effects!

Notional Design Flow vs. Reliability



Complexity vs. Model Fidelity

Crossing Expert Domains



Lowest Level of Fidelity: COTS Radiation Guideline

1	Guideline for the Selection of COTS Electronic Parts that will operate in a Space Radiation Environments	1-1
2	Radiation-Based Selection of COTS Devices for JPL Flight Systems: Field Programmable Gate Arrays (FPGA)	2-2
2.1	Introduction	2-2
2.2	FPGA Technology Overview	2-2
2.3	Radiation Effects on FPGA Technologies	2-3
2.4	References	2-12
3	Radiation-Based Selection of COTS Devices for JPL Flight Systems: Non-Volatile Flash Memories	3-1
3.1	Introduction	3-1
3.2	Non-Volatile Flash Memories Technology Overview	3-1
3.3	Radiation Effects on Non-Volatile Flash Memories Technology	3-4
3.4	References	3-12
4	Radiation-Based Selection of COTS Devices for JPL Flight Systems: ADCs and DACs	4-1
4.1	Introduction	4-1
4.2	References	4-11
5	Radiation-Based Selection of COTS Devices for JPL Flight Systems: Devices used in Power Systems	5-1
5.1	Introduction	5-1
5.2	Radiation effects for power system parts	5-1
5.3	Summary of Mitigation Methods	5-7
5.4	References	5-9
6	Radiation-Based Selection of COTS Devices for JPL Flight Systems: Processors	6-1
6.1	Introduction	6-1
6.2	Processor Technology Overview	6-1

technology nodes). The primary design tradeoff for using these devices is that they are volatile, requiring an external configuration memory to store the configuration data; this adds design overhead, real-estate, power and additional reliability concerns to the system.

2.2.2 Flash-based architecture

A flash-based FPGA architecture replaces SRAM configuration elements with floating gate flash technology. The primary benefit being the configuration is non-volatile, meaning it is live on power-up and does not require external memory. The flash process is typically more efficient in terms of area and power. One drawback to flash-based FPGA is that the number of erase-program cycles is limited, unlike SRAM. However, that number is typically in the 10,000 to 100,000 range, which is more than enough for most space applications. Another drawback is that it is a non-standard CMOS process, meaning it will lag behind the aggressively scaled SRAM architecture. Microsemi, formerly Actel Corporation, is the main manufacturer of flash-based FPGAs.

2.2.3 Antifuse-based architecture

Finally, antifuse-based FPGAs implement one-time-programmable (OTP) switches to route and define logic elements. The advantages to this technology are its non-volatility and very small area overhead. The clear disadvantage is the inability to reprogram functionality, and the non-standard CMOS process required to produce the FPGAs. Microsemi and Aeroflex are the two primary manufacturers of antifuse FPGAs.

2.3 RADIATION EFFECTS ON FPGA TECHNOLOGIES

This section provides an overview of radiation effects on the three main FPGA technologies. While not intended to be a comprehensive review of radiation effects, the goal is to provide enough information to aid in the selection of the right COTS FPGA technology for a particular JPL flight mission and/or application.

2.3.1 Destructive Effects – Single Event Latchup – Any FPGA Containing CMOS

2.3.1.1 Overview

CMOS technology is potentially susceptible to single event latchup (SEL). SEL susceptibility in these devices can range from complete immunity, to very rare events, to extremely frequent and/or destructive events.

Rad Guidelines Codified in an Expert System

Small Sat Radiation Tool Utilities

Home Search Parts Plot Flux vs LET

PlotFluxvsLET

1. Upload LET File

convert.let

2. Cross-section Parameters

$$F(x) = A(1 - e^{-(\frac{x-x_0}{W})^s})$$

Plateau Cross-Section, A:

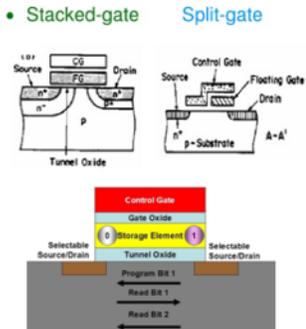
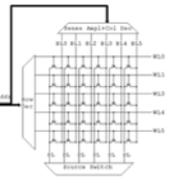
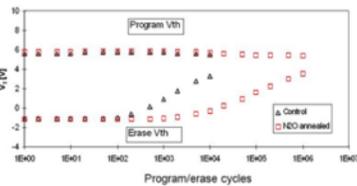
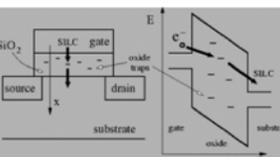
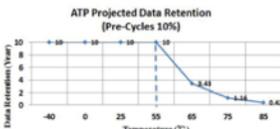
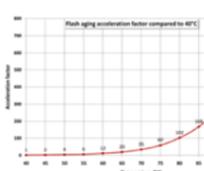
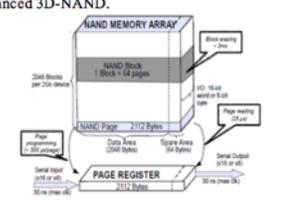
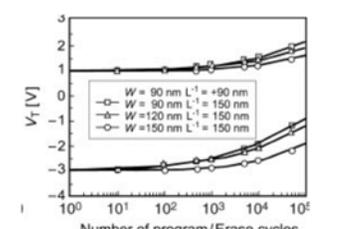
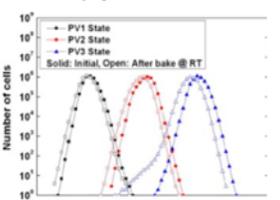
Onset Parameter, x_0 :

Width Parameter, W:

Dimensionless Exponent, s:

LET (MeV-cm ² /g)	Flux (Right Y-axis)	Weibull Cross Section (Left Y-axis)
0	1e+4	1e-3
10	~5e+3	~5e-2
20	~2e+3	~1e+0
30	~1e+3	~1e+0
60	~5e+2	~1e+0
102.61	~1e+1	~1e+0

JPL Lowest Level of Fidelity: COTS Reliability Guideline

M-2 Microcircuits							
Type	Overview/General Construction	Circuit Applications	Common Failure Modes	Failure Mechanisms	Technology Trends	Reliability	Recommendations
<p>NVM, NOR Flash Single-level Cells</p>	<p>split-gate-based. Floating-gate-based and split-gate-based use a floating poly-Si gate to store the data while the charge-trapping type uses nitride (Si3N4) for charge storage. They all employ channel hot electron mechanism to program and tunneling for erase. Generally available in TSOP and BGA packages.</p> <p>• Stacked-gate Split-gate</p> 	<p>its random access capability. Faster read and write compared to NAND Flash. Technology of choice for embedded applications.</p> 	<ul style="list-style-type: none"> Data retention due to charge loss at higher temperature (>150°C) Over-erase bit causing excessive bit line leakage Degradation of charge pump efficiency Gate oxide rupture 	<p>of trap sites and interface states inside oxide) from P/E cycling is the root cause of failures.</p> <ul style="list-style-type: none"> Stress induced leakage current (SILC) attributed to data retention failure 	<p>data retention compared to both floating-gate and charge-trapping types. However, its density (~64Mb) is relatively small as compared to floating-gate and charge-trapping (~1 Gb). The major Floating gate vendors are Micron, Atmel and Intel. Split gate vendor: Microchips (formally SST) Charge Trapping (Mirror bit) Vendor: Cypress (formally Spansion)</p>	<p>quality of the tunnel oxide. They are sensitive to P/E cycle, extended read conditions.</p> 	<p>PE cycles and operating temperature. easily degraded under excessive radiation. Recommend a derating factor of 0.75 rated endurance cycles from manufacturer. Use Hamming ECC at a minimum. Per cycling at min, max & nom. Vcc to fully over life for critical applications.</p> 
<p>NVM, NOR Flash Multi-level Cells</p>	<p>Only the Floating-gate and Charge-trapping type offer MLC (two bits per cell), e.g., Intel's StrataFlash and Spansion's mirror-bit technologies. Intel's StrataFlash employs different charge density in the floating gate to store 2 bits of information. Spansion's mirror bit employs charge trapped near the source and drain junctions to store 2 bits max. of information.</p>	<p>Widely used for code storage due to its random access capability. Faster read and write as compared to NAND Flash. Technology of choice for embedded applications.</p>	<ul style="list-style-type: none"> Read window closure due to excessive P/E cycle. Data retention failure due to charge loss at higher temperature (>150°C) Over-erase bit Over-program bit Gate oxide rupture 	<ul style="list-style-type: none"> Electron trapping and charging attributed to cycling-induced failures. Stress induced leakage current (SILC) attributed to data retention failure. 	<p>Currently not widely offered by the vendors. MLC is typically offered for NAND-based Flash.</p>	<p>MLC NOR is generally less reliable than SLC. Typically the endurance spec will show a 10x difference (10K for MLC, 100K for SLC).</p>	<p>MLC Flash is not recommended for use in applications. Extra consideration need ECC.</p>
<p>NVM, NAND Flash Single-level Cells</p>	<p>The basic storage cell in a mainstream NAND flash is similar to NOR. The key difference is how these storage cells are connected. For NAND, there are a total of 16 to 32 storage cells connected in series with two select transistors at the top and bottom of the string. NAND employs Fowler Nordheim tunneling mechanism for both program and erase. NAND SLC has a 2D planar topology compared to the more advanced 3D-NAND.</p> 	<p>Widely used for data storage, e.g., thumb drive, solid state disk drive) due to its low bit cost (< \$1 per Gb).</p>	<ul style="list-style-type: none"> Read window is widening due to excessive P/E cycles. Charge loss leading data retention failure at high temperatures. Degradation of charge pump efficiency under radioactive environment. 	<ul style="list-style-type: none"> Electron trapping and charging attributed to cycling-induced failures. Stress induced leakage current (SILC) attributed to data retention failure. High voltage operations resulting in severe cell-cell interference and program disturbs. 	<p>2D NAND encounters scaling challenges at 10 to 19 nm node. Vendors have gradually migrated towards 3D-NAND topology to continue with the NAND scaling.</p>	<p>NAND shares common reliability problems with NOR. Cycling-induced oxide degradation is one major issue.</p>	<p>SLC NAND is considered to be more reliable than MLC NAND. The endurance spec for typically rated up to 10K cycles. Rec factor of 0.75 for Vmax, Imax and rate from the manufacturer's data sheet. A chip is typically introduced for gigabyte (>Gb) for efficient and reliable data management (garbage collection, bad blocks). Use Reed-Solomon ECC. Perform end min, max & nom. Vcc to fully characterize for critical applications.</p>
<p>NVM, NAND Flash Multi-level Cells</p>	<p>Multi-level cells in 2D-NAND still adopt the SLC NAND string structure. The key difference is how the cells are programmed to different levels. Three types of multi-level cells are available - MLC (2 bits/cell), TLC (3 bits/cell) and QLC (4 bits/cell). Recently 3D NANDs are being introduced with 48 Gb/mm^2.</p>	<p>Widely used for data storage, e.g., thumb drive and solid state disk drive due to its low bit cost (< \$1 per Gb).</p>	<ul style="list-style-type: none"> Read window widening due to excessive P/E cycles. Charge loss leading to data retention failure at high temperature. Degradation of charge pump efficiency under radiative environment. 	<ul style="list-style-type: none"> Electron trapping and charging attributed to cycling-induced failures. Stress induced leakage current (SILC) attributed to data retention failure. 	<p>Transition of 2D-NAND towards 3D-NAND started in late 2016.</p>	<p>Reliability of MLC NAND is worse than its SLC counterpart. An obvious differentiator is the endurance specs: < 1K for MLC versus 10K for SLC.</p>	<p>MLC Flash is not recommended for use in applications. Extra considerations need ECC.</p>

JPL COTS Reliability Codified in Expert System

Automatically retrieves Intel Fab information to predict physics of failure



- Part Database
- Bayesian Estimation
- Circuit Simulation
- Process Factor



ES performs:
Non-Homogenous and Linear α_{PF} adjustment

Prior: λ_{DB}

Likelihood: Results of BE (λ_{BE}) and CS (λ_{CS})
The final result will be adjusted by (α_{PF})

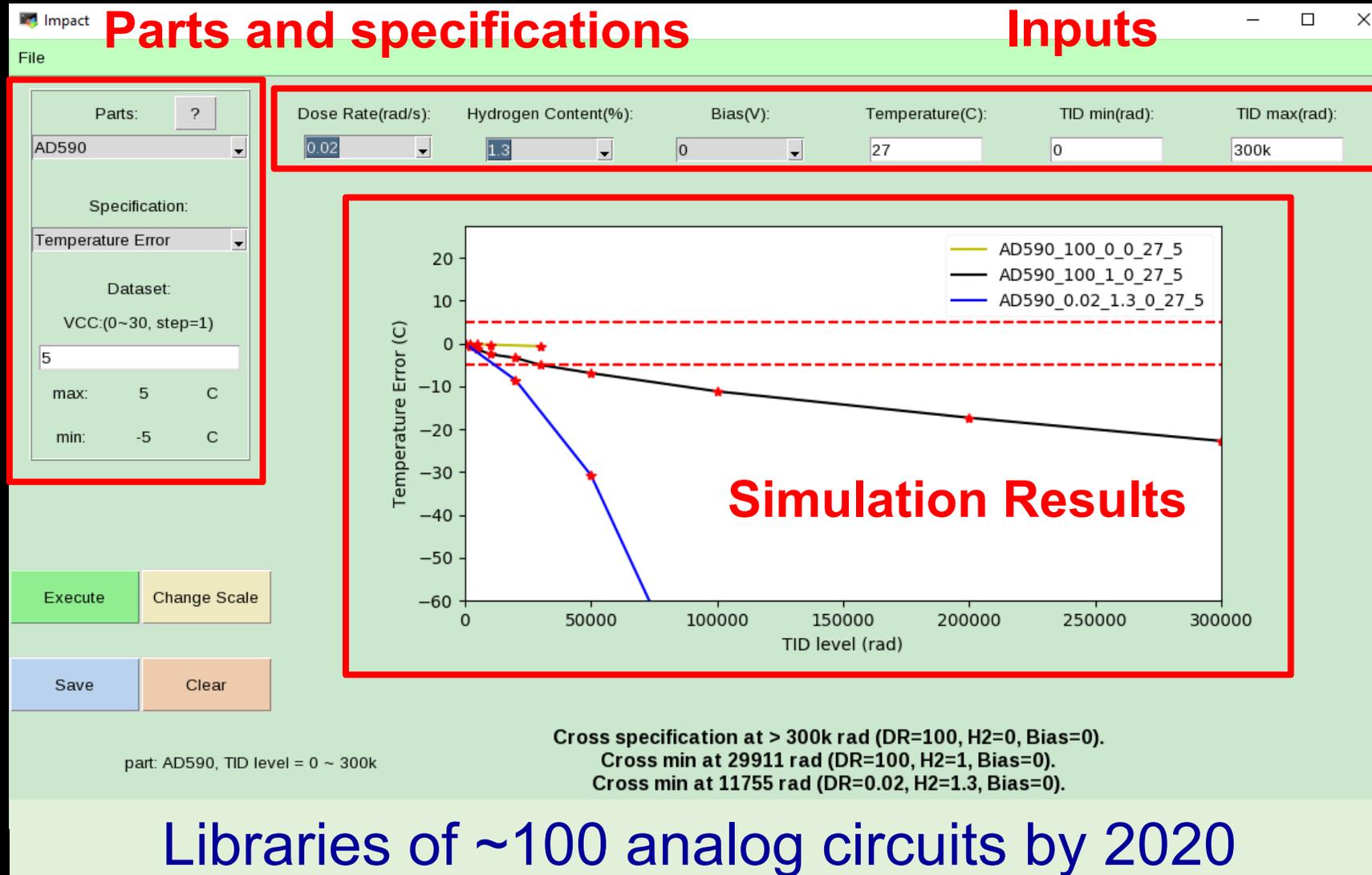
The interface consists of several overlapping panels:

- Main Panel:** Circuit Type (SRAM selected), Technology Node (180 nm selected), Physics of Failure (TDDB, BTI, HCI checked), Mission Time (27778 hrs), Temperature (27 °C). Buttons: SAVE, RUN.
- ADC Failure Criteria Panel:** Effective Number of Bits selected. Parameters: Offset Voltage (6 bits), Threshold Resolution (10 bits), Ideal Resolution (10 bits), Operating Voltage (1.8 V), ENoB Before Degradation (10 bits). Button: SAVE.
- SRAM Failure Criteria Panel (Left):** Standby Power Increase selected. Parameters: Cell Power Increase (100), Power Increase Criterion (0.1), SRAM Size (1024 bits). Button: SAVE.
- SRAM Failure Criteria Panel (Right):** Bit Error Rate selected. Options: Intrinsic SNM (button: INTRINSIC), Degraded SNM (button: DEGRADED). Button: SAVE.

WholeParts

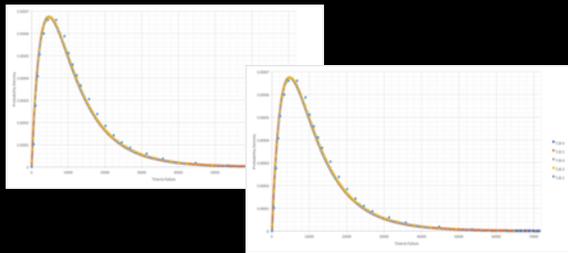
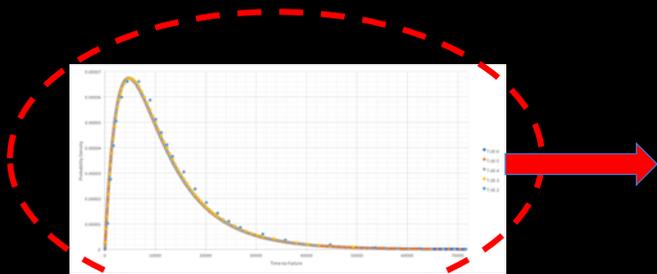
A JPL tool to troll the internet and automatically approve parts for flight
>500,000 parts already in database
>50% of JPL parts are automatically approved

Predictive TID for Analog Devices: IMPACT

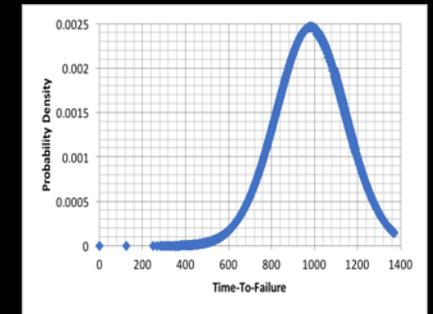
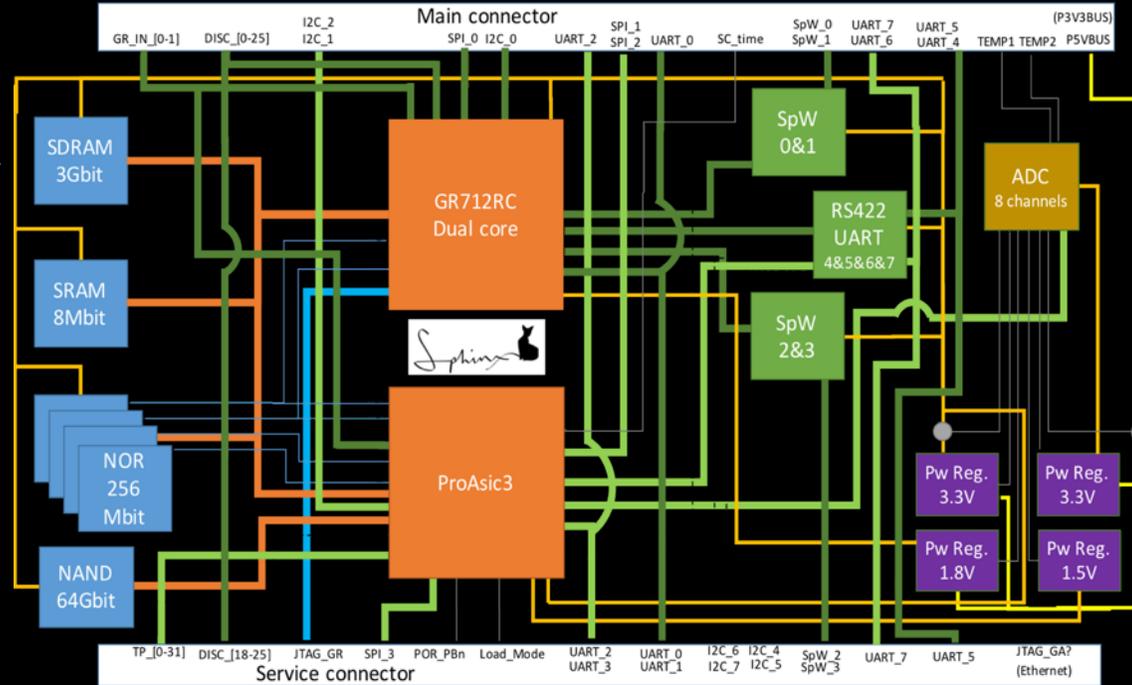


Libraries of ~100 analog circuits by 2020

Predictive Rad Modeling at the circuit/board level



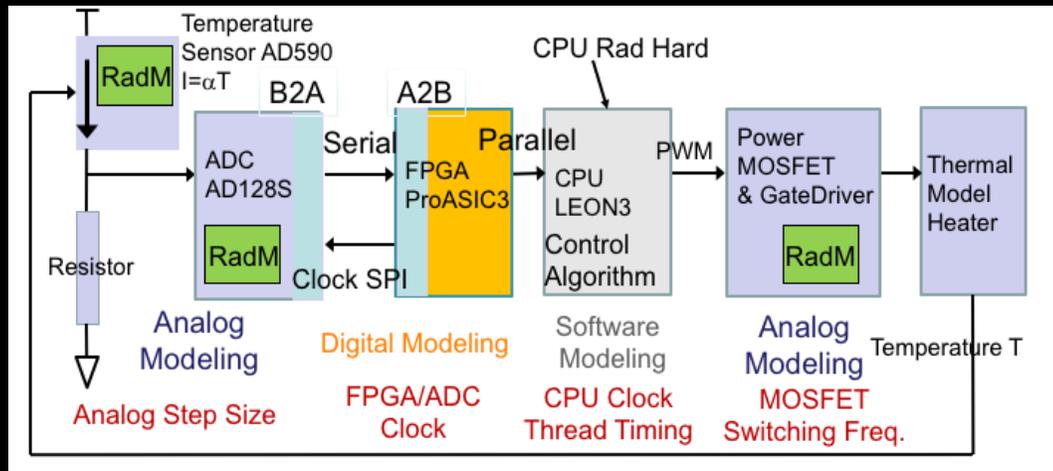
Component Reliability Metrics



System Reliability Metrics

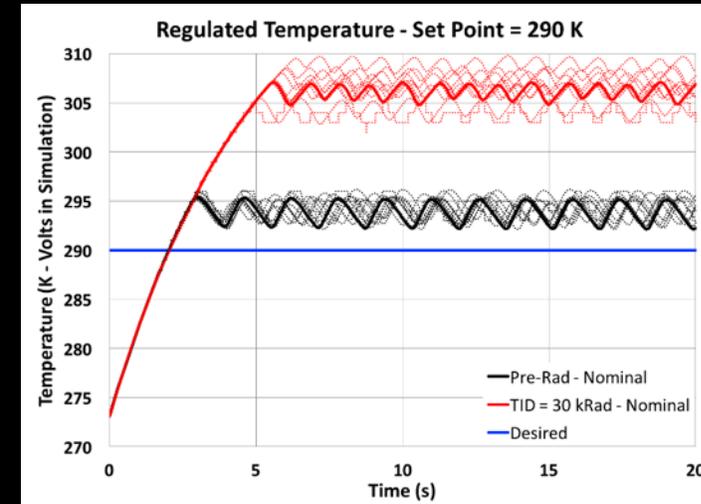
Predictive Rad Modeling at the circuit/board level

Temp. control loop within Sphynx C&DH



Rad modeling embedded in parameter variation

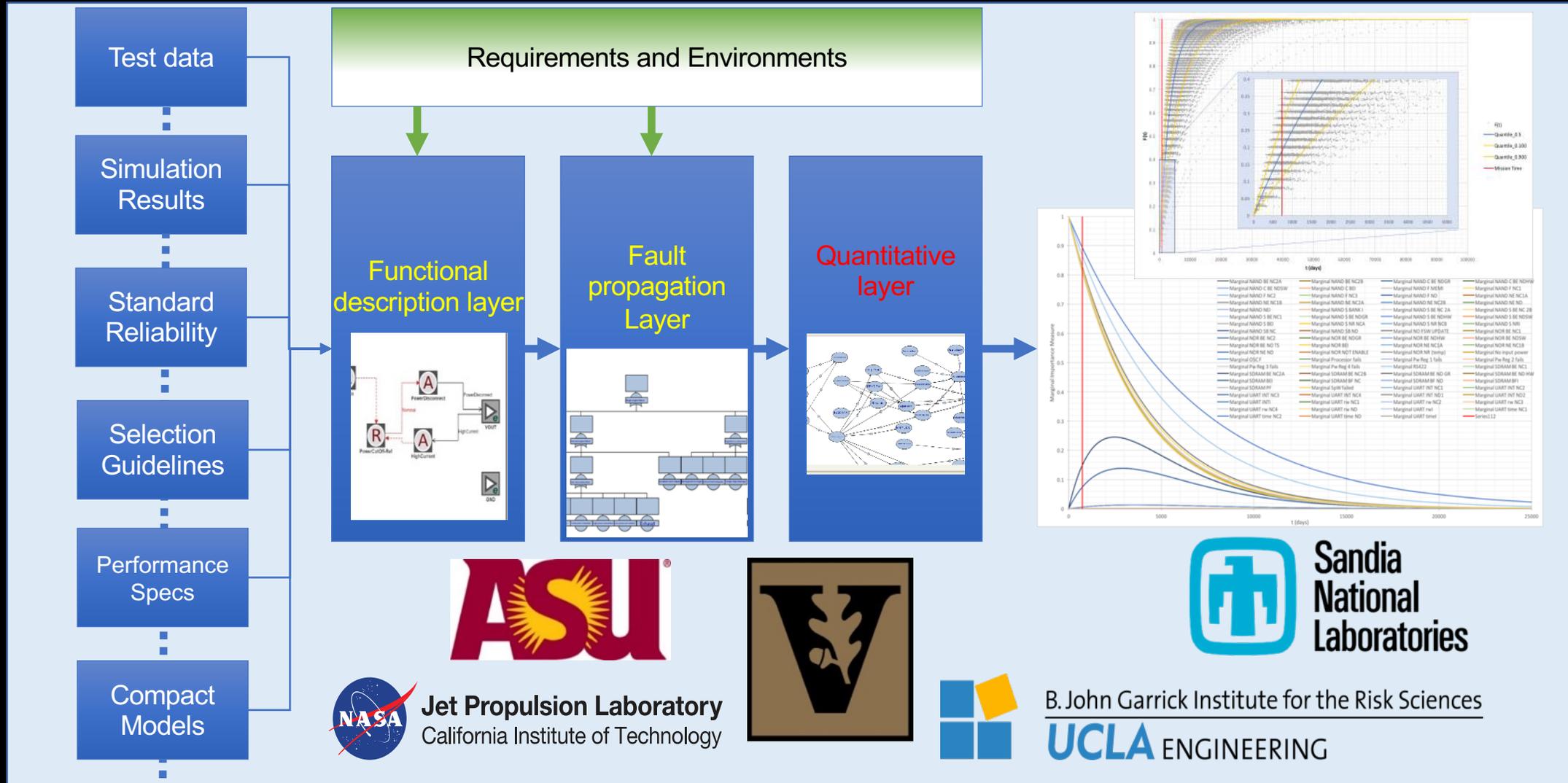
Closed-loop simulation results



Monte Carlo analysis included



System Level Model-based Assurance



Conclusion

The (Unexpected) Benefits of Modeling

- Modeling can be a powerful RHA tool
- Make use of vague information
 - Expert knowledge can flow into model if properly weighted
- Effective way to collect information (standard format, metadata, C.C.)
- Enables information sharing
 - Sharing piles of papers, lists of lessons learned or best practices is cumbersome and discourages adoption
- A guide through a design/development/Ops process
 - Model fidelity needs to be adapted to stages in design