Vision Compute Element FPGAs

Jet Propulsion Laboratory
California Institute of Technology

- HK FPGA (Housekeeping)
  - Burn once RTAX 2000
  - Design and V&V complete
  - FPGA installed on flight CVAC
- VP-E FPGA (Vision Processing – EDL)
  - Reprogrammable Virtex-5 (SIRF)
  - Design and verification complete
  - Final Design Review complete
  - Implemented image processing optimizations to speed up LVS time-line
    - Normalize Image: 1660 MIPS, 20ms/image
    - Feature Selection: 7025 MIPS, 4ms/image
    - FFT Correlation: 5187 MIPS, 740ms/image
    - Image Warp: 3550 MIPS, 134ms/image
    - Spatial Correlation: 6775 MIPS, 457ms/image

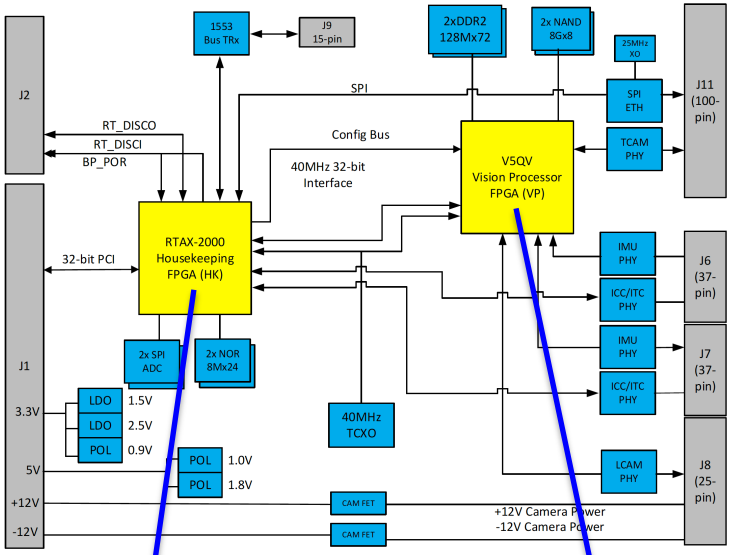

Figure 3-1 CVAC Board Level Block Diagram

HK FPGA (RTAX2000)
- Time sync
- VP configuration
- NOR memory
- 1553
- ICC/ITC
- ADC
- Ethernet

VP-E FPGA (Virtex5)
- DDR2 memory
- NAND memory
- Image Processing
- LCAM interface
- IMU interface

MARS 2020 PROJECT