

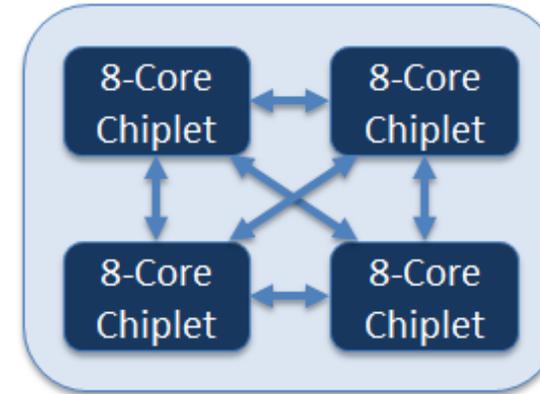
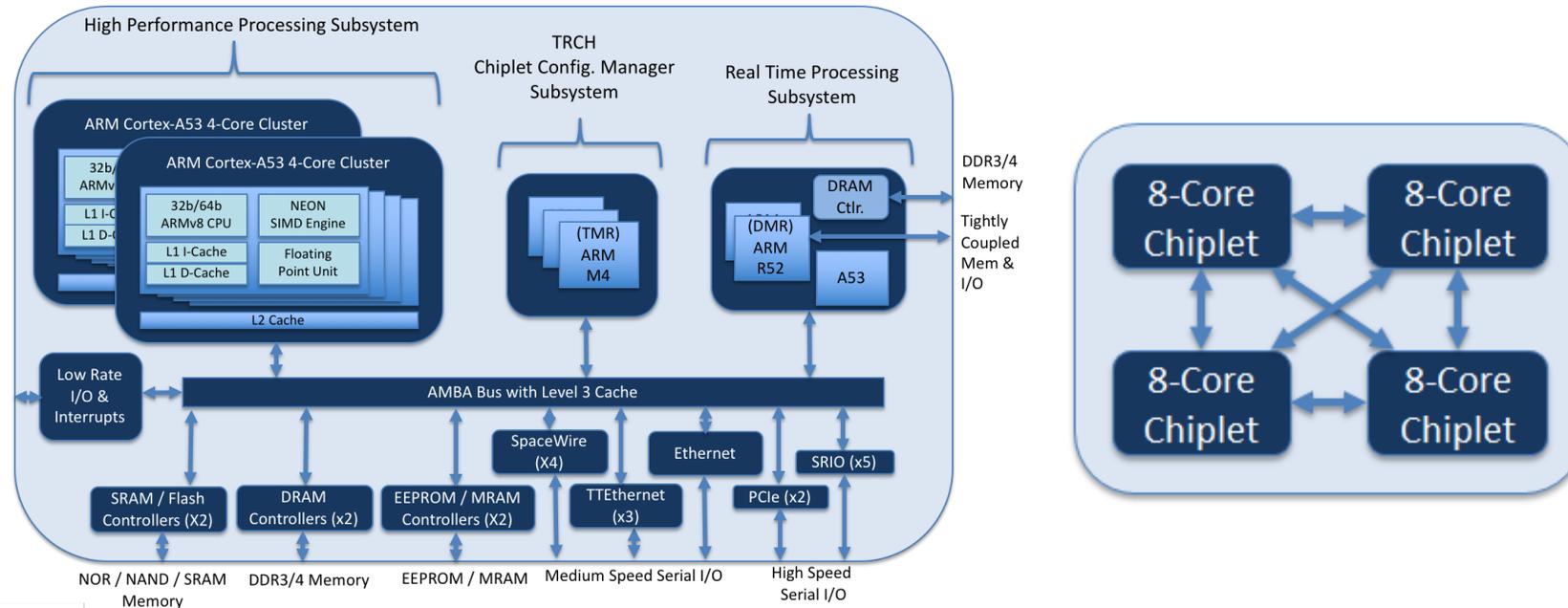


Space Technology Mission Directorate Game Changing Development Program High Performance Spaceflight Computing

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HPSC – Technology Overview

Reinventing the Role of Computing in Space



- **HPSC offers a new flight computing architecture** to meet the needs of NASA missions through 2030 and beyond. Providing on the order of **100X the computational capacity of current flight processors for the same amount of power**, the multicore architecture of the HPSC chiplet provides **unprecedented flexibility** in a flight computing system by enabling the operating point to be set dynamically, **trading among needs for computational performance, energy management and fault tolerance**. This kind of operational flexibility has never been available before in a flight computing system.
- **HPSC has been conceived to be highly extensible**. Multiple **chiplets can be cascaded together** for more capable computing, or HPSC can be **configured with specialized co-processors** to meet the needs of specific payloads and missions.
- **HPSC is a technology multiplier**, amplifying existing spacecraft capabilities and enabling new ones. The HPSC team anticipates that the chiplet will be **used by virtually every future space mission**, all benefiting from more capable flight computing.

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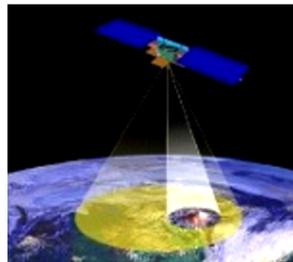
Mission Infusion



- Develop HPSC-based, flight-qualified, single board computers (SBCs), ready for infusion into missions
 - Develop a NASA SBC reference design
 - Integrate the board with at least one set of flight-ready system software
 - Demonstrate flight readiness of the single board computer
 - Fund industry to develop standards-based HPSC SBCs
- HPSC infusion framework



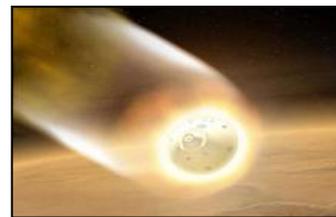
Deep Space



**High Data Rate
Instruments**



Surface Systems



Landing Systems

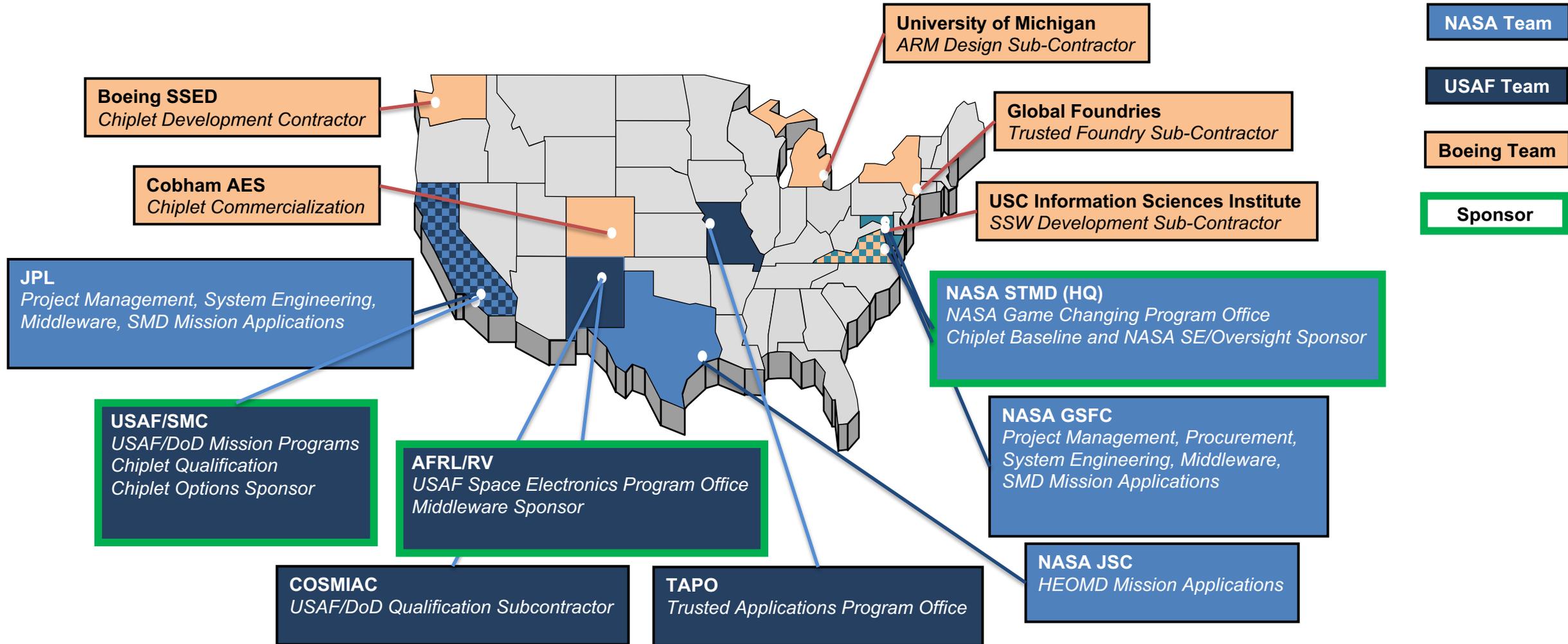


Human Spaceflight



CubeSats + SmallSats

HPSC Partners



Technology Goals and Project Objectives

Technology Goals	
Goal #1	Provide on the order of 100X the computational capacity of current flight processors for the same amount of power.
Goal #2	Provide unprecedented flexibility in a flight computing system by enabling the operating point to be set dynamically, trading among needs for computational performance, energy management and fault tolerance.
Goal #3	Enable capability to be cascaded for more capable computing, or configured with specialized co-processors to meet the needs of specific payloads and missions.

Project Objectives	
Objective #1	Vendor delivery of a rad-hard general-purpose multi-core hardware design and tested chiplets, with flight computing system advances in computational performance, power scaling, power/performance ratio, I/O bandwidth, fault tolerance, and extensibility
Objective #2	Vendor delivery of system software, to include an operating system, a FSW development environment, an emulator, and evaluation boards, along with design documentation and user guide documentation.
Objective #3	NASA delivery of middleware, to provision flight project access to the full range of architectural advantages of a multi-core flight computing system

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Performance

Key Performance Parameters				
Performance Parameter	State of the Art	Threshold Value	Project Goal	Estimated Current Value
Computational	350 MOPS	9 GOPS	15 GOPS	15 GP GOPS + Up to 100 SIMD GOPS
Power Scalability	10W	10W scalable to <1W	7W scalable to <1W	9.1W scalable to TBD W
Performance / Power	20 MOPS/W	0.9 GOPS/W	1.5 GOPS/W	1.5 GP GOPS/W + TBD SIMD GOPS/W
I/O Bandwidth	800 Mbps	40 Gbps (4 SRIO)	60 Gbps (6 SRIO)	240Gps (6 SRIO @ up to 40Gbps/port)
Fault Tolerance	Customized redundancy hardware	Application / middleware SW-level methods with timing, coverage and power advantages	Hardware / System SW-level methods with improved efficiency over application / middleware methods	Application / middleware SW-level methods with timing, coverage and power advantages
Extensibility	Generally not available	Cascade chiplets via SRIO	Cascade chiplets via SRIO transparently	Cascade chiplets via SRIO
Note: Working estimates from PDR; high resolution updates by CDR.				

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Technical Approach



- Following a competitive procurement, the HPSC contract was awarded to Boeing for the development of prototype Chiplets, system software, evaluation boards, and emulators.
- The Chiplet architecture leverages commercially available intellectual property (IP) cores.
- The Chiplet will be implemented with a Radiation Hardened By Design (RHBD) library that utilizes the commercially available Global Foundries 32nm silicon-on-insulator (SOI) fabrication process.
- Chiplet I/O provided by SRIO, SpaceWire, Time-Triggered Ethernet (TTE), and other low rate interfaces.
- Power scaling is provided with on chip “power islanding” where regions of the Chiplet can be powered down when not in use, and by clock gating.
- System software developed under contract will utilize commercially available and open source operating systems included Linux and RTEMS.
- Middleware will provide a software layer that provides services to the higher-level application software for configuration management, resource allocation, power/performance management, and fault tolerance capabilities of the HPSC chiplet
- A tiered fault tolerance approach will provided fault isolation, detection, and mitigation within the Chiplet hardware, system software, and middleware.

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Technical Status



- Major results for FY18 (**chiplet**)
 - HPSC Preliminary Design Review held on May 30-31, 2018
 - Derived requirements and flow down completed
 - Baseline architecture and theory of operation completed
 - Preliminary design capture and test bench development completed
 - Preliminary performance analysis completed
 - Continued System Engineering and detailed design effort in progress – collaborative effort between NASA and Boeing
- Major results for FY18 (**middleware**)
 - Held HPSC Middleware Systems Requirements Review (SRR) May, 2018
 - Kicked off Middleware Release 1 activities geared towards first release of middleware to occur during 1QFY19.
- Significant technical operational / design **concerns** resolved or in work
 - Key issues to be resolved during the detailed design phase
 - Fault Tolerance architecture and analysis – *in process*
 - Power analysis – *in process*
 - Radiation analysis – *in process*
 - Packaging Design – *in process*
 - These items are being worked actively by the Boeing team with weekly interactions with the NASA team.
 - NASA is providing guidance and expertise on requirements and use cases. Boeing is investigating options, approaches and impacts.
 - All items are tracked in the Systems Engineering action item spreadsheet.

HPSC – Programmatic Products vs. Enhancements Timeline

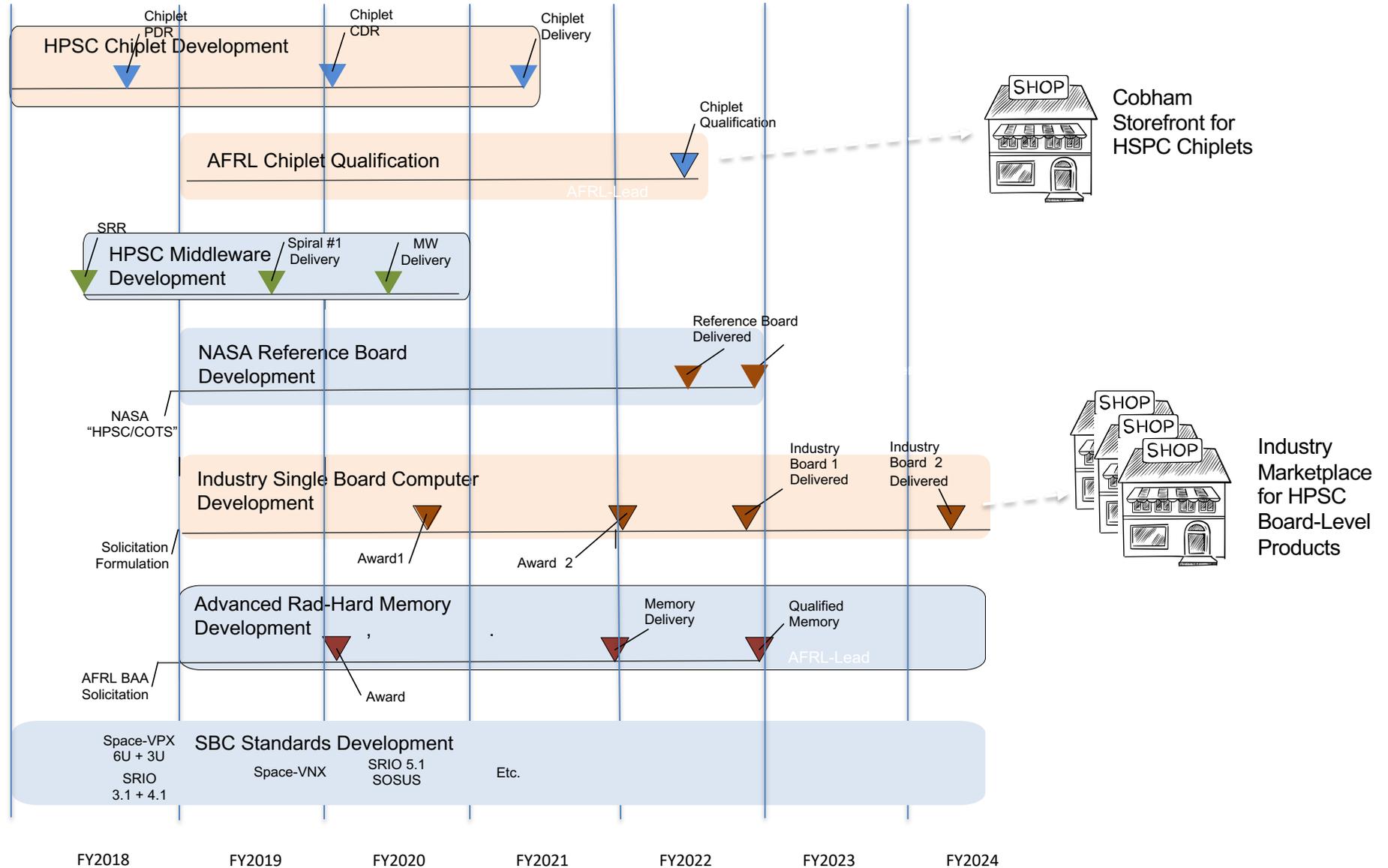


The central development path leading to HPSC flight-ready **products** proceeds through:

- Chiplet Development
- Chiplet Qualification
- SBC Development

Additional HPSC **enhancements** include:

- Middleware Development
- NASA Reference Board Development
- Advanced Rad-Hard Memory Development
- Standards Development



HPSC – Programmatic RFA Status

- The HPSC Preliminary Design Review (PDR) was held May 30-31, 2018
- A total of 48 total RFAs were received from the board (21 action, 27 advisory)
- At present, 19 RFAs (8 action, 11 advisory) are dispositioned for closure but are awaiting documentation
- Boeing has assessed that 6 RFAs have the potential for significant impact

19	Run HAPS to validate architecture prior to CDR	Potential bottlenecks for benchmarks may not be identified prior to final design.	<u>Consider::</u> Running benchmarks on the HAPS systems to validate architecture prior to final critical design phase.	Advisory
20	IBIS model characterization	No IBIS model characterization performed of HPSC after the test campaign is complete.	<u>Consider::</u> Perform an IBIS model characterization of HPSC after the test campaign is complete. This will aid users to assess signal integrity of the systems using the HPSC.	Advisory
23	32 nm Qualification	32 nm technology reliability rated low risk. Not clear if assessment is based upon a thorough understanding of foundry rel. data. If qualification is addressed, towards the end of the program, the solution space where qualification issues that may arrive is constrained.	<u>Consider::</u> Initiating a reevaluation of reliability of the 32 nm RHDB process including the accumulation of foundry reliability data for each failure mechanism. Where required reliability cannot be demonstrated, consider an experimental program be designed to demonstrate reliability.	Advisory
26	Dose Rate Upset	While good dose rate upset results have been obtained on the pathfinder chip, the pathfinder chip is small & DRU effects are very non-linear on chip size. The photocurrents are larger & the layout effects are enhanced. Proper design to avoid rail span collapse is currently based on intuition & pathfinder results, not analysis. This could lead to risk in meeting the DRU requirement.	<u>Consider::</u> A detailed analysis on rail span collapse for the chiplet be performed to determine if the proposed design meets the target requirement. If not, design can be modified & reanalyzed.	Advisory
29	Review & update security requirements	HPSC team has not received clear guidance regarding security requirements.	<u>Recommendation::</u> NASA and USAF provide HPSC team with updated security requirements and verify that no additional HPSC hooks are required to support an external security chip.	Action
34	GPIO Availability	The number of GPIOs available seems low given the number and use cases for GPIO.	<u>Consider::</u> Review the GPIO quantity and figure out impact of sizing these counts to match current usage levels for GPIO signals	Advisory

HPSC – Programmatic *USAF Qualification Planning*



- USAF/SMC is initiating the qualification program for the HPSC Chiplet
- The Chiplet Qualification effort will require a non-standard qualification due to advanced nature of HPSC technology
- An early start is needed to define the program, allowing a rapid transition of HPSC technology to production and infusion
- D. Alexander / COSMIAC (UNM) will lead the USAF qualification planning effort
- NASA is engaging SME consultants at GSFC and JPL

HPSC – Programmatic *USAF Security Chiplet*



Context

- NASA / USAF made an architectural decision to host protection/security functions in a separate chiplet
- Allows security / protection functionality to evolve independently

Next Steps

- Following discussion at AFRL on August 21, USAF is standing up an Architecture Study team to define the Security Chiplet

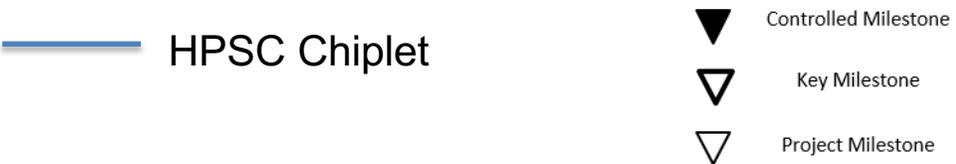
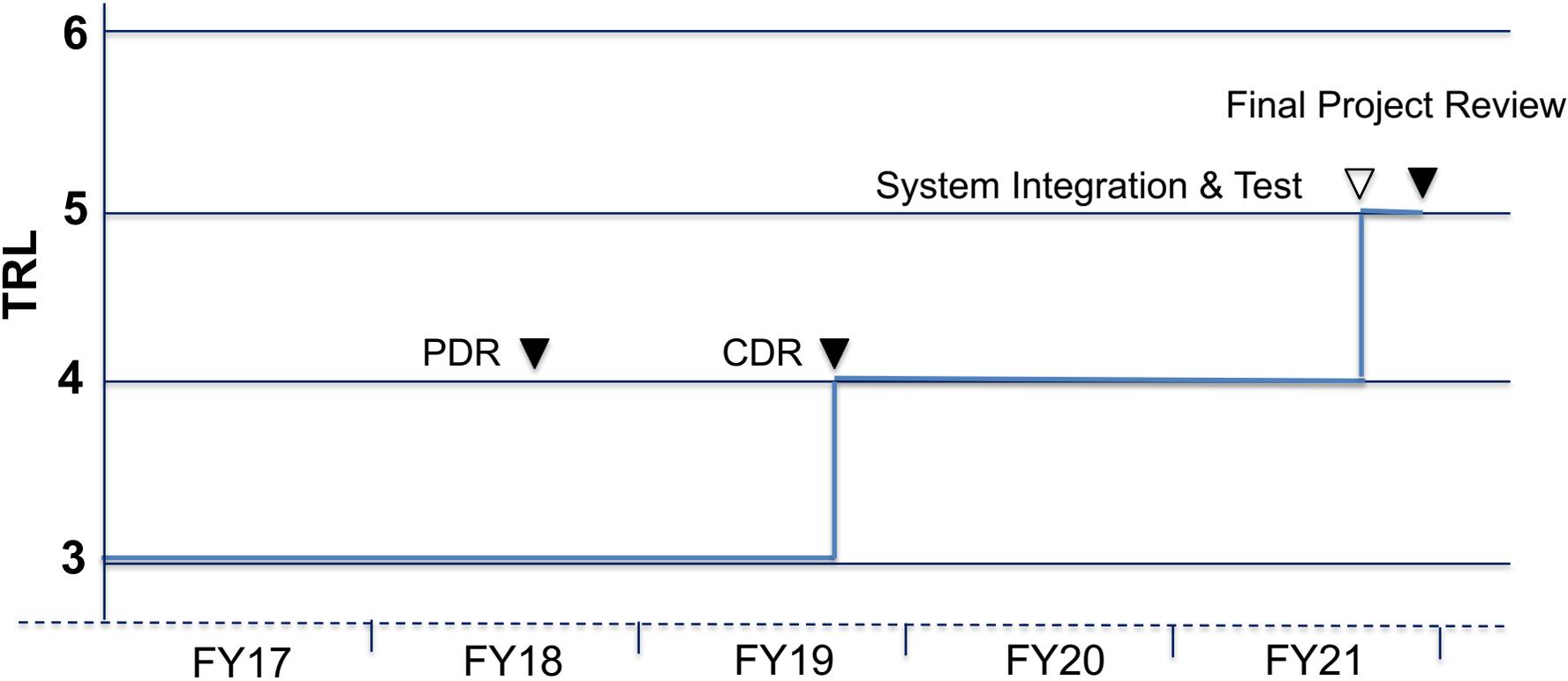
Scope of Architecture Study

- Function allocation HPSC vs. Security Chiplet
 - Confirm native HPSC security features
- ARM Trust Zone implementation
- Secure communication between chiplets
- Flight system functionality for key management, layered authentication, intrusion detection and response, etc.



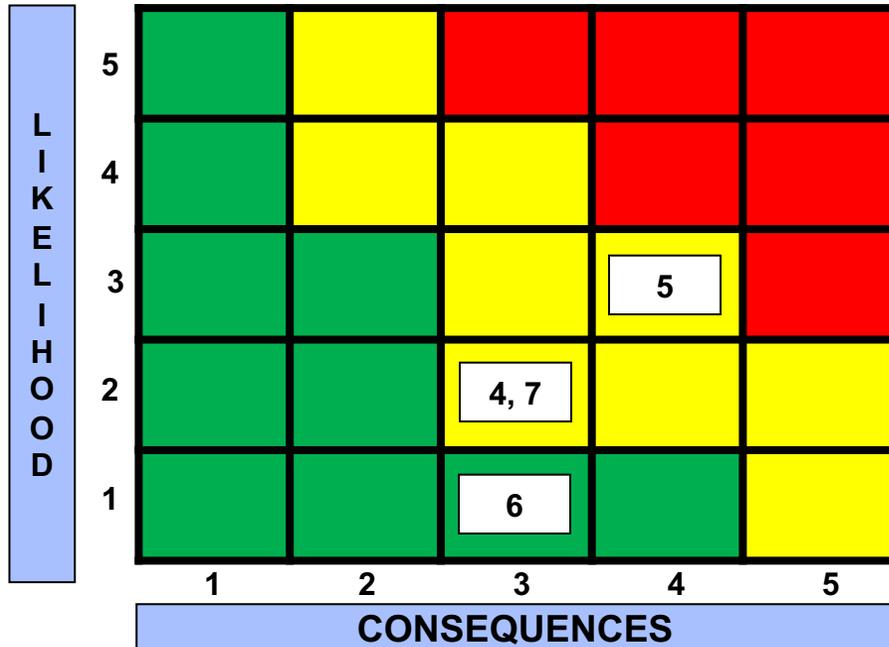
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IMS / TRL Alignment





HPSC Risk Summary



Criticality	L x C Trend	Approach
High	Decreasing (Improving)	M - Mitigate
Med	Increasing (Worsening)	W - Watch
Low	Unchanged	A - Accept
	New Since Last Period	R - Research

Affinity: T-Technical C-Cost Sc-Schedule Sa-Safety

Risk ID	Affinity	Description/Status	Trend
ID# 4	C, S	Licensing for Tech Demo	<input type="checkbox"/>
ID# 5	T, C, S, P	Second Spin	<input type="checkbox"/>
ID# 6	S	TAPO Sponsor	<input type="checkbox"/>
ID# 7	T, C, S, P	Security Chiplet	<input type="checkbox"/>

Risk #4: Given that HPSC Chiplet development involves licensing of IP, there is a possibility that the planned HPSC+SPLICE Tech Demo will be interpreted as production development rather than prototype development, resulting in separate and additional licensing costs.

Risk #5: Given that processor chip technology development often involves a second spin to address errata concerning technical or performance objectives not met, there is a possibility that the HPSC Chiplet development will require a second spin, resulting in product completion delays with associated programmatic impacts.

Risk #6: Given that USAF qualification activities require the identification of a DoD sponsor to the Trusted Applications Program Office (TAPO), and that such a USAF sponsor has not yet been identified, there is a possibility that HPSC Chiplet qualification is not fully enabled, resulting in delays.

Risk #7: Given that certain native security features are planned to be implemented in the HPSC Chiplet, to be architecturally available for a planned separate security chiplet, there is a possibility that the relevant requirements will exceed current or previously existing security-related requirements, resulting in increased scope for the HPSC Chiplet development effort.

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EPO Summary Chart



- HPSC was presented at several major conferences (DASIA 2017, SMC-IT 2017, GOMACTech 2018, Space Computing 2018 and RADECS 2018), via papers and invited talks by the NASA PM, DPM and TA, and the Boeing PI



- GCD prepared an HPSC video for general communications and outreach, working with the PM at JPL and the DPM at GSFC

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Annual Summary



- **System Requirements Review completed on February 22, 2018**
 - Over 500 derived requirements have been vetted, flowed and tracked
- **Middleware System Requirements Review completed on May 2, 2018**
 - NASA Middleware and USC-ISI System Software are closely coordinating
- **Preliminary Design Review completed on May 31, 2018**
 - Independent Review Team issued board report in July, including 48 RFAs
- **A strategic planning meeting was held at AFRL on August 21, 2018**
 - Outcomes include qualification planning start and security chiplet study
- **An SBC co-investment is poised for an FY19 new start**
 - NASA reference board and industry-developed single board computers



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Annual Assessment Summary



Technology	Mid Year				Annual Performance				Comments
	C	S	T	P	C	S	T	P	
HPSC	Yellow	Yellow	Green	Green	Green	Yellow	Green	Yellow	<p>Cost – Boeing contract and NASA efforts are adequately forward-funded into FY19.</p> <p>Schedule – Detailed, trackable development schedule is in development, separate from EVM artifacts. As can be assessed, effort is on track heading to CDR.</p> <p>Technical – Detailed design considerations are worked in bi-weekly system engineering deep dives.</p> <p>Programmatic – SBC development as an FY19 new start is in work. The schedule for an HPSC+SPLICE Tech Demo on a lunar lander is success-oriented. Partnering with USAF is excellent – SMC qualification planning and AFRL security chiplet study have been initiated.</p>
Advanced Memory	Green	Green	Green	Yellow	Green	Green	Green	Yellow	<p>Technical – Study is complete and published.</p> <p>Cost – USAF and USN partners are funding to a total of \$48M, sufficient for two complete memory technology developments. NASA is a junior partner at \$6M.</p> <p>Schedule – AFRL has prepared a BAA for issuance in early FY19.</p> <p>Programmatic – Economy Act likely applies and an IAA will be developed. Working with AFRL to define possible options which can be funded by NASA. Final details will wait on actual awards.</p>

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EPO Summary Chart



➤ Conferences attended

Conference	Date	Paper Title	HPSC Speaker
RADECS 2018 (Gothenburg, SWEDEN)	Sept 2018	(Invited) Next Generation Processing for Space Systems	R. Some, JPL
Space Computing (Bedford, MA)	June 2018	HPSC Chiplet Program Overview	J. Ballast, Boeing
Space Computing (Bedford, MA)	June 2018	High-Performance Spaceflight Computing (HPSC) Program Overview	W. Powell, GSFC
GOMACTech (Miami, FL)	March 2018	HPSC Chiplet Program Overview	J. Ballast, Boeing
SMC-IT 2017 (Madrid, SPAIN)	Sept 2017	(Invited) Data Science and Computing on the Path to Autonomy	R. Doyle, JPL

Licensing for Tech Demo – R. Some (TA)

Risk ID #4

Trend



Criticality



Current L/C

2x3

Affinity Group

, Cost, Schedule

Planned Closure

03/31/2019

Open Date

09/27/2018

Risk Statement :

Approach: (choose one) **Mitigate**, Watch, Accept, Research

Given that HPSC Chiplet development involves licensing of IP, there is a possibility that the planned HPSC+SPLICE Tech Demo will be interpreted as production development rather than prototype development, resulting in separate and additional licensing costs.

Context

HPSC Team reading of the relevant IP licensing agreements does not appear to preclude technology demonstration activities within the current licensing agreement. However, the question is not resolved.

Status

09/2018 – New this reporting period.

Mitigation Steps	Dollars to implement	Trigger/ Start date	Schedule UID	Completion Date	Resulting L/C
Resolve the interpretation of the IP licensing agreements with Boeing assistance.	\$25K	09/2018			
Engage NASA legal counsel as needed.	TBD	09/2018			

(Note: The Schedule UID is the unique id no of the mitigation step in your schedule if appropriate.

Dollars to implement are not extra approved \$ from the Program Office but \$ set aside as part of project budget to mitigate.)

HPSC



Second Spin – R. Doyle (PM)

Risk ID #5

Trend



Criticality

Med

Current L/C

3x4

Affinity Group

Technical, Cost,
Schedule, Performance

Planned Closure

07/28/2021

Open Date

09/27/2018

Risk Statement :

Approach: (choose one) Mitigate, **Watch**, Accept, Research

Given that processor chip technology development often involves a second spin to address errata concerning technical or performance objectives not met, there is a possibility that the HPSC Chiplet development will require a second spin, resulting in product completion delays with associated programmatic impacts.

Context

Second spins are not uncommon. The recent and relevant Maestro development effort required a second spin.

Status

09/2018 – New this reporting period.

Mitigation Steps	Dollars to implement	Trigger/ Start date	Schedule UID	Completion Date	Resulting L/C

(Note: The Schedule UID is the unique id no of the mitigation step in your schedule if appropriate.

Dollars to implement are not extra approved \$ from the Program Office but \$ set aside as part of project budget to mitigate.)

HPSC



TAPO Sponsor – K. Bole (AFRL)

Risk ID #6

Trend



Criticality



Current L/C

1x3

Affinity Group

, Schedule

Planned Closure

03/31/2019

Open Date

09/27/2018

Risk Statement :

Approach: (choose one) Mitigate, **Watch**, Accept, Research

Given that USAF qualification activities require the identification of a DoD sponsor to the Trusted Applications Program Office (TAPO), and that such a USAF sponsor has not yet been identified, there is a possibility that HPSC Chiplet qualification is not fully enabled, resulting in delays.

Context

SMC is the identified USAF program office for HPSC Chiplet qualification and AFRL is the identified USAF implementation organization. Qualification planning activities are underway.

Status

09/2018 – New this reporting period.

Mitigation Steps	Dollars to implement	Trigger/ Start date	Schedule UID	Completion Date	Resulting L/C
Resolve the interpretation of the IP licensing agreements with Boeing assistance.	\$25K	09/2018			
Engage NASA legal counsel as needed.	TBD	09/2018			

(Note: The Schedule UID is the unique id no of the mitigation step in your schedule if appropriate.

Dollars to implement are not extra approved \$ from the Program Office but \$ set aside as part of project budget to mitigate.)

HPSC



Security Chippet – R. Doyle (PM)

Risk ID #7

Trend



Criticality

Med

Current L/C

2x3

Affinity Group

, Technical, Cost, Schedule, Performance

Planned Closure

02/28/2019

Open Date

09/27/2018

Risk Statement :

Approach: (choose one) **Mitigate**, Watch, Accept, **Research**

Given that certain native security features are planned to be implemented in the HPSC Chippet, to be architecturally available for a planned separate security chippet, there is a possibility that the relevant requirements will exceed current or previously existing security-related requirements, resulting in increased scope for the HPSC Chippet development effort.

Context

NASA and USAF made a joint architectural decision to implement security/protection features in a separate security chippet. However, certain native security features are required within the HPSC Chippet to enable this secure flight computing system architecture concept.

Status

09/2018 – New this reporting period.

Mitigation Steps	Dollars to implement	Trigger/ Start date	Schedule UID	Completion Date	Resulting L/C
AFRL is leading an HPSC Cybersecurity Architecture Study with Boeing, NASA and USAF.	\$100K	08/2018			
The objective is to capture any increased scope for HPSC security features within previously existing HPSC Chippet security requirements.	TBD	08/2018			

(Note: The Schedule UID is the unique id no of the mitigation step in your schedule if appropriate.

Dollars to implement are not extra approved \$ from the Program Office but \$ set aside as part of project budget to mitigate.)

HPSC

Boeing Risk Cube



1	32nm SOI foundry process is not available
2	Government-provided cyber-security requirements are not defined early in the program
3	Planned number of cores, memory and I/O do not fit in space-qualifiable PBGA
4	Power efficiency of baseline design is less than expected
5	HPSC Chiplet does not close timing at target clock rate
6	Agreement on 3 rd party IP terms and conditions takes longer than expected - Closed
7	HPSC Chiplet is ITAR restricted - Closed
8	32nm SOI manufacturing process and RHBD design libraries do not provide required reliability
9	If the requirements converge too slowly, or if there are late additions to requirements or I/O subsystems, then
10	If there is a functional failure in the HPSC Chiplet with no workaround, then the Chiplet will need a second design pass.
11	If a multi-project wafer run is not timely, then must consider earlier or later delivery of the design

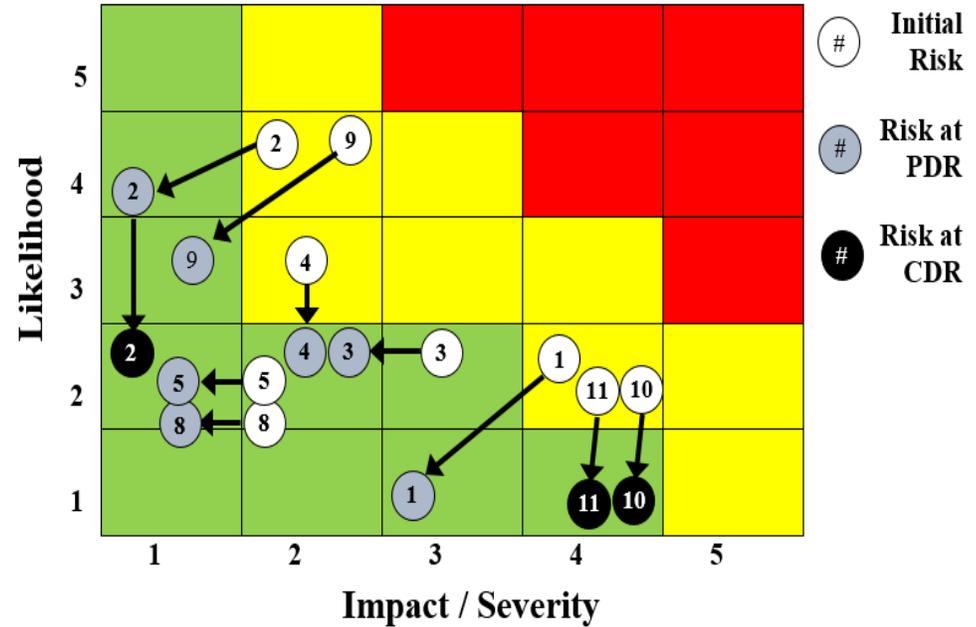
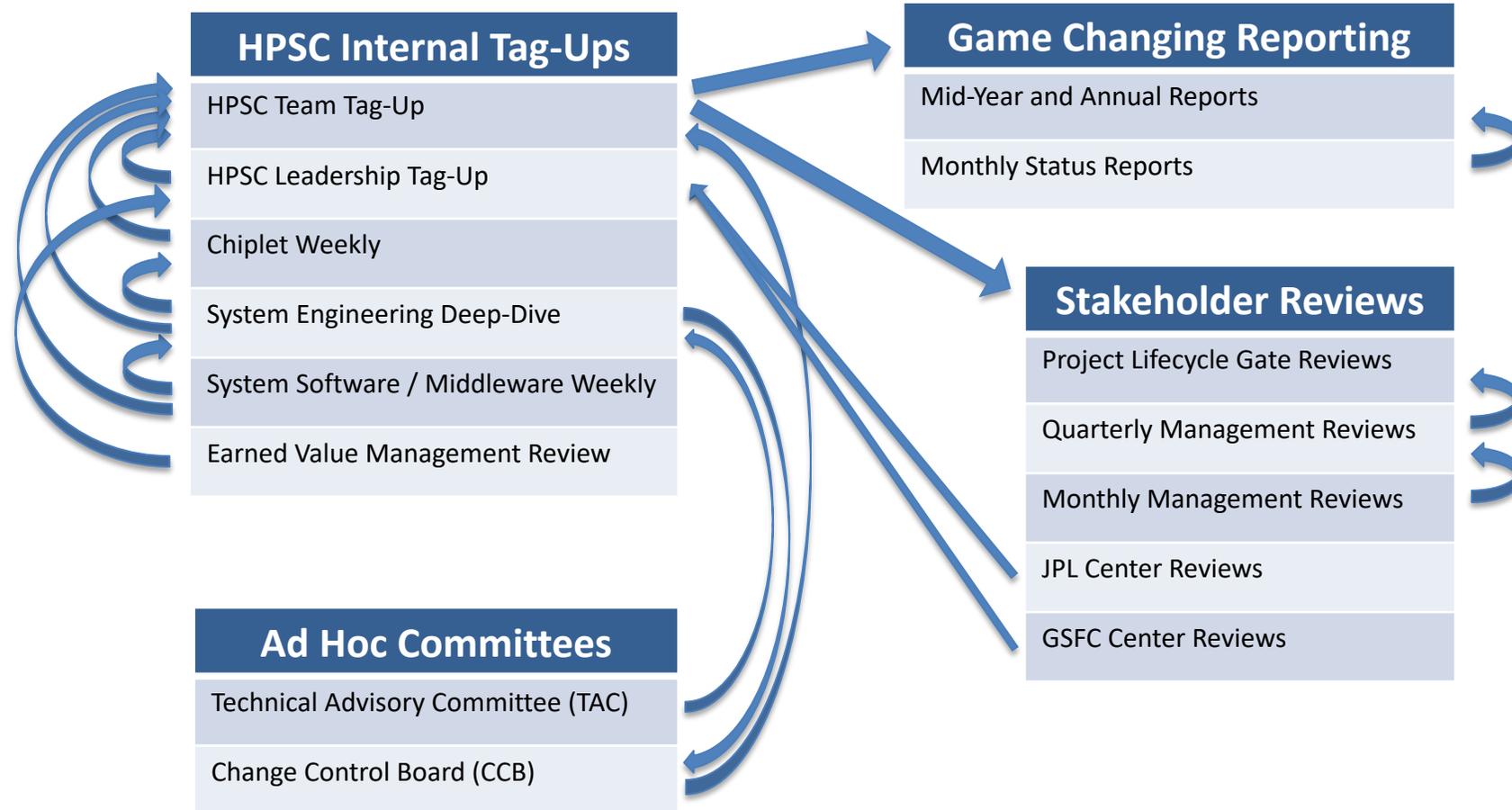


Figure 21: HPSC Risk Cube

= Retired or transferred

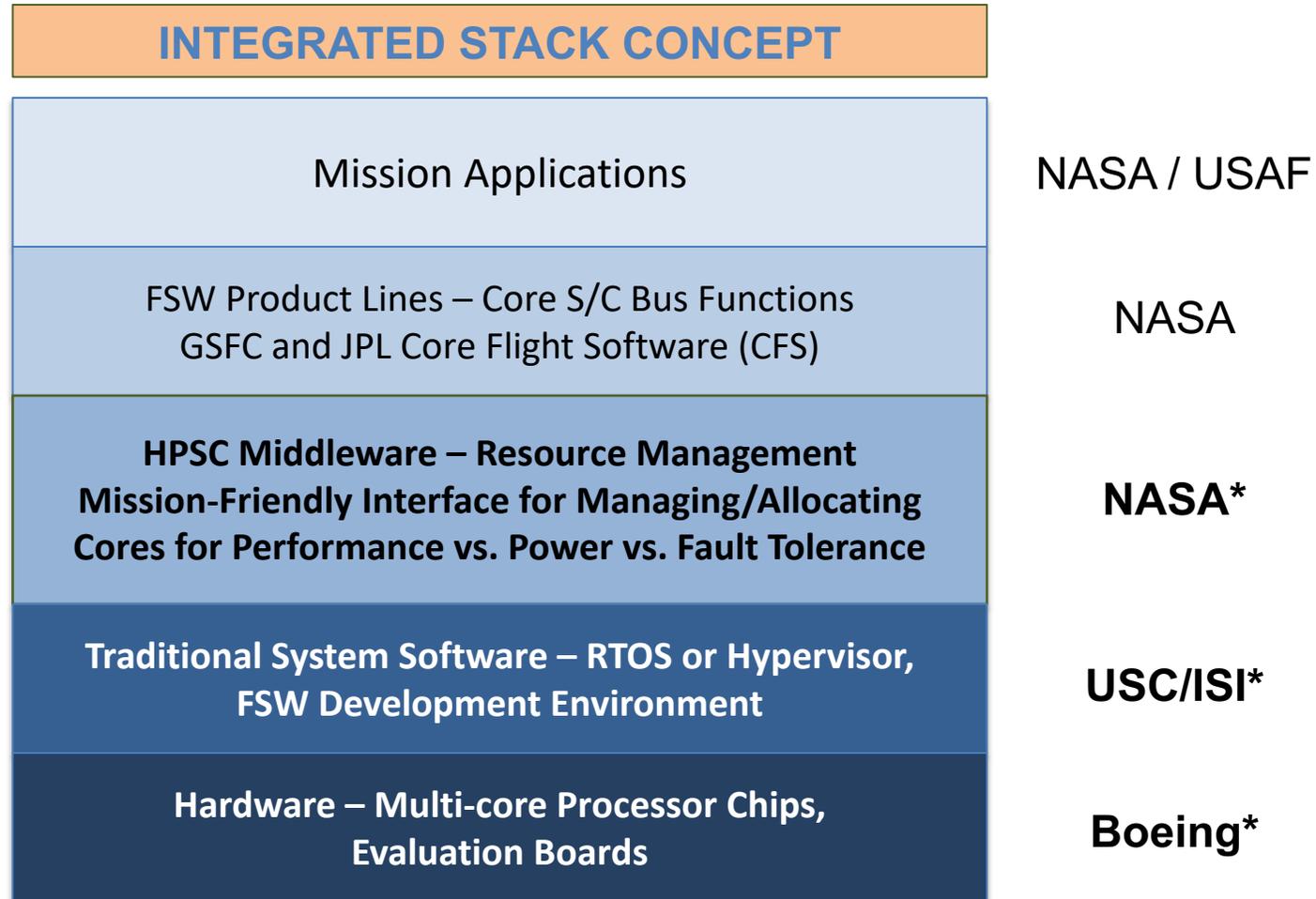
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Information Flow



HPSC

Integrated Stack



* Part of the HPSC Development

