High Performance Space Computing with System-on-Chip Instrument Avionics for Space-based Next Generation Imaging Spectrometers (NGIS).

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***Abstract*— The emergent technology of system-on-chip (SoC) devices promises lighter, smaller, cheaper, and more capable and reliable space electronic systems that could help to unveil some of the most treasured secrets in our universe. This technology is an improvement over the technology that is currently used in space applications, which lags behind state-of-the-art commercial-off-the-shelf (COTS) equipment by several generations. SoC technology integrates all computational power required by next-generation space exploration science instruments onto a single chip. This presentation will describe a Xilinx Zynq-based data acquisition, cloud-screening and compression computing system that has been developed at the Jet Propulsion Laboratory (JPL) for JPL's Next Generation Imaging Spectrometers (NGIS). The Xilinx Zynq-based Alpha Data hardware assembly fits into a 120mm by 190m by 40mm assembly and uses 9 watts at peak performance. The computing element is a Xilinx Zynq Z7045Q which includes a Kintex-7 FPGA (equivalent to 3 RAD Virtex5 FPGAs in terms of logic cell resources) and dual-core ARM Cortex-A9 Processors (equivalent to 10 RAD750 Power PCs in term of processing capability).**

Keywords—data compression, system-on-chip, hyperspectral imagers

I. Introduction

Hyperspectral images are three-dimensional data sets, where two of the dimensions are spatial and the third is spectral (Figure 1). They can be regarded as a stack of individual images that represent the same spatial scene viewed in a distinct, narrow part of the electromagnetic spectrum. The Airborne Visible/Infrared Imaging Spectrometer-Next Generation (AVIRIS-NG [16]) instrument is an example of an instrument that can acquire such imagery. Hyperspectral imagery can also be acquired from spacecraft. Because one hyperspectral image can be comprised of hundreds of spectral bands, it can represent a large volume of data. Future spacecraft that acquire hyperspectral imagery [26] may have modest bandwidths available to transfer the data to the ground, and there is much interest in compressing the data efficiently [1][2][3].

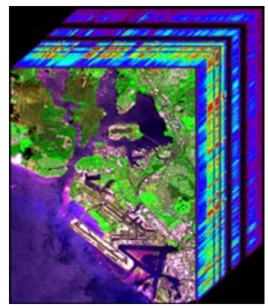

Figure 1. An example of a hyperspectral data cube: Pearl Harbor, Hawaii, taken by the AVIRIS instrument

II. System-on-Chip

The JPL-developed "Fast Lossless Extended" (FLEX) hyperspectral compressor [23] is a low complexity compression technique. The compression effectiveness is derived from an adaptive filtering method. The technique is currently implemented on both software and hardware platforms for various space applications. In particular, the algorithm has been programmed on a Field Programmable Gate Array (FPGA), which is a hardware platform that can be used in space for data processing. The FPGA implementation is capable of compressing data in real-time as it is acquired.

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Hybrid System-on-Chip (SoC) devices that embed one of the world's most energy efficient processors (ARM Cortex-A9 [8]) and the latest and most powerful FPGA architecture (Xilinx 7-series [9]) into a single chip (Xilinx Zynq [10]) promise new opportunities due to the performance, power consumption, weight and volume benefits they bring. Currently, programmable logic and processors are usually combined in most spacecraft subsystems as separate components distributed along one or several circuit boards [11][12]. NASA and other space agencies are considering SoC technology for its high computation capabilities and power efficiency, hoping to pave the way for future space exploration missions that are becoming so performance-demanding that currently available space-grade technology (e.g., RAD750 [13]) cannot meet their needs [24]. Despite the fact that currently there are no space-qualified SoC parts, NASA is testing commercial Xilinx Zynq SoC devices in the International Space Station (ISS) as well as in precursor CubeSats operating in Low Earth Orbit (LEO), where the exposure to radiation is limited [19][20][21][28].

The SoC instrument avionics perform data acquisition, cloud-screening and compression computing system for hyperspectral imagers. They are implemented on the Xilinx Zynq-based custom Alpha Data hardware assembly which fits into a 120mm by 190m by 40mm assembly and uses 9 watts at peak performance (Figure 2) [25]. The computing element is a Xilinx Zynq Z7045Q which includes a Kintex-7 FPGA and dual-core ARM Cortex-A9 Processors.

The SoC instrument avionics have been integrated with a particular NGIS-based implementation. Hyperspectral images are acquired, screened for atmospheric clouds [27], and compressed (either losslessly or lossily) in real-time using JPL's "Fast Lossless Extended" (FLEX) compressor [22], implemented into the Programmable Logic (PL) of the Zynq SoC device, and sent to on-line HW/SW verification tools either through Camera Link (LiveView [4]) or LVDS protocol (cl3_console). In addition the PL interfaces with the focus step motor, 32 temperature sensors, 12 heaters and an IMU/GPS device providing inertial/position information and time synchronization with GPS or UTC time. The processing system (PS) of the Zynq SoC implements Command and Data Handling to program the Hyperspectral Camera (frame rate, exposure time), acquires telemetry (temperature, pulse-per-seconds counts, frames count), control heaters, focus motor and data flow inside the PL. The PS interfaces with the Real-Time Cmd&Tlm (p2serialcmds) performing on-line HW/SW verification

III. Compression Core

The FLEX data compression algorithm exploits dependencies in all three dimensions of hyperspectral data sets, which produces substantially more effective compression than two-dimensional approaches such as applying conventional image compression to each spectral band independently. FLEX is a predictive technique that uses an adaptive filtering method to achieve a state-of-the-art combination of low complexity and compression effectiveness. The lossless part of FLEX has been adapted as

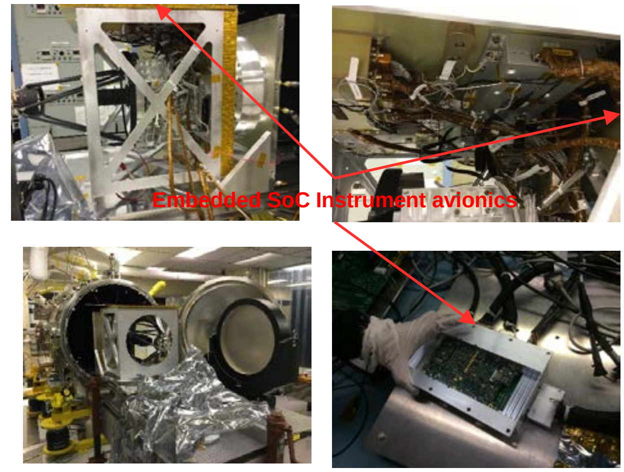

Figure 2. SoC instrument avionics integrated with a particular Space-based Next Generation Imaging Spectrometers (NGIS) implementation.

the standard for Lossless Multispectral & Hyperspectral Image Compression by the Consultative Committee for Space Data Systems (CCSDS) [23] and the lossy component is the basis for the emerging Consultative Committee for Space Data Systems standard for low-complexity lossless and lossy multispectral and hyperspectral image compression. The low computational complexity of FLEX is well-suited for implementation in hardware. Software implementations may not meet the speed and real-time requirements of some space applications. Three FLEX IP cores have been integrated into the SoC Programmable Logic to provide a compression data rate of 70 frames/sec.

IV. Hardware/Firmware/Software Architecture

Figure 3 shows the SoC Architecture. Starting at the bottom we have the hardware components: customized COTS Alpha Data SoC board with a Zynq chip and external memory and custom carrier that connects the SoC board to the camera, the motor, the heaters, the compressed data and the Cmd&Tlm. One layer up we have the SoC FPGA fabric and custom logic. The interface to the hardware is abstracted using a C++ object based abstraction layer. This provides function for configuring the FPGA, reading and writing to the FPGA fabric, and handling interrupts. In addition is also provides OS independent objects for threading, and a few other useful normally platform dependent tools. The abstraction work is already done in the Alpha Data framework, and allows to migrate to other hardware platform and systems very easily such as change to different OS, run on different types of FPGA cards, and on different form factors of system, such as something VPX or PCIe based. Right at the top of the stack we have the NGIS application which provides some functionalities. First it lets the user control programming the camera, Data Flow Control inside the SoC FPGA fabric, heaters, the motor, the focal plane interface electronics.

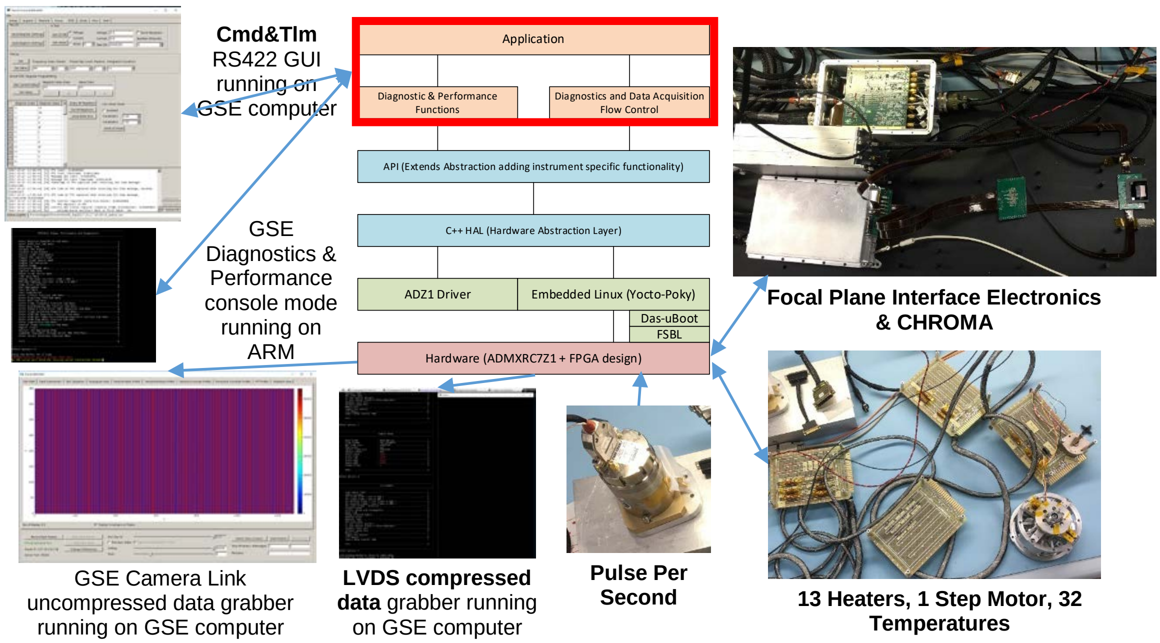

Figure 3. Hardware/Firmware/Software Architecture of SoC instrument avionics

In addition it has some diagnostic routines, such as checking the memory banks in the FPGA design are working. In addition to interacting with the NGIS API that application also has other jobs; communicating data, control and status with the flight computer, handling space craft inputs, and storing data to the local file system during GSE testing. Because the ARM in the Zynq is a dual core processor (and interaction with the FPGA is interrupt driving when it's waiting for the FPGA to complete a task), there is plenty of CPU time to do some data processing, that could be used to better tune the instrument. To mitigate for single event upset radiation effects on LEO orbit, parts on the customized COTS SoC have been screened for destructive latch-up, and unused functionalities have been eliminated (Ethernet, USB and ucontroller). In addition the customized COTS board has been populated with rad hard parts such as rad-hard oscillator and rad-had watchdog timer/hardware reset where no COTS part could meet the destructive latch-up radiation requirements.

V. Hardware/Software Co-verification tools

The complexity of hardware, software and HW/SW integration that arises from the convergence of so much functionality in such small hybrid SoC devices has driven both hardware and software innovation at almost break-neck speed, while the development methodology that brings hardware and software together lags behind. Sequential development, with software development waiting for available hardware, is still the prevailing norm. But sequential development often fails to deliver quality products within the short windows that rule the faster, cheaper and robust space missions today [7]. A more robust systems engineering approach is to have both HW/SW co-developed and genetically linked. To help in the parallel agile development of hardware and software for SoC technology [14], hardware/software co-verification tools have been developed for the hyperspectral imagers (Figure 4). These tools make sure that embedded system software works correctly with the hardware, and that the hardware has been properly designed to run the software successfully before deploying the image spectrometers in expensive space or airborne missions [5]. One of the co-verification tool is LiveView [4]. It was initially designed for real-time calibration of focal plane arrays. It is performing real-time analysis of images acquired through the Camera Link interface of the hyperspectral camera. This calibration analysis is used to identify sources of electronic noise and interference in the imaging spectrometer and to characterize the FPA [15]. In the co-verification process, it is detecting errors in the firmware or software implementations.

Two techniques of hardware/software co-verification for instrument avionics for hyperspectral spectral imagers have been developed: on-line and off-line. The on-line verification tool controls the instrument to perform all the required functionalities and recognizes and handles unexpected behavior. It is used as ground support equipment (GSE) connected to the spectrometer and its avionics. The off-line verification tool is parsing the data acquired by the spectrometer. Its goal is to guarantee that the raw data are consistent to be processed for calibration and analysis data processing

VI. Conclusion

We developed a high performance data acquisition and data compression SW/FW/HW targeting SoC boards based on modified COTS devices for space deployment. The single core FLEX data compression targeting Virtex5 FPGA has been integrated into the ECOsystem Spaceborne Thermal Radiometer Experiment on Space Station (ECOSTRESS)

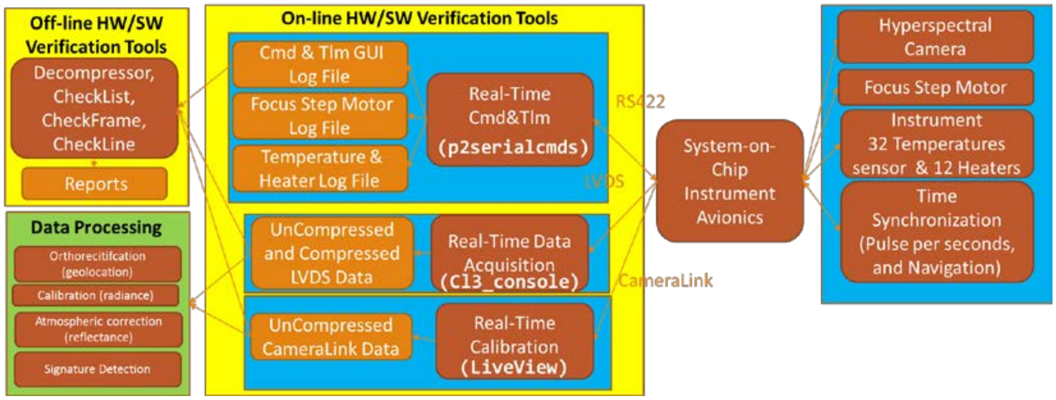

Figure 4. System-on-Chip instrument avionics architecture for hyperspectral imagers

mission (launchd in June 2018). The SoC instrument avionics will be used for the Earth Surface Mineral Dust Source Investigation on Space Station (EMIT) mission (launch 2020). Future technology developments will explore Multiple Processor System-on-the-Chip (MPSoC) and space qualified XQR Kintex UltraScale FPGA (XQRKU060) embedded with CHROMA-D which will able to provide hardware resource needed for real-time radiance, reflectance and data analysis.

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