Japan Aerospace Exploration Agency (JAXA)
The 30th Microelectronic Workshop (MEWS30)
October 18-19, 2017

National Aeronautics and
Space Administration

NASA's View on Space Electronics for the Next Decade

Shri G. Agarwal

NASA – Jet Propulsion Laboratory, California Institute of Technology

Shri.g.agarwal@nasa.gov
818-354-5598

JPL NEPAG Program Manager

Michael J. Sampson

NASA – Goddard Space Flight Center

michael.j.sampson@nasa.gov
301-614-6233

NEPP Program Manager

http://nepp.nasa.gov

Cassini Makes its "Goodbye Kiss" Flyby of Titan
Cassini made its final, distant flyby of Saturn's moon Titan on Sept. 11, which set the spacecraft on its final dive toward the planet.

Credits: NASA/JPL-Caltech

Copyright 2017. All rights reserved..

- **Thank you Suzuki-san for your invitation. It's always a great pleasure to visit Tsukuba.**
- **Congratulations on the 30th anniversary of the MEWS Workshop! It's a significant milestone for MEWS and JAXA!**
- **JAXA is our valued partner in NASA Electronic Parts Assurance Group (NEPAG) activities.**

Introduction

- This talk is about space electronics for the next decade.
- Perhaps we should first look at the last decade and take an inventory of some of the accomplishments of NEPAG and the space community in recent years.
- Advanced technologies provide lower power needs, higher performance, more functionality, and smaller packages.
- But, there are many challenges, including tighter budgets, constrained workforce, and shorter schedules.
- NASA supports a very wide spectrum of space missions/programs ranging from smallsats/cubesats to flagship missions such as the planned Europa mission. The success of each mission is important.
- As part of NEPAG, we work with manufacturers and the space parts user community to develop/evaluate new space products.
- The following pages will discuss some of the issues and related activities.

Partnering

JEDEC JC-13
(Manufacturers)

JC-13	Solid State Devices for Government Products
JC-13.1	Discrete Semiconductors for Government Products
JC-13.2	Microelectronics for Government Products
JC-13.4	Radiation Hardness
JC-13.5	Hybrids and Multi-chip Modules for Government Products
JC-13.7	New Electronic Device Insertion for Government Products

Joint meeting held
3 times a year

SSTC G-11/G-12
(Industry Users, Primes, Subs)

SAE SSTC G-11	Users of Passive Components
SAE SSTC G-12	Users of Solid State Devices
	G-12 Management:
	Chair – A. Touw
	Vice Chair – S. Agarwal
SAE SSTC G-11 & G-12	Space Subcommittee Chair – S. Agarwal

NASA Centers:

ARC	JSC
GRC	KSC
GSFC	LaRC
JPL	MSFC

Weekly Telecons
(Domestic)

Monthly Telecons
(International)

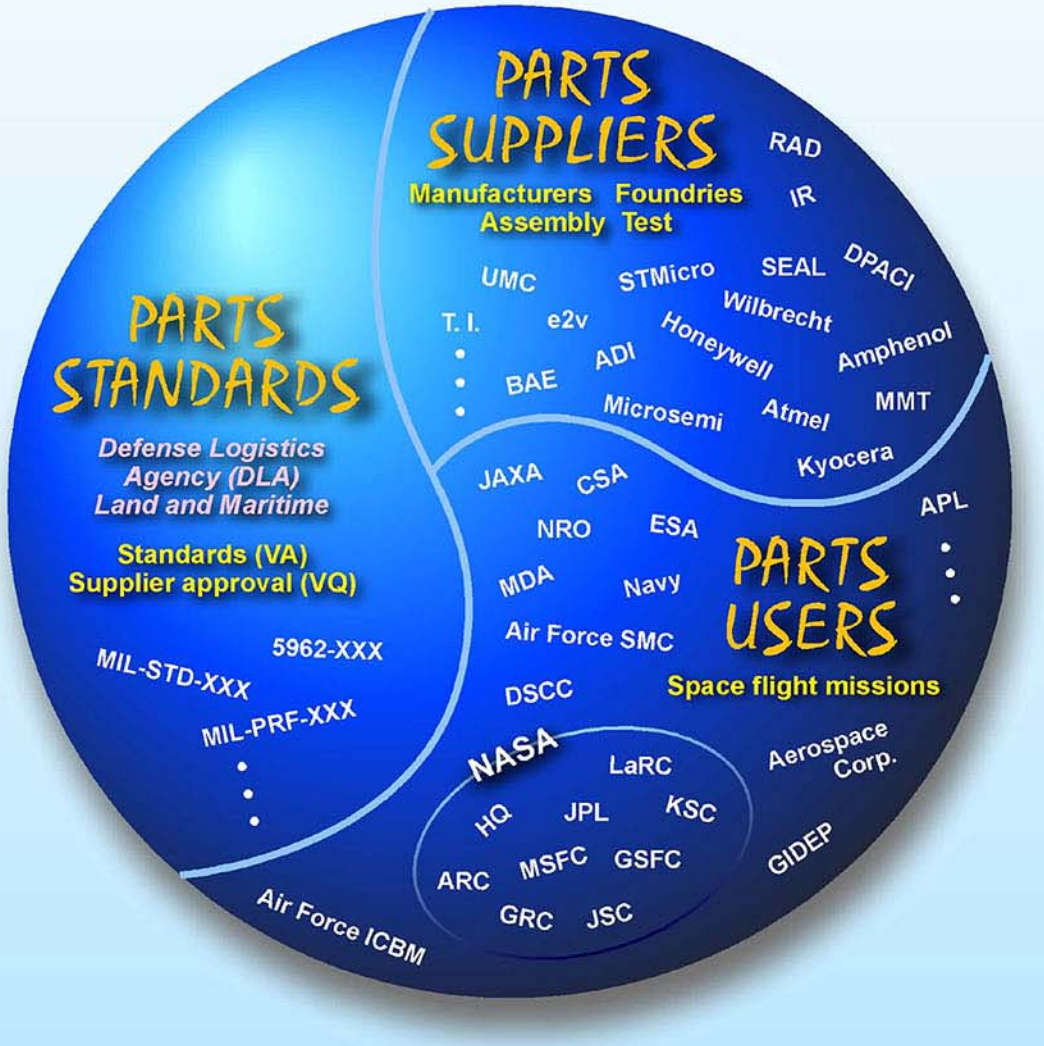
Partners from Outside NASA:

Domestic
- JHU/APL, Others
- The Aerospace Corp,
- U.S. Air Force, U.S. Navy,
- U.S. Army, DLA,

International
- ESA, JAXA, CSA

Space Parts World

NEPAG helps to Develop/Maintain Standards for Electronic Parts



The parts users and standards organizations work with suppliers to ensure availability of standard parts for NASA, DoD, and others. ***For Space microcircuits, DLA, NASA/JPL (S. Agarwal*) and the U.S. Air Force / Aerospace Corp. (L. Harzstark) form the Qualifying Activity (QA).***

**Also Systems, Standards and Technology Council (SSTC) G-12 Vice-Chair.*

NASA and JC-13

- **NASA is an active participant in many JC-13 activities.**
- **Some of the JC-13 Task Groups were started at NASA's request.**
  - **Example: Electronic Parameters and Burn-in Standardization.**
- **The newly started New Technology initiative (JC-13.7) provides an opportunity to look ahead:**
  - **Identify new technologies**
  - **Develop a path for their infusion into military and space.**

An artistic rendering of the OSIRIS-REx spacecraft over the asteroid Bennu (NASA)

In 2010, JAXA's Hayabusa (MUSES-C) completed the first sample return from the near-Earth asteroid 25143 Itokawa. Now, NASA's Origins, Spectral Interpretation, Resource Identification, Security-Regolith Explorer (OSIRIS-REx) spacecraft is on course to study and return a sample from the asteroid Bennu, a very different carbonaceous asteroid.

NASA and SAE SSTC G-12*

- NASA is an active participant in many G-12 activities.
- When requested, NASA has led the G-12 Task Groups.
  - Example: Infusion of new technology into DoD standards, the Class Y initiative.
- With the appointment of Shri Agarwal as the Vice-Chair of G-12, NASA is helping run the organization.
- Just recently, NASA was asked to take over the G-12 Space subcommittee as its Chair. In addition to the regular presentations from international agencies, two invited talks were given on electrostatic discharge (ESD) and the state of crystal oscillators
- * SAE = Society of Automotive Engineers
  SSTC = Systems, Standards and Technology Council
  G-12 = Solid State Devices

JEDEC/G-11/G-12 Schedule (Sept. 2017)

Columbus, OH — NEPAG MTG. — FINAL Meeting Schedule — September 2017

Day	Room	7:30 AM	8:00 AM	9:00 AM	10:00 AM	11:00 AM	12:00 PM	1:00 PM	2:00 PM	3:00 PM	4:00 PM	5:00 PM	6 PM	7PM
Mon 9/11	Hayes C							JC-13 TM1014 Leak Rate Definitions	G-12 Derating	JC-13.7 >2D packaging	G-12 PEM TG Qual and Screening Flow	G-12 Plastics / PEMS Subcommittee	G-12 Terrestrial & Avionics Subcommittee	
	Hayes D								JC-13.1 Technical 750 Test Method Review		JC-13.1 should attend PEMs Screening flow	MIL-PRF-19500R		
	Hayes E						JC-13 ExCo Mtg. *		JC-13.5 TG158 - Element Evaluation		JC-13 TG 17-01 TM 2020 PIND			
Day		7:30 AM	8:00 AM	9:00 AM	10:00 AM	11:00 AM	12:00 PM	1:00 PM	2:00 PM	3:00 PM	4:00 PM	5:00 PM	6 PM	7PM
Tues 9/12	Hayes C	New Member Orientation	JC-13.1 GaN Working Group (8 to 10:30)			JC-13.1/JC-13.7/G-12 SiC Tech Insertion (10:30 - 12)		JC-13/G-12 Joint Meeting	JC-13.1/JC-13.7/G-12 New Technology Appendix in 19500	JC-13.7 Copper Wire Bonds	JC-13.2 Elec Parameters & B/I Stand.	JC-13 TG 17-03 ESD *	G-12 & G-11 Counterfeit Mitigation Subcommittee	
	Hayes B		JC-13 TG 17-02 MIL-STD-883 Inspection and Criteria (Note >50 people attended)		JC-13.2 JEP121	JC-13.5 TG 175 - PL / QML			JC-13.5 TG 172 QML Req		JC-13.1 MIL-PRF-19500 Appendix J Non-Hermetic			
	Hayes E		JC-13.4 should attend GaN		ASTM				JC-13.4 Subcommittee Meeting					
Day		7:30 AM	8:00 AM	9:00 AM	10:00 AM	11:00 AM	12:00 PM	1:00 PM	2:00 PM	3:00 PM	4:00 PM	5:00 PM	6PM	7PM
Wed 9/13	Hayes C		Joint G-12 & G-11	Joint JC-13.2/G-12 Meeting (9 to 10:30)		Joint JC-13.1/G-12 Meeting (10:30 to 12)		JC-13 TG 15-02 X-Ray Seal Voids	Joint JC-13.5/G-12 Meeting	Joint JC-13.7/G-12 New Electronic Device (Only 2 hours if have speaker)		G-12 & G-11 Space Subcommittee		
	Hayes D		JC-13.5 Meeting							JC-13.5 Meeting		Chaired by NASA		
	Hayes B		G-12 Radiation RHA Subcommittee					Joint JC-13.1/JC-13.4/G-12 Advanced Radiation Topics Meeting						
	Hayes E		G-11 should go to joint G-12	G-11 Committee Meeting				G-11 Commmittee Meeting						
Day	Room	7:30 AM	8:00 AM	9:00 AM	10:00 AM	11:00 AM	12:00 PM	1:00 PM	2:00 PM	3:00 PM	4:00 PM	5:00 PM	6PM	7PM
Thurs 9/14	Hayes C		JC-13 General Session		Tech Talk: Radiation Effect Considerations for Electronics Used in Space Application (Reed Lawrence)	JC-13 ExCo Meeting (by invitation) *								
	Hayes D		G-11 Committee Meeting											

* Attended by NASA; NASA is G-12 Vice Chair.

New Technology Evaluation
A Multi-pronged Effort

- **New Technology Evaluations**
  - **There are NEPP (NASA Electronic Parts and Packaging) funded evaluations**
  - **NEPP also joins hands with other organizations. For example,**
    - **Working with the Navy Crane**
    - **Forming groups to understand advanced devices**
      - **Hold periodic telecons**
- **The JC-13 Effort**
  - **A few years back, JC-13 created a new committee, JC-13.7**
    - **JC-13.7 charter is to look into next generation technologies**
      - **List of top candidates**
        - **SiC, GaN (jointly with JC-13.1)**
        - **Copper bonds (with G-12 COTS/PEMs)**
        - **2.5D and 3D microcircuits (with G-12)**
    - **What would it take to infuse new technologies into QML standards**
      - **Identify the gaps**
    - **The JC-13.7 meets three times a year (same time as other JC-13 and G-11/G-12)**
    - **It is supported by NASA, JAXA among others**

New Technology Evaluation
A Multi-pronged Effort (Cont.)

- Preparing to embrace advanced technologies
  - Continually Improving the Existing Infrastructure
    - The role of Microcircuits Qualifying Activity (QA)
    - QML Classes
      - Is the current set of Q, V, and Y sufficient to cover new devices?
    - Specs and Standards
      - Bring them current (more details later)
    - Some of the side issues
      - Handling/packaging/ESD (electrostatic discharge)
      - Burn-in of high speed devices
      - Usefulness of the Qualified Products List (QPL) program
        - QPLS (space grade) crystal oscillators Limited resources
        - Workforce
        - Budgets

New Technology - Some Major Activities

- **Technical support to the Defense Logistics Agency (DLA) audits of supply chain:**
  - **Wafer foundry**
  - **Wafer bumping**
  - **Assembly**
  - **Column attach**
  - **Proper shipping/handling/ESD precautions become important**
    - **Per unit costs approaching $100k**
    - **NASA ESD surveys**
      - **NASA *EEE Parts Bulletins***

- **Qualifying Activity (QA) Reviews/Approvals:**
  - **NASA is part of the QA**
  - **Manufacturers to perform qualification as required in MIL-PRF-38535.**
    - **For example, a 4000-hour life test**
  - **DLA and manufacturers to develop standard microcircuit drawing (SMD)**
    - **Update existing boiler plate to accommodate new features - example on next page**

Standards Today

- **Past Standards:**
  - **Were written to accommodate multiple sources.**
  - **Minimal flexibility was allowed.**

- **Current Standards:**
  - **Written to infuse new technology.**
    - **Addressing complexities at both die and package levels**
  - **Introduced PIDTP (Package Integrity Demonstration Test Plan) for Classes V and Y**
    - **Allowing manufacturers to build their products the best way they know how**
    - **(PIDTP discussed further on page 21)**

NASA's Involvement in Developing New Space Products

- With the Defense Logistics Agency (DLA) and the Aerospace Corporation, NASA participates in the review and approval of new space products:
  - Standard Microcircuit Drawings (SMDs)
  - Characterization and qualification data per Appendix H of MIL-PRF-38535 (for the monolithics)
- During fiscal year 2017, 16 microcircuit SMDs were approved for release. The mix of new product types included:
  - Class Y ASICs from Honeywell
  - Analog-to-digital converters from ADI
  - 8-bit and 20-bit switches from Cobham
  - DC/DC converters from VPT and International Rectifier
  - Operational amplifiers from Anaren
  - Regulators from Linear Technology and Anaren
  - Memories from Atmel
  - And others

Standard Microcircuit Drawings (SMDs)

- DLA-VA responsible organization
- Supposed to be a self contained document
- Table I. In particular delta parameters
- Table IIa. Electrical measurements
- Table IIb. Delta measurements
- More functional/operational details added in SMDs, as applicable
  - e.g., Power-supply sequencing
- Per manufacturers, there is a strong demand for space products

An Example of SMD Boiler Plate Update

TABLE IIA. Electrical test requirements.

Line Number	Test requirements	Subgroups (in accordance with MIL-PRF-38535, table III)	
		Device class Q	Device class V
1	Interim electrical parameters (see 4.2)	1,2,3,7,8A, 8B,9,10,11 1/	1,2,3,7,8A, 8B,9,10,11 1/
2	Static burn-in I and II (method 1015)	Not required	Required
3	Same as line 1	- - -	1, 7 Δ 1/ 2/
4	Dynamic burn-in (method 1015)	Required	Required
5	Same as line 1	1, 7 Δ 1/ 2/	1, 7 Δ 1/ 2/
6	Final electrical parameters	1,2,3,7,8A,8B,9, 10,11 1/	1,2,3,7,8A,8B,9, 10,11 1/
7	Group A test requirements 3/	1,2,3,4,7,8A,8B,9,10 ,11 4/	1,2,3,4,7,8A,8B,9, 10,11 4/
8	Group C end-point electrical parameters 3/	1,2,3,7,8A,8B, 9,10,11 Δ 2/	1,2,3,7,8A,8B, 9,10,11 Δ 2/
9	Group D end-point electrical parameters 5/	2,3,8A,8B	2,3,8A,8B
10	Group E end-point electrical parameters 3/	1,7,9	1,7,9
11	Column attach 6/	1,7,9	1,7,9

- **For Flip-chip column attach**
  - **Add room temperature electricals (subgroups 1, 7, 9) after column attach – step 11 above**

Electrical Characteristics

TABLE IA. Electrical performance characteristics.

Test	Symbol	Conditions $-55° \le T_C \le +125°C$ $1.7\ V \le V_{DD} \le 1.9\ V$ $1.4V \le V_{DDQ} \le V_{DD}$ Unless Otherwise Specified 1/ 2/ 3/	Group A Subgroups	Device Type	Limits		Units
					Min	Max	
Output HIGH Voltage 4/	V_{OH1}	I_{OH} = -0.1 mA, 50 ohm impedance	1, 2, 3	All	V_{DDQ} -0.20	V_{DDQ}	V
Output LOW Voltage 5/	V_{OL1}	I_{OL} = 0.1 mA, 50 ohm impedance	1, 2, 3	All	V_{SS}	0.20	V
Output HIGH Voltage	V_{OH2}	I_{OH} = -2.0 mA, 50 ohm impedance	1, 2, 3	All	$V_{DDQ}/2$ - 0.12	$V_{DDQ}/2$ + 0.12	V
Output LOW Voltage	V_{OL2}	I_{OL} = 2.0 mA, 50 ohm impedance	1, 2, 3	All	$V_{DDQ}/2$ - 0.12	$V_{DDQ}/2$ + 0.12	V
Input HIGH Voltage 6/	V_{IH}		1, 2, 3	All	V_{REF} +0.1	V_{DDQ} +0.3	V
Input LOW Voltage 6/	V_{IL}		1, 2, 3	All	-0.3	V_{REF} -0.1	V
Input Reference Voltage 6/ 7/	V_{REF}	Typical value = 0.75 V	1, 2, 3	All	0.68	0.95	V
Input Leakage Current	I_X	$GND \le V_I \le V_{DDQ}$	1, 2, 3	All	-20	20	uA
Output Leakage Current	I_{OZ}	$GND \le V_I \le V_{DDQ}$, output disabled	1, 2, 3	All	-20	20	uA

- **Encircled are the delta parameters**
- **The limits should be split into room-temperature limits and over-temperature limits**

New Technology Flip-chip Devices: Underfill Status Update

- **Use of Underfills**
  - **The use of underfill material enhances reliability of flip-chip packages.**
  - **MIL-PRF-38535K requires flip-chip devices to meet the underfill requirements specified in MIL-STD-883, Test Method 5011.**

- **Activities**
  - **NASA *EEE Parts Bulletin* on underfills.**
  - **Defense Logistics Agency (DLA) Engineering Practice (EP) study**
  - **Discussion in Underfill Task Group**

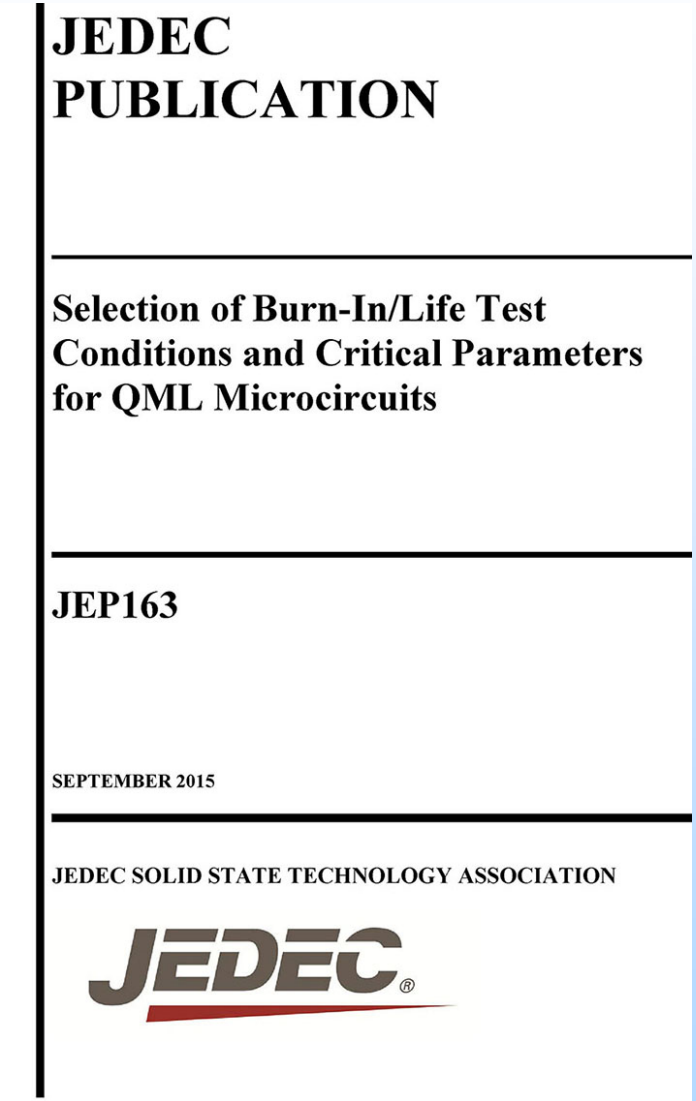
- **Status**
  - **The specification issue was resolved at the September 2016 meeting.**
  - **Task Group is now closed.**

Example of Updated Requirements, Microcircuits Burn-in (BI)

(NASA Inputs 12 September 2016)

- **Status**
  - Task Group chaired by N. Shindler
  - Published Guideline document JEP163.
  - Task Group is still open to address new concerns.

- **A New Concern**
  - DLA's Engineering Practice (EP) study on BI of high speed devices is in progress.
  - BI of high-speed devices (frequencies approaching gigahertz range)
    - What about hot spots on the die? For example, SERDES in an FPGA may run much hotter than the rest of the die.
      - Practically no data on hot spots (no verification of models)
    - Ambient vs. case vs. junction temperature



JEDEC PUBLICATION

Selection of Burn-In/Life Test Conditions and Critical Parameters for QML Microcircuits

JEP163

SEPTEMBER 2015

JEDEC SOLID STATE TECHNOLOGY ASSOCIATION

MIL-STD-883, Test Method 1005

MIL-STD-883J
w/CHANGE 1

TABLE I. Steady-state time temperature regression. 1/ 2/ 3/ 4/

Minimum temperature T_A (°C)	Minimum time (hours)			Test condition (see 3.5)
	Class level S	Class level B	Class level S hybrids (Class K)	
100		7500	7500	Hybrid only
105		4500	4500	"
110		3000	3000	"
115		2000	2000	"
120		1500	1500	"
125	1000	1000	1000	A -E
130	900	704	---	"
135	800	496	---	"
140	700	352	---	"
145	600	256	---	"
150	500	184	---	"
175		40	---	F
180		32	---	"
185		31	---	"
190		30	---	"

1/ Test condition F shall be authorized prior to use and consists of temperatures 175°C and higher.
2/ For condition F the maximum junction temperature is unlimited and care shall be taken to ensure the device(s) does not go into thermal runaway.
3/ The only allowed conditions are as stated above.
4/ Test temperatures below 125°C may be used for hybrid circuits only.

METHOD 1005.9
26 February 2010

- ***Life test below ambient temperature (T_A) = 125°C not allowed for monolithic microcircuits.***

What if A New Product Didn't Fit Any of the Existing Classifications? The "Class Y" Initiative

- Packaging and device technology advances are happening rapidly.
- How do we enable space flight projects to benefit from the newly developed devices?
- For Xilinx Virtex-4 and -5 FPGAs (which are ceramic-based flip-chip nonhermetic parts), a new class was needed.
- NASA led a G-12 initiative, called Class Y, for infusing Xilinx Virtex-4 and -5 FPGAs and other similar devices into military/space standards.
- Such an effort must be coordinated with the suppliers and users.
- Need to address all aspects of packaging configuration.
- New test methods must be created and the existing standards updated as necessary.

Infusion of New Technology into MIL/Space Standards PIDTP and Its Applicability

- **Issue**
  - How to address the manufacturability, test, quality, and reliability issues unique to new non-traditional assembly/package technologies intended for space applications
- **Solution implemented**
  - A new concept: package integrity demonstration test plan (PIDTP)
  - Each manufacturer shall develop a PIDTP to be approved by the qualifying activity after consultation with the space community.
- **The PIDTP requirement applies to:**
  - Non-hermetic packages
  - Flip-chip assembly
  - Solder terminations
  - (Refer to 38535, Appendix H)

Class Y SMD / Qualification / Certification Status

- **Class Y SMD (Standard Microcircuit Drawing)**
  - DLA generated first SMD draft for a QMLY ASIC
- **Qualified Manufacturers**
  - Honeywell, Plymouth, MN.
  - Cobham, Colorado Springs, CO (In Progress)
- **Certified Manufacturers**
  - Cobham, Colorado Springs, CO
  - Honeywell, Plymouth, MN
  - Cypress, San Jose, Ca (Planned)
- **Certified Assembly and Test**
  - Kyocera, San Diego, CA
- **Certified Column attach service providers**
  - Six Sigma, Milpitas, CA
  - Micross, Crewe, UK
  - BAE Systems, Manassas, VA
- **Recommendation**
  - Recommend developing slash sheets for BME (Base Metal Electrode) IDCs (Inter-Digitized Capacitors) ASAP

Note: Certification is demonstration of capability to produce a part, and qualification is actually producing the part per the space requirements.

Released SMD for First Class Y Part

REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED

Preliminary
Last updated
6/9/17

Class Y SMD

(Class Y Ceramic non hermetic flip chip LGA devices)

REV																			
SHEET																			
REV																			
SHEET	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33

REV STATUS		REV											
OF SHEETS		SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14

PMIC N/A	PREPARED BY Phu H. Nguyen	DLA LAND AND MARITIME COLUMBUS, OHIO 43218-3990 http://www.landandmaritime.dla.mil
STANDARD MICROCIRCUIT DRAWING THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE	CHECKED BY Muhammad A. Akbar	
	APPROVED BY	MICROCIRCUIT, CERAMIC NON HERMETIC FLIP CHIP, DIGITAL, CMOS SOI, GATE ARRAY HX5000, RADIATION HARDENED, MONOLITHIC SILICON
	DRAWING APPROVAL DATE	
AMSC N/A	REVISION LEVEL	SIZE A / CAGE CODE 67268 / 5962-17B01
		SHEET 1 OF XX

DSCC FORM 2233
APR 97

5962-EXXX

DISTRIBUTION STATEMENT A. Approved for public release; distribution is unlimited.

STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: XX-XX-XX

Approved sources of supply for SMD 5962-17B01 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DLA Land and Maritime-VA. This information bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535. DLA Land and Maritime maintains an online database of all current sources of supply at https://landandmaritimeapps.dla.mil/programs/smcr/default.aspx

Standard microcircuit drawing PIN 1/ 2/	Vendor CAGE number	Vendor similar PIN
5962H17B0106YXC	34168	HX518X
5962H17B0106YYC	34168	HX518Y

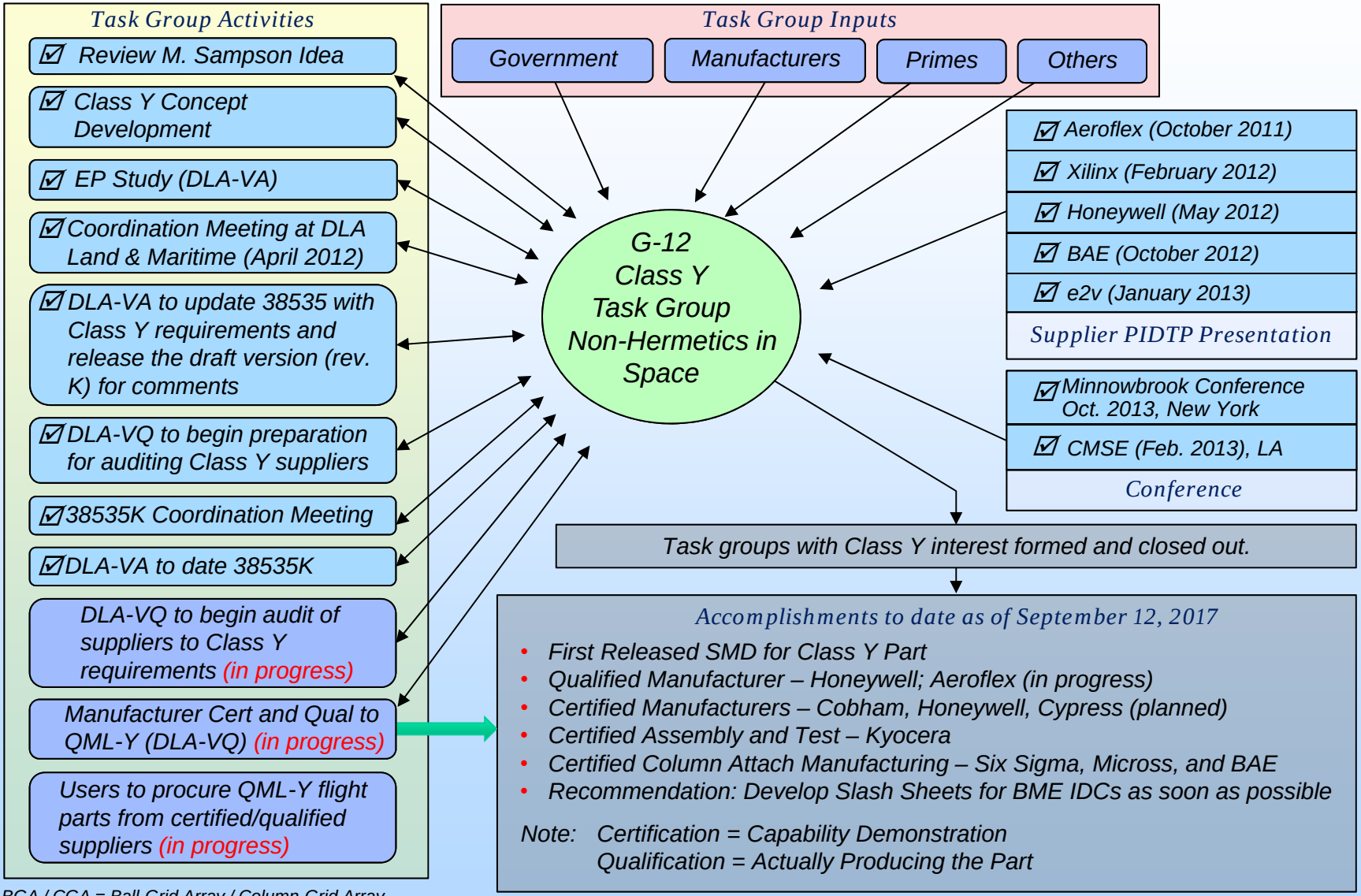
1/ Microcircuits devices supplied to this drawing are land grid array (LGA) packages with lead finish mark letter C (gold). However,for future AID drawing column grid array (CGA) or ball grid array (BGA) packages terminal lead finish mark shall be provided with "F".

2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

Vendor CAGE number	Vendor name and address
34168	Honeywell Aerospace - Plymouth 12001 Highway 55 Plymouth, MN 55441-4744

The information contained herein is disseminated for convenience only and the Government assumes no liability whatsoever for any inaccuracies in the information bulletin.

Infusion of the New Class (Y) Technology into the QML System for Space



BGA / CGA = Ball-Grid Array / Column-Grid Array
BME = Base Metal Electrode
IDC = Inter Digitized Capacitor

PIDTP = Package Integrity Demonstration Test Plan
SMD = Standard Microcircuit Drawing

Signal Integrity Capacitors

- New technology high-speed devices require signal integrity capacitors
  - Commercial capacitors of base metal electrode (BME) construction were designed into the products
    - Tiny, low voltage
- A task group comprised of the manufacturers and the users developed a screening specification
- Status
  - The general specification MIL-PRF-32535 and a set of 10 slash sheets were released.
  - The slash sheets for the interdigitated capacitors (IDCs), used in Xilinx Virtex 5 FPGAs and other new devices, are being worked.

Other JEDEC/G11/G12 Major Activities Supported by NASA

- Leak rate and residual gas analysis (RGA)
- New technology insertion (>2D packaging)
- GaN, SiC Working Groups
- Hybrid element evaluation
- Passives
- Radiation hardness
- Plastic encapsulated microcircuit (PEM) screening and qual flows
- Copper bond wires qualification, testing
- Other

Electronic Parts and ESD – NASA Concerns

- **MIL-STD-883, Test Method 3015**
  - Too old
  - Includes only the human body model (HBM)—no mention of the charge device model (CDM),
  - Must be revisited for new technology
    - Smaller feature sizes (down to 45 nm)
    - More contacts/pins (~1750 for Xilinx FPGA)
    - More items; hence, more testing time and touches
    - packaging advances going vertical (2.5D, 3D)
    - Cumulative result: increased danger of ESD damage
- **MIL-PRF-38535, Performance Specification for Microcircuits**
  - DLA audits of microcircuit manufacturers and their supply chains
    - Are done to the requirements stated in 38535
  - Poor coverage for ESD
    - No CDM testing required
    - Confusing requirements (e.g., 3 zaps/pin 883 vs. 1 zap/pin for HBM test)
    - No requirements for wafer foundries
    - Many new technologies not covered
    - No requirements for shipping and handling of products in multi-stop supply chain production (which is becoming the norm)
  - Needs to be updated

ESD and Electronic Parts

- **NASA Parts Bulletins**
  - **Special edition on ESD**
- **Invited Talks**
  - **By STS at Space Subcommittee in September 2016**
- **DLA Engineering Practice (EP) Study on ESD**
  - **DLA presented the results of their EP study in January 2017**
- **A New JC-13 Task Group on ESD**
  - **JC-13 voted to open a new Task Group on ESD (Chair: P. Coe)**
- **JEDEC/ESDA Joint Effort**
  - **JESD 625B and S20.20 Harmonization telecons**
- **MIL-STD-883, Test Method 1014**
  - **Added Para 2.2.1d. "ESD Protective Tubes shall be utilized to ensure the system is ESD safe…"**
- **NASA ESD Surveys**

Electrostatic Discharge

- ***NASA EEE Parts Bulletin (August 2016 – May 2017)***

National Aeronautics and Space Administration

EEE Parts Bulletin

Electrical, Electronic, and Electromechanical

A periodic newsletter of the NASA Electronic Parts Program / NASA EEE Parts Assurance Group and the Jet Propulsion Laboratory

August 2016–May 2017 • Volume 9, Issue 1 (Published since 2009), June 16, 2017

Second Special Edition on Electrostatic Discharge (ESD)

Damage from ESD is a major cost to the microcircuit industry in terms of time, money, and mission risk. The first issue dealt with the need to upgrade specifications related to ESD and suggestions for better ESD practices wherever parts are manufactured, stored, or prepared for shipment. This second ESD special issue focuses on a parts failure investigation that ultimately concluded that ESD was the most likely cause of the failure. The issue also includes an important reminder about regular ESD testing and a table of standard microcircuit drawings that were recently reviewed,

Figure 1 is an example of damage that was probably caused by ESD.

Fig. 1. Detailed view of a damaged site on a metal oxide semiconductor field-effect transistor (MOSFET) probably caused by ESD.

ESD, the Silent Killer—

A. Background

There are several great points to consider with respect to ESD knowledge, practice, and compliance. However, the key for ESD program success is consistency. If we detect the results of an event, then, we [the operational group] should be able to ascertain and confirm that we never have any lapses in the program implementation. With systematic practices, we should be able to surmise that there is no way any events can occur on the organizational project watch.

ESD is the silent killer in electronics, and the resulting impacts are hidden project costs that are the motivator to address project risk cost and schedule impacts. When an ESD event occurs, one of three scenarios may play out.

1) There is no impact, and no detrimental result.

2) There is a catastrophic strike and the immediate

1

and shipped off for failure analysis.

Figure 2 shows the PCB assembly with two noted nonfunctional parts circled in red. Although not conclusive, the corner location of damaged parts on the board was thought to be important to the forensics analysis. One theory implied that handling of the board (by the perimeter) allowed for the ESD event to contact these parts directly. During transport, the board is handled only inside an ESD-approved materials bag. There were questions as to the integrity of these transport bags. Due to bag traceability and reuse issues, there was no definite conclusion on this concern.

Figures 3 thru Figure 7 Show the die and damage areas from various photographic and radiographic perspectives. During upper-level assembly circuit troubleshooting, the potential for design or operational damaging voltages to the MOSFET gates were conclusively ruled out. The circuit was incapable of generating the necessary damaging voltages that would have the effect observed.

C. Investigation Conclusion

The conclusion of this ESD failure investigation was that failure was attributed to user error but review of all ESD compliance logs showed that all precautions were taken during operator handling. Due to lack of further evidence, the OCM and the PCB assembly operation were not ruled out as possible culprits, but neither could be confirmed.

Under these circumstances the team was advised of the event and warned of the total cost for repair and the need to double check all future handling procedures. The board was repaired with same lot date code parts, and there were never any repeat operational issues with that PCB assembly nor at the box operational level. The "Silent Killer" only struck once on that program. At least as far as can be determined at this time.

Figures 1 through 7 (provided courtesy of NASA Langley Research Center) were generated by Hi-Rel Labs as part of a project Component Failure Investigation at Langley.

For more information, contact

John E. Pandolf 757 864-9624

2

circled in red.

Fig. 3. Optical micrograph of the die in the failed device. The red arrows indicate the damage sites.

damage sites on the die.

Fig. 5. SEM image of one of the damage sites. The arrow indicates the area where the damage originated

ET after delayering. The arrows indicate the damage at the ends of the gate runners.

Fig. 7. SEM image of another damaged area on the die. Note that the gate polysilicon fused during the failure, which is why the oxide is visible.

3

NASA Electrostatic Discharge (ESD) Surveys of Microcircuit Manufacturers & Their Supply Chains

- Candidate companies for NASA ESD survey are identified during the DLA audits.
- These are independent surveys by NASA—Not a part of the DLA audit process.
- The purpose of these surveys is to better prepare manufacturers to develop space products.
- The findings of the survey are non-binding.
- There has been good feedback from companies that went through it.

Growing Complexity/ESD Challenges in Shipping and Handling

A New Trend – Supply Chain Management
Ensuring gap-free alignment for each qualified product
(All entities in the supply chain must be certified/approved)

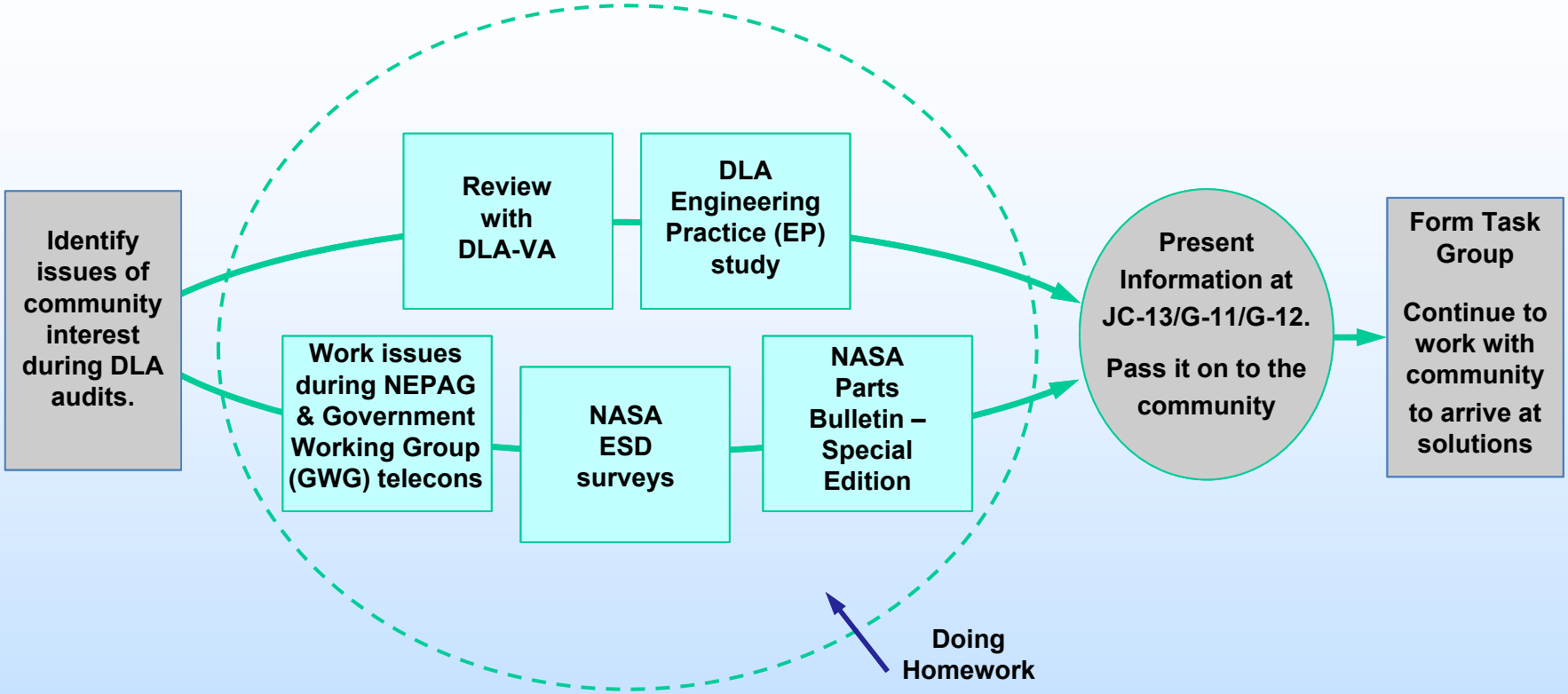
Manufacturer A	Die design
Manufacturer B	Fabrication
Manufacturer C	Wafer bumping
Manufacturer D	Package design and package manufacturing
Manufacturer E	Assembly
Manufacturer F	Column attach and solderability
Manufacturer G	Screening, electrical and package tests
Manufacturer H	Radiation testing

How Audits & NASA Surveys Help Expedite Issue Resolution at JEDEC/G12

- **Audits: NASA, Aerospace Corporation, & other organizations often participate along with the Defense Logistics Agency (DLA) Land & Maritime personnel in DLA audits. DLA audits get better electronic parts by monitoring compliance with the MIL specs & by working with the manufacturers to enhance quality of their products.**

- **Surveys: NASA has conducted electrostatic discharge (ESD) surveys of parts manufacturers. Those surveys produced recommendations regarding ESD mitigation and control. These recommendations are not enforced, but the surveyed companies all implemented the suggestions.**

Taking Audit Findings a Step Further!
NASA Timesaving Approach



- Bring general awareness (Via NASA Bulletins, Surveys)
- Work with DLA to help them conduct an engineering practice (EP) study
- Generate a basic proposal and related information so the potential task group (TG) has a strong starting point.
- This path has saved time in resolving major issues found during audits.

Issues from Microcircuit / Other Audits and Methods of Resolution

Audits						
Class Y	New Technology Infusion		NASA Parts Bulletin	DLA Engineering Practice (EP) study	G-12 Task Group (TG)	MIL-PRF-38535 Revision K
Burn-in	Varied interpretations of requirements			DLA Engineering Practice (EP) study	JEDEC Task Group (TG)	JEP163. TG still open
Underfill	Difficulties in meeting requirements		NASA Parts Bulletin – Special Edition on Underfills	DLA Engineering Practice (EP) study	JEDEC Task Group	Resolved
ESD	Old/inconsistent requirements (e.g. 3 zaps vs 1 zap per pin)	NASA ESD Surveys	NASA Parts Bulletin – Special ESD Edition	DLA Engineering Practice (EP) study	DLA presented EP results in January 2017	JC-13 ESD task group formed
Crystal Oscillators	Per manufacturers, practically no sales for QPLS oscillators		NASA Parts Bulletin – in preparation	DLA EP study planned	DLA talk at Space meeting last September	New issue

Process Flow:

*DLA Audits: Major issues uncovered during DLA audits

*NASA Parts Bulletin – Special Edition: Gives subject matter background. Provides results of NASA evaluations, ESD surveys, etc.

*DLA EP Study: A large survey of manufacturers, users, others.

*JEDEC/G11/G12 Meetings: Where discussions are held.

Growing Use of NASA CubeSats and SmallSats

- **Trend toward CubeSats and SmallSats**
  - **Many new NASA flight missions are CubeSats and SmallSats.**
  - **The weekly NEPAG telecons discuss types of standard products that would fit those applications, including commercial-off-the-shelf (COTS) plastic encapsulated microcircuits (PEMs).**

- **Three parts manufacturers are offering customized parts.**
  - **Cobham Aeroflex has several flows assigned based on extent of testing to assist users in picking the best parts.**
  - **Texas Instruments offers parts in five different versions, including their QML offerings.**
  - **Linear Technology plans to offer PEM products with guaranteed total dose radiation (rad tolerant, RT) ratings.**

Standardized Flows for NASA CubeSats and SmallSats

- **The need for standardization**
  - **The developments discussed on previous slide are all good, but**
  - **It would be cumbersome to manage multiple nonstandard flows.**
  - **Moreover, some of these approaches may or may not apply to NASA missions depending on acceptable risk levels.**

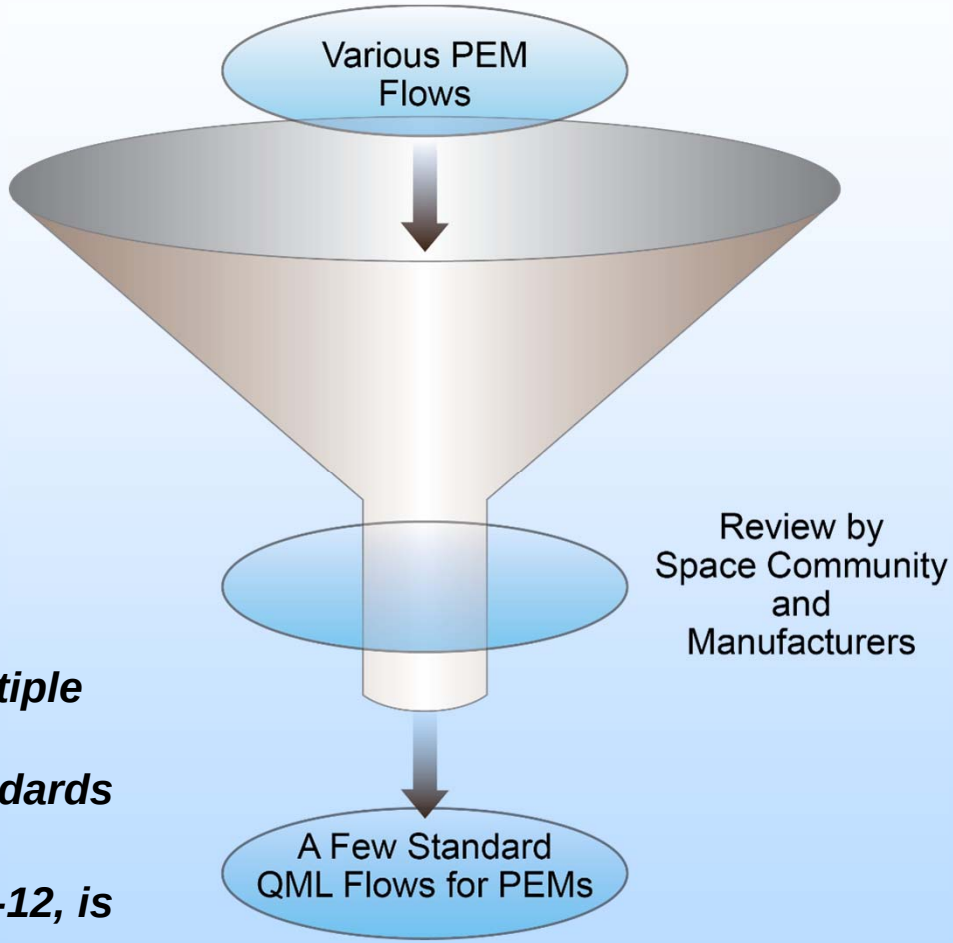
- **Possible methods to get standardized flows**
  - **The ideal situation would be for the space community and manufacturers to agree on a limited number of standard QML PEM flows to offer solutions for small missions (CubeSats, NanoSats, SmallSats, etc.).**
  - **There is an existing QML N flow for standard non-space PEM devices.**
  - **G12 developed a document SAE AS6294**
  - **In addition, DLA has Vendor Item Drawing (VID) program and parts built for automotive applications.**
  - **Of course, every major issue needs to be discussed.**

PEMs for Space

- ***Newer Applications***
  - ***CubeSats***
  - ***SmallSats***

Standardizing on a few well-defined flows rather than multiple flows defined by each manufacturer or by each standards group.

SAE AS6294, developed by G-12, is one candidate.



DLA's VID (Vendor Item Drawing) Program

Current Supplier's Program Benefits

1. Single Standardization Document
2. Controlled baseline.
3. Enhanced product change notification of processes, materials, electrical performance, finish, molding compounds and manufacturing locations.
4. Extended temperature performance.
5. Enhanced Pedigree - Reliability and electromigration checks, electrical characterization over temperature and confirmation of package performance over temperature.
6. Enhanced Obsolescence management.
7. No pure tin.
8. No copper wire bonds.

See the attached listing or check our website for an up to date list of product coverage.

DSCC ANNOUNCES THE RELEASE OF A NEW TYPE OF STANDARDIZATION DOCUMENT.

DSCC is releasing new Vendor Item Drawings (VIDs) almost daily. These documents have been created to provide a procurement vehicle for enhanced commercial products. Specifically, commercially available microcircuit products are being documented for the first time on a standardization document. Use of these DSCC VIDs will avoid the use of manufacturer generated specification control drawings (SCDs) or manufacturer's VIDs and avoid the potential proliferation of non-standard products. The participating manufacturers have agreed to provide information and services that have not traditionally been associated with commercial products. See our website for a list of documents that are currently available.

All Vendor Item Drawings are ***NOW*** available on the DSCC web site

http://www.dscc.dla.mil/Programs/MilSpec/

- **Analog and digital functions offered.**

Evaluating Automotive Parts for Potential NASA Applications

- The main drivers are size, weight, and price of electronic components
  - Commercial electronic parts usually offer varied functions
  - How do automotive parts compare to catalog commercial?
- Commercial Parts Options
  - Manufacturers make parts to meet the needs of their chosen market(s)
  - Automotive parts are designed to meet the needs of subsystem suppliers to automobile manufacturers
- Space
  - Parts from manufacturers that are qualified to the Automotive Electronics Council (AEC) Q specifications seem to offer advantages for the smallsat users
  - NASA is doing a limited evaluation of automotive electronic parts

Evaluating Automotive Parts for Potential NASA Applications

AEC Q specifications are Qualification Requirements Only, Focused on:

- **A One-Time INITIAL QUALIFICATION of a Device Family**
  - **"Device Family" is Common Materials, Processes, Designs, Manufacturing Location, etc.**
  - **"Generic Data" may be used provided relevance of data can be demonstrated**
- **Requirements for REQUALIFICATION**
  - **Provides recommendations as needed**
- **Requirements for process change notification (PCN) to automotive customers**
- **THEY DO NOT PROHIBIT PURE TIN**

– Whisker mitigation is recommended!

Counterfeit Parts

- Refers to counterfeit parts awareness and mitigation.
- GIDEPs (Government Industry Data Exchange Program [reports]) on counterfeit parts are reviewed on NEPAG telecons.
- During the DLA audits, the manufacturers are asked for their counterfeit mitigation plans. Most of them have some form of mitigation.
- NASA provides counterfeit training.
- NASA supports the SAE (Society of Automotive Engineers) effort.
- Procure parts, particularly new technology devices, from the authorized sources.

NASA Workshop

- **Workshop**
  - **NASA's Electronic Technology Workshop (ETW) is held in June every year**
  - **Venue: Goddard Space Flight Center, Greenbelt, MD**
  - **Past papers posted on NEPP Website:**
    nepp.nasa.gov
  - **See above website for other details**

NASA's Cassini: The Grand Finale

- Was launched two decades ago.
- An incredible mission to planet Saturn.
- Provided new insights into Saturn's interior structure, its moons, and its rings
- It was my distinct privilege to be the parts specialist for microcircuits and crystal oscillators that were used on Cassini.
- Cassini made several orbits that swooped between the rings and the planet before ending its mission on September 15, 2017, with a final plunge into Saturn.

- Please watch the video for Cassini (courtesy of NASA/JPL- CalTech; see videos of "Cassini's Last Looks at Saturn" and "The Beauty of Saturn" at

https://www.nasa.gov/mission_pages/cassini/videos/index.html).

Conclusion

- Evolving products incorporating new technology is an on-going challenge.
- NASA supports a wide spectrum of space missions/programs ranging from smallsats/cubesats to flagship missions such as Juno and the planned Europa mission. The success of each mission is important.
- NASA is working with the space community to help infuse new technologies during the coming decade.
- The JAXA Microelectronics Workshop (MEWS) is an extremely useful resource in these endeavors.

Thank you!

http://nepp.nasa.gov

ACKNOWLEDGMENTS

The research described in this publication was carried out, in part, at the Jet Propulsion Laboratory, California Institute of Technology, under a contract with the National Aeronautics and Space Administration.

Help is gratefully acknowledged from Roger Carlson, Mohammad Mojjaradi, Joon Park, and Michael Sampson.

Government sponsorship acknowledged.