Power and Signal Integrity Findings in a FPGA Layout for an Aerospace Application

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Abstract: **Design principles concerning the use of FPGA are of particular importance in aerospace applications since the neglect of such design principles can cause catastrophic effects in aerospace system, as it will be explained in this paper. FPGA design rules such as power conditioning and signal integrity for properly interfacing high speed FPGA with its interface circuits are discussed in this paper as it relates to aerospace systems. Signal integrity to avoid crosstalk within a FPGA has not been a great concern because most of the attention over the years had been on signal integrity at the PCB level. However, this paper shows a real example of crosstalk within a FPGA in an aerospace application.**

I. INTRODUTION

The convergence of Field Programmable Gate Arrays (FPGA) design with issues related to their layout design principles, their power conditioning, and their signal integrity was just a matter of time. The interactions of FPGA with other circuits in a Printed Circuit Board (PCB) have become of interest in the past few years as these FPGA are increasing handling switching speeds whose frequencies are very high (e.g. > 2GHz) and where the wavelengths are now comparable to the physical size of the Printed Wiring board (PWB) layouts features, and where passive components are now behaving more as components with complex inductive and capacitive parasitic effects. This evolution has also caused studies in power supply requirements for FPGA where power supply distribution networks need to be of better design to accommodate fast current surge in an increasingly Radio Frequency (RF) behavioral environments.

Power conditioning in PCB layouts has been a good area of research and a design constrain over the last decade and a half. Mix mode design accommodations have been needed to implement more complex architectures dealing with analog digital converters (ADC) and sensors acquisitions data, together with the high-speed processing of such data. Many papers have been written concerning power switching generated noise. Likewise, considerable effort has also been dedicated to address the topology of PWB designs, as signal integrity has become an issue in digital designs [1-6]. Signal integrity issues such as crosstalk, differential, and common mode interference have become areas of active research in the past and there is ample work in the technical literature for diagnosing and minimizing the effects of such signal integrity problems in PCB.

Past work in these areas have dealt very little with FPGA. For example, most of the design work and the design tools used to address signal integrity are mostly tailored to the design of PCB. A widely used tool in the aerospace industry for the design of PCB is Hyperlynx from Mentor Graphics. Because the tool was developed to address mainly parasitic effects for PCB, it can be difficult to perform such modeling in very small and highly dense layouts such as those found within a FPGA where the footprints of all the electrical features are very small. Therefore, in most aerospace application designs, including those performed by this author, Hyperlynx is used mostly in PCB and used also for designing the interfaces between FPGA and signals lines in the PCB. We therefore, perceive the need for better tools to address proper power conditioning and signal integrity design within a FPGA and within Application Specific Integrated Circuits (ASIC) in future work, and especially as it relates to aerospace applications because of the high levels of required reliability for aerospace hardware. Most digital designs in PCB are moving away from discrete components and incorporating systems on a chip, basically using FPGA and ASIC. It is the cleanliness of the FPGA or ASIC, in terms of power integrity

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and signal integrity, which will dictate in the future the overall behavior of the PCB (which are also decreasing in size as less components are needed). The analog world is also moving in that direction, but it will take another ten years in this author's opinion for analog technology to reach the level of compactness expressed in digital technology in the form of ASIC and FPGA.

There has been some preliminary work which shows how important FPGA timing controls are for the overall timing integrity of the board [7-8]. In aerospace applications, the widespread use of FPGA in critical control functions requires that even a greater effort must be made in insuring the avoidance of power conditioning and signal integrity issues. In this paper we provide a brief overview of both power and signal conditioning design principles applicable to FPGA, which are established knowledge in the aerospace industry. We provide information of why these design principles are so critical in aerospace applications and they are worth mentioning them here. We then proceed to discuss signal integrity and more specifically the findings of crosstalk within a real FPGA that was used in the performance of control function in an aerospace application.

II. POWER CONDITIONING FOR FPGA

We now briefly address three issues that can be implemented as design principles for proper powering of FPGA in high speed signaling applications, such as in control functions for aerospace applications.

A. Powering up FPGA followed by POR

In the process of powering up a FPGA there is a period of high transient current (Icc) which occurs when the FPGA pump is enabled and all the logic within the FPGA is connected to Vcc routing tracks. The transient currents start when Vcc reaches between 1.5V and 2V in most typical FPGAs. The duration of the transient current depends on the Vcc ramp rate, but usually is in the order of hundreds of µS. Often, FPGAs are designed such that their I/O go to a high impedance (HZ) tri-state condition until the FPGA becomes fully functional. For a FPGA whose application is in command and control, as it is often in an aerospace applications, it is very important that a tri-state HZ condition is maintained during power up, otherwise, I/O conditions of HI or LOW could occur which can create inadvertent commanding with potential reliability risks for aerospace applications such as the inadvertent firing of pyros or the command of inadvertent maneuvers which could disable the aerospace asset. This author has observed such erratic behavior during powering up in the Actel 1280 FPGA, used in aerospace applications in the 1990's and early 2000's. Because flip-flops in FPGA are not designed to power-on in any given state, a Power-on-Reset (POR) circuit is recommended to reset the FPGA before accepting any I/O. POR designs are now part of most control circuits designs for aerospace applications using the Microsemi RTAX series FPGA. Fig. 1 shows a typical POR circuit (R1 is omitted in TTL circuits).

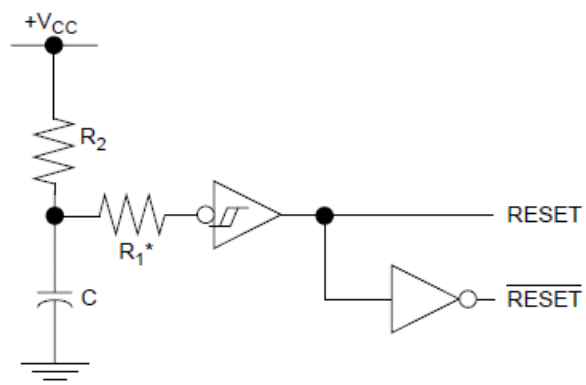

Fig. 1. Typical POR Circuit for FPGA

The Schmitt trigger in the figure is making the reset signal to switch off cleanly.

B. Power Sequencing for FPGA

Most FPGA require at least two voltages, the core voltage V_core and the I/O voltage V_io. During power-up both voltages ramp up to a level voltage within 5% of steady state tolerance. The ramp rate is between tmin/V_core and tmax/V_core. The ramping is due to the presence of a POR and/or an externally present voltage controlled oscillator (VCO) used for sensitive analog circuitry in the FPGA such as a Phase Locked Loops (PLL). The charging current during ramping up is I_charge = Cb*dV/dt; where Cb is the bypass capacitance of several µF. The charging current is in the order of several amperes, reaching I_core(max) before settling to the steady-state (SS) current, I_core(SS), as shown in

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Fig. 2. All FPGA require large transient in-rush current to charge up the capacitance of millions of its internal components and provide a quick low resistance path to ground. Most aerospace applications use the more reliable DC/DC converters which have very low input and output impedance and fast response time which are needed for intensive FPGA applications.

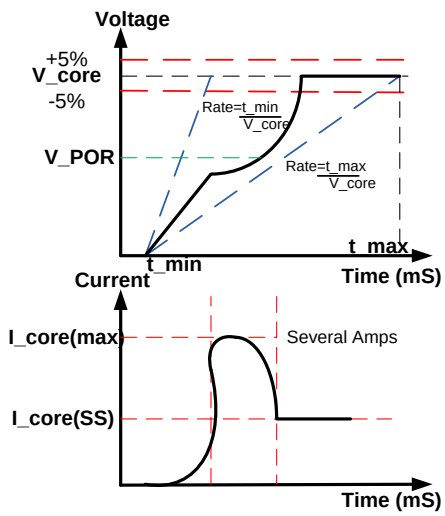

Fig. 2. Voltage and current profiles during powering up in a FPGA

In an optimal approach to power sequencing for aerospace applications, a dedicated DC/DC converter will supply Vcc_core, and linear regulators, enabled by power monitoring circuits in the DC/DC converter, will supply V_io and other power needs of the FPGA. This approach in power up could be sequential in nature which would prevent the execution of control functions by the FPGA that could activate, in an aerospace application, a sequence of commands in an inadvertent manner. The inadvertent applications of commands due to unpredicted power sequencing caused the loss of at least two spacecraft in the first decade of the 2000's.

C. *Clean Analog Power in FPGA*

FPGA can interface with analog components such as PLL or interface with analog integrated circuits (IC) in a PCB layout which is very common in aerospace applications. Just about every digital board and most of the mixed analog/digital board in aerospace systems have at least one FPGA and/or ASIC. Just about all the control boards in aerospace applications, where analog circuits abound, use either ASICs or FPGAs. Analog devices are highly sensitive to noise. Noise caused by variations in the power supply voltage can couple to analog devices and amplified along with the desired signal. This can result in processing errors that affect the overall system. The digital gates in the FPGA consume switching power. The current drawn from the power supply leads to parasitic (frequency dependent) voltage drops (IR drops) in the Vcc and Vss (ground) traces in the PCB. This occurrence is known as ground bounce in the Vss plane (see Fig. 3). The ground bounce is related to the parasitic inductances of the package layout and IC, device ground, and system ground. This dynamic current can transform into noise by a noise voltage (Vn) calculated to be Vn= L dV/dt. In aerospace applications good grounding techniques must be followed to address the charged space environment, but an added benefit of good grounding techniques is the avoidance of ground induced interference.

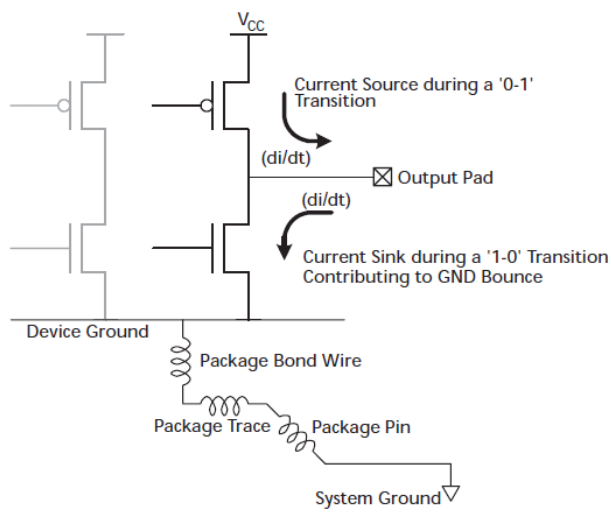

Fig. 3. Parasitic inductances causing ground bounce.

Large current loops will increase the signal rise time and it will also increase crosstalk due to the increase capacitance. Minimizing loop area between signal planes and ground planes and minimizing the inductance in such planes will substantially decrease the noise voltage. A typical configuration showing such arrangement is shown in Fig. 4 [8]. Notice the interlaying of ground planes around signal and power planes.

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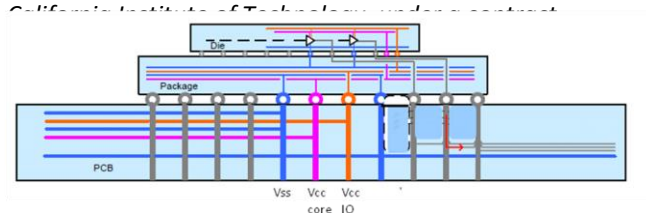

Fig.4. Example of power rails in a FPGA

III SIGNAL INTEGRITY AND FPGA

A. Crosstalk Findings of a FPGA in a PCB

In a PCB, signal integrity (SI) is dependent on having transmission lines with controlled impedance in the frequency range at which the PCB operates. The impedance is determined by the geometry of the traces and the dielectric constant of the board in and around where the traces are located. If the impedance can't be controlled because of parasitic (capacitive, inductive) effects in the transmission lines, noise problems can develop which will affect the signal integrity during propagation. These noise problems are often related to power distribution issues (as discussed above) but can also be related to crosstalk among signal lines.

In a PCB one or more FPGA signal integrity issues can also develop. In a pre-layout Signal Integrity (SI) analysis, nets with the fastest edge rate or with the most critical timing conditions and with the greatest number of loads (e.g. FPGA) are often the most susceptible to signal integrity degradations. Once the critical nets are identified, the next step is to address the topology of each of the nets, from driver(s) to receiver(s) via simulation (behavioral models or transistor level models). These simulations use the physical and electrical parameters of the links and it help us: 1) identify the maximum link length and other properties that will meet the noise margin criteria., 2) help define the FPGA buffer properties such as driver strength and slew, 3) define the FPGA receiver buffer properties, 4) perform crosstalk analysis to verify that adjacent nets do not affect each other's quality of signal, and 5) help defines termination strategies that will minimize ringing and other phenomena which could affect signal propagation quality. Termination strategies can be either serial or parallel and each strategy needs to be evaluated and be most useful to the designer's system environment. In a post-layout SI analysis, after the board place-and-route is finished, we need to perform SI analysis on the most critical nets of the design to assure that the noise level in the implemented links is within margins defined by the design specifications. The analysis is often of the same type as the pre-layout analysis, but this time the emphasis is on crosstalk and Electromagnetic Interference (EMI) analysis, since at this point we know the actual layout of traces. If problems are found in this post layout analysis with a net, it can be redone until the requirements are met.

The simulation results below show an example of a crosstalk scenario (post layout) between an aggressor net connecting a FPGA input to an Integrated Circuit (IC) in the PCB and a susceptible net connecting an FPGA output to a receiver IC. The results show crosstalk among the two nets involving FPGA in a PCB during post layout analysis. Output was provided by Mentor Graphics Hyperlynx tool.

```
"NET = /FIRING PYRO_FPGA_RESETN
  ELECTRICALLY ASSOCIATED NETS ----------------------
----------------
NET = /FIRING PYRO_FPGA_RESETNX
AGGRESSOR NET (Estimated peak crosstalk)
/TS_SE_1_ = 178 mv
   Total estimated crosstalk =178 mv
   ** Warning ** Estimate exceeds maximum allowed cross-
talk!
NET = /WTA_CLKN_ 45(VICMIM NET)
  SIGNAL-INTEGRITY STATISTICS ---------------------------
---------
total receiver capacitance ... 3.2 pF
effective net Z0 .............58.7 ohms
termination type .........No termination found
  TERMINATION VIOLATIONS -------------------------------
-----------
   ** Warning(Severe) ** CROSSTALK VIOLATION and
SUGGESTED FIX
Net too long!
found length ............ 000.543 in
max. recommended length. 000.438 in
 Add a series terminator at the driver or reroute to reduce the
net length.  Or use driver with slower output.
Resistor suggested ...... 46.2 ohms"
```

The above simulation shows just one example (of a recorded output) among hundreds of nets that had to be analyzed for crosstalk. The simulations for the above cases were done with the Mentor Graphics Hyperlynx tool in an aerospace application. The analysis shows a

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178mV crosstalk between a reset command signal from a FPGA to a pyro circuit interfering with a CLK signal. The crosstalk can be reduced by decreasing the net length and a few options are available to the designer.

In addition to crosstalk concerns, the *timing analyses* of the FPGA must be assessed, and such timing analyses is quite different when comparing the pre and post layouts timing analyses. Static and dynamic timing analyses are important steps in verifying the performance of the overall design incorporating the FPGA and the board. The static timing analysis is mostly pre-layout while the dynamic timing analysis is post-layout. The timing analyses usually report maximum clock frequency, input to register delays, register to output delay and input to output port delays for best, worst, and typical cases based on user preference. Path delays are reported on real pin-to-pin model where all the gated and net delays are considered and reported individually. The whole delay in the path is the individual sum of all the net and gate delays in the path. For example, Fig. 5 shows a sample of a few FPGA nets and the type of delays that are calculated in static timing analysis in a pre-layout configuration.

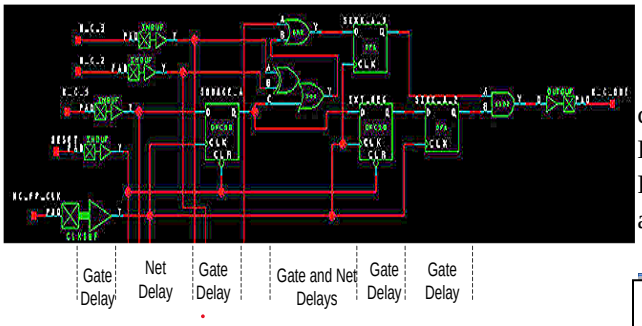

Fig 5. Showing different paths delays is a static timing analysis

In post layout configurations the parasitic transmissions lines effects of the board layout must be considered. Both capacitive and self/mutual partial inductance of PCB lands must be considered [9]. Dynamic timing analysis is considered for post layout configurations and it must accounts for the timing analysis from FPGA outputs to all the interface circuits on the board.

B. Crosstalk Findings Inside a FPGA.

The following crosstalk scenario was the first case of crosstalk inside a FPGA discovered by this author in his experience. Limited literature research conducted by this author also found no studies of crosstalk inside a FPGA. The crosstalk was discovered during testing of a control board for an aerospace application. As a consequence of this finding, during test, the FPGA design was updated, and the new implementation proved to be satisfactory. Nevertheless, this finding shows that small EMI problems can cause significant cost and delays issues in aerospace systems development since this whole process took several weeks to resolve.

In an aerospace application, and in the development of a control board, a FPGA signal is used to command a memory dump to several memory ICs. It was noticed that memory errors were observed in the form of several error words in the memory. A partial list of the wrong words in memory are shown in red color.

00056dd2 00038ff3 00048ff5 00046ff5
0056ff8 00046ff9 00046ff8 00046ff9
00046ffb 00046ffc 00046ffd 00056ffe
00056ffe 00046ffd 00047000 000450d2
00033902 00032701 80023802 00042801
00033903 00032703 80023804 00042802
90033905 00032704 80023806 0007700f
0009800d 000570ff 00047010 00077011f

The timing of the several FPGA critical signals, including the command signal, were analyzed on Silicon Explorer tool. The results are shown in Fig. 6. Notice in Fig. 6 that an extra bit (shown by the arrow) shows up in an otherwise regular train of pulses.

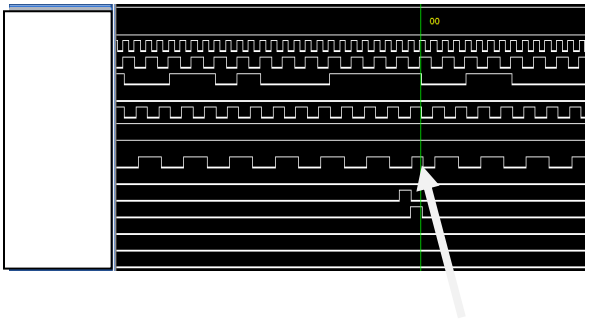

Fig. 6. Arrow showing an extra bit in a counter from a FPGA timing diagram.

Further analyses from the results of Fig. 6 and other analyses done, show that the errors in memory were

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caused by an extra bit in a counter that counts the words going in/out of memory. Notice that the extra bit is out of family as previously stated. Where does the extra bit comes from since it is not part of the design?

The next step was to assess the physical layout of the signals involved within the FPGA. After a series of investigations and tests which go beyond the scope of this paper, it was calculated that the source of the extra bit was the result of a crosstalk scenario within a FPGA. The source of EMI for the crosstalk (i.e. the offender) was a FPGA command signal from registers inside the FPGA which couples to a clock signal (victim) in the FPGA. The clock signal drive multiple flip-flops (FF) of a counter register. The crosstalk is illustrated in Fig. 7.

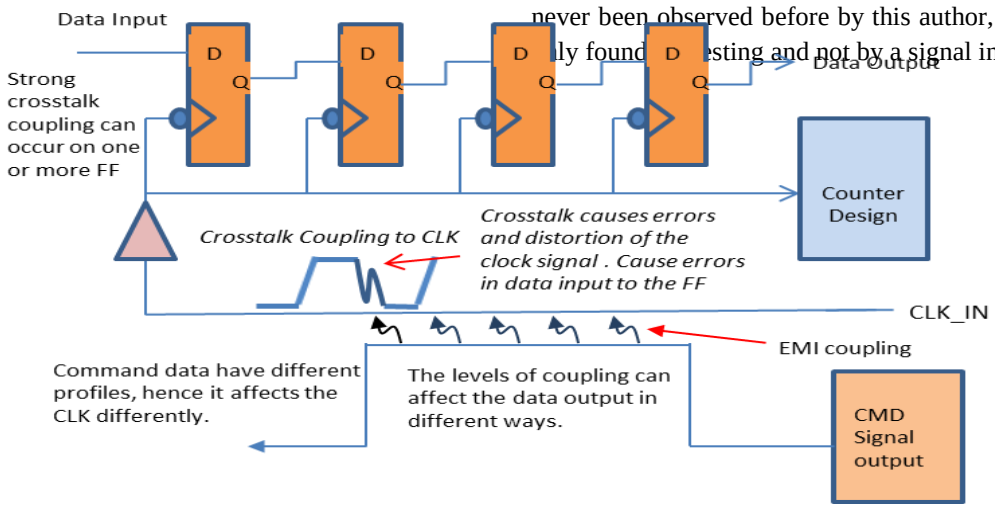

Fig. 7. Crosstalk among signals inside a FPGA.

In Fig 7 the quality of an internal clock input (clk_in) signal which drives a series of FF is affected by the signal strength of a command signal (CMD) whose layout is in very close proximity to the clk_in signal. Capacitive coupling between the offender (command signal) and victim (clk_in) are the basis of the crosstalk. The crosstalk causes a distortion of the clock signal to the FF and such distortion causes errors in the FF inputs and outputs. One or more FF can be affected simultaneously. The levels of crosstalk interference may affect the FF in different ways which are unpredictable. The end result however, is the generation of memory errors for this particular application, and in Fig 7 these errors are in the form of word errors in a memory counter. It must be stated again that the crosstalk issue was discovered by test. A signal integrity tool that could work well at the level of FPGA internal design could be very useful in the avoidance of signal integrity issues within a FPGA during the design phase.

IV. CONCLUSION

This paper addresses the important of signal and power integrity in FPGA and ASIC for use in aerospace applications. This is especially true for aerospace systems whose control functions and data acquisition functions are very much dependent on FPGA and ASIC. This paper provides numerical examples of why power and signal integrity are of particular importance in aerospace application. This paper ends by providing an example of crosstalk within a FPGA, a finding that had never been observed before by this author, and that was [illegible]ly found [illegible]esting and not by a signal integrity tool.

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