

Radiation Performance of Memory Technologies for Space Applications

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Abstract—MRAM and DRAM memory technologies identified for possible radiation hardening were investigated for memory-array- and controller-level radiation sensitivity. TID and SEE performance of memory arrays and associated cells is good, but with some questions about viability of hardening of problematic control circuitry. Control-circuitry-related SEE problems are highlighted. TID data are focused on memory arrays only.

Keywords—SEE; TID; Radiation; MRAM; DRAM

I. INTRODUCTION

Space missions require memory for many system uses, including computer main memory, buffers, program and data storage, boot ROMs (read only memory), and other applications. DRAMs are often the only viable high-density memory option for many applications due to speed and power considerations. Recent performance of dynamic random-access memory (DRAM) has shown improvement of memory-array-level radiation tolerance, with significant increases in single-event functional interrupt (SEFI) sensitivity. Meanwhile, in the non-volatile sector, currently dominated by Flash memory, total ionizing dose (TID) performance has become problematic for moderate TID space missions. Given the current shortfall in commercially available memory products with adequate radiation tolerance, power, speed, and overall lifetime reliability, it is desirable to either find or develop a memory technology suitable for future space missions.

A study focused on establishing the viability of various memory technologies was performed [1]. Based on this study, the following were determined. (A) There is no current viable memory product that provides the desired capabilities. And, (B) one of the most efficient approaches for developing a space memory that meets the desired performance goals, is to identify an already-acceptable memory-array technology and mate it with radiation-hardened control circuits (either on the same chip, or in a separate chip) that can handle radiation-induced memory array errors.

The previous study identified two specific memory technologies of interest based on maturity of the technology and ability to meet key performance metrics such as power consumption and data access speed. DRAM was chosen because it meets density and speed characteristics for applications that do not require non-volatile memory, and

because the primary application-level radiation issues are related to DRAM controllers, not the DRAM memory array. DRAM bit upsets are easily handled, provided the architecture does not generate multi-cell errors within error-correction blocks. Magnetic random-access memory (MRAM) was similarly chosen for its speed-power-density characteristics, its non-volatility, and its ability to provide sufficient radiation performance for many missions. It should be noted here that although MRAM is acceptable for many non-volatile applications, it cannot replace other non-volatile technologies, e.g., Flash, where extreme density is required. Similarly, MRAM is capable of replacing DRAM in applications where its density is sufficient. The evolving density of MRAM technology makes it an attractive technology for moderate-density applications and, with continuing density improvements and 3D chip-stacking, a potential “universal memory”.

This effort targets the radiation response of memory arrays for the individual technologies. However, radiation characteristics of the on-chip controller circuitry are necessarily gathered as part of the testing in order to establish baseline and to understand the overall chip radiation characteristics so that we can extract the memory-array radiation tolerance.

In order to minimize confusion due to the combined elements in the commercial devices we studied, we performed radiation testing in an unbiased condition where it would result in unambiguous data. This is not the standard approach to radiation testing of commercial devices, but was necessary in this case in order to minimize the potential confusion due to the myriad of errors generated by on-chip controller circuitry. It was not always possible to test unbiased. Further, it was determined that some testing that was performed unbiased would benefit from additional biased testing (this point is taken up in the discussion section below).

This paper is organized as follows. Section II gives background on the effort and how the radiation testing was focused. Section III presents efforts and results on MRAM. Section IV presents efforts and results on DRAMs. Section V provides a review of the results in the context of the effort. Conclusions are presented in Section VI.

II. BACKGROUND

The research approach used in this work focuses on isolating or highlighting radiation performance at the following functional levels of the candidate devices. The cell-level refers to the individual storage elements that store data, such as the one-transistor-one-capacitor DRAM cell. The cell-array refers to the level of the macro necessary for cells to be created by the fabrication facility. We also refer to the cell-array as the

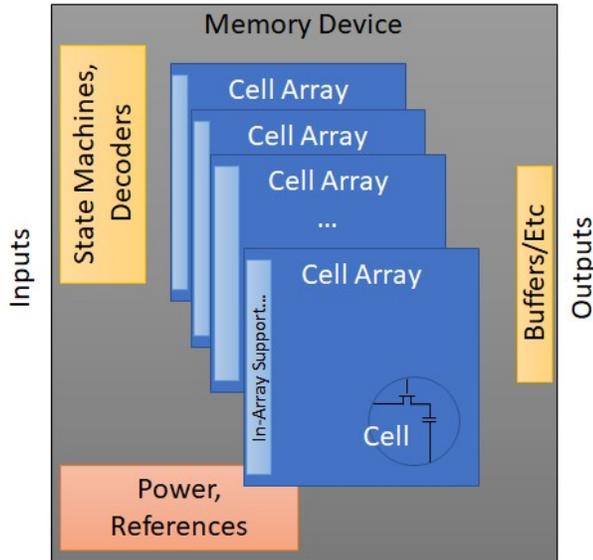


Figure 1: Cell, Cell Array (Memory Array), and Device Level – this work focuses on evaluating Cell and Cell-Array performance.

collection of many such macros, as long as no additional control logic, power, or analog support circuits are added. This breakdown is indicated in Fig. 1.

In DRAMs, it is expected that the cell-array includes some amount of decoding logic for addressing, and the read-out circuits (sense-amplifiers) that detect the charge stored on the storage capacitor during access.

In the MRAM candidate, it is less obvious what the cell array includes relative to the full device structure. However, it is expected that the cell array is repeated many times to build the actual device under test (DUT) and similar to the case of DRAMs, may also include a minimum set of integral circuitry such as decoding-logic and read-out circuits.

Once the radiation performance of the smallest reasonable building block for the memory array is found, an informed decision can be made regarding how to build an RHBD (radiation-hardened by design) memory where the memory

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array (cell array) is the existing (tested) array, but any other circuits are replaced with RHBD alternates. By doing this, the traditionally weak DRAM controllers, which have resulted in increasing low-LET SEFI sensitivity with newer DRAMs [2] can be avoided, and the device can perform up to the level of the cell array’s intrinsic performance. Radiation hardening can also be augmented by error correction or other forms of redundancy to further improve the radiation performance.

A similar argument applies to the MRAM performance, although it is not as well-established what radiation problems are the most problematic. In any case, however, identifying the MRAM cell-array’s performance can establish a level to which a device built of a standard MRAM cell array and RHBD control circuitry can achieve before the cell array itself must be modified.

III. MRAM

Commercial STT-type MRAM memory devices were tested. Radiation weaknesses of the commercial devices were anticipated before the study began as these chips do not have radiation-hardened control circuitry. However, the goals of the MRAM evaluation focused specifically on memory-cell and memory-array radiation sensitivities.

A. Single-event effects (SEE) Evaluation

No SEL was observed with Au at LET of 84 MeV-cm²/mg, with nominal device bias, at room temperature (SEL test was intended to be indicative only, rather than worst-case). Exposure level was 1×10⁷/cm².

We tested the MRAM with the device unbiased to establish limits for exposure with no bit upsets. Fluence levels achieved with no changes in the stored data are shown in Table 1.

Table 1: Summary of unbiased MRAM SBU results

Ion	Energy	LET	Fluence	Bit Errors
Ne	25 Mev/amu	1.9 MeV-cm ² /mg	2.00E+07	0
Ar	25	7.6	2.00E+07	0
Kr	25	33.7	2.00E+07	0

The only surprising result was a SEFI behavior, that occurred during biased testing, and which resulted in loss of most of the programmed data in the DUTs. Because the focus

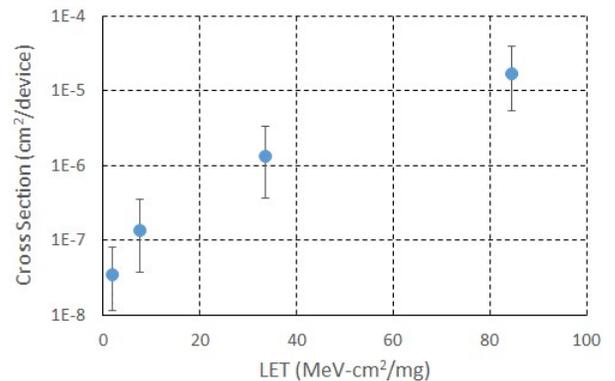


Figure 2: Sensitivity of MRAM test devices to device-wide SEFI.

of this effort was at the memory-array-level, we report these findings merely for completeness. The cross section for SEFIs in the MRAM device is given in Fig. 2.

B. Total Ionizing Dose (TID) Evaluation

We briefly discuss TID results of the MRAM devices here. We have exposed devices up to 1.5 MRad(Si). All exposures were unbiased, but future, biased testing is recommended. No changes were observed in stored data. Devices were exposed to 50, 100, 200, 300, 400, then 1,500 kRad(Si), rewriting the devices between exposures. The largest step with no rewriting was 1.1 MRad(Si). Additional testing with individual MRAM cells showed no change in data with exposures of up to 7 MRad(Si).

IV. DRAM

DRAM memory arrays were tested utilizing standard commercial devices from a candidate manufacturer and were expected to demonstrate typical DDR-class bit error performance, SEFI sensitivity, and TID performance. The effort was focused on verifying this type of standard performance to determine if these were acceptable candidates for separating memory-array and control logic for development of a radiation-hardened DRAM device that would minimize the inherent SEFI sensitivity.

A. SEE Evaluation

DDR2 devices were tested at LBL (Lawrence Berkeley National Laboratory) and TAMU (Texas A&M University) to the exposure levels indicated in Table 2, below.

Table 2: Ions used in SEE testing of candidate DDR2 device.

Ion	Facility	LET	Exposure
Xe	LBL	83 MeV-cm ² /mg	2.00x10 ⁷ /cm ²
Ne	TAMU	3.3	8.90x10 ⁶
Ne	TAMU	6	2.04x10 ⁶
Ar	TAMU	13	6.99x10 ⁵
Kr	TAMU	39.9	3.13x10 ⁵

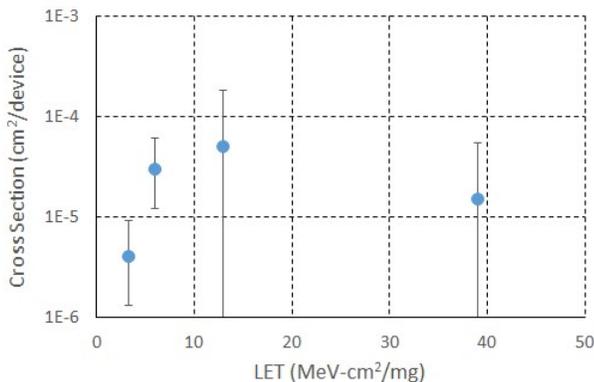


Figure 3: DRAM SEFI sensitivity. Note that many SEFIs resulted in the device showing millions of errors.

Devices were tested for SEL up to $2 \times 10^7 / \text{cm}^2$ with an LET of 83 MeV-cm²/mg with no SEL events occurring (devices held at 95°C, nominal voltage).

Devices were observed to have typical DDR2-class SEFI sensitivity of between $1 \times 10^{-5} - 1 \times 10^{-4} \text{cm}^2 / \text{device}$. SEFIs included relatively small SEFIs (100s-1000s of errors) and device-wide SEFIs sometimes referred to as “mega-SEFIs” or MSEFIs because they involve millions of errors. The SEFI sensitivity for the test device is shown in Fig. 3, above.

SBU performance of these devices is shown in Fig. 4, below. Bit errors were observed at all tested LETs. However, for LETs below 10 MeV-cm²/mg, SEFI events significantly obscured actual SBUs and may contribute to a systematic overestimate of SBUs. The ISSI 2016 data are included for comparison [2].

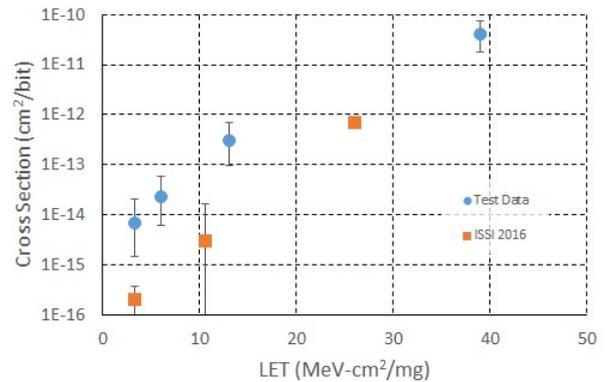


Figure 4: Sensitivity of DDR2 devices to bit upsets. This cross section is consistent with expected bit-level SBU sensitivity. No MBUs were observed in a single read operation.

B. Total Ionizing Dose (TID) Evaluation

DDR2 devices were exposed to TID using JPL’s Co-60 room irradiator. TID levels achieved were 50, 100, 200, 300, 400, 500, 600, 700, 800, and 900 kRad(Si). Two devices were irradiated – one in the static-biased configuration, and the other with a data pattern loaded into the part prior to irradiation and periodic refresh performed.

We evaluated the performance of the DUTs during TID by two means. First, we monitored the operating currents drawn by the test devices in standard operating modes. Second, we observed if any bits failed to store data under normal conditions, and under a simulated hot condition (achieved by increasing the refresh interval from 32 ms to 1 s, which simulates the charge lost in the cells during normal operation at about 75°C). This second refresh interval is used because actually heating the device will significantly alter the annealing response, which was not desired for this testing but would significantly affect an actual field use. Our testing is, therefore, conservative in regard to annealing.

Only small changes in the static bias current were noted, with increases on the order of a few mA by 900 kRad(Si).

Other operating currents for reading and writing were monitored (they are nominally over 100 mA) and showed no clear change over the TID testing.

Stuck bits were observed in both 32 ms and 1 s refresh period testing. At 32 ms, stuck bits were observed (a few 100) in the refreshed device at 400 kRad(Si). 300 kRad(Si) was the last level with no stuck bits at 32 ms refresh. At 1 s refresh, stuck bits were observed (a few 1000) in the static biased device at 500 kRad(Si). No stuck bits were observed at 1 s refresh for the 400 kRad(Si) test point and below. Once stuck bits started to be observed, the number increased but did not follow the expected rapid increase with increasing dose. Instead, the number of stuck bits was significantly dependent on time between irradiations (a 168 hour anneal occurred after the 500 kRad[Si] test point, and a 20 hour anneal occurred after the 700 kRad[Si] test point). Most of the stuck bits appeared to completely anneal between test exposures. See the discussion for more information on impact and possible follow-up testing.

V. DISCUSSION

A. MRAM

The MRAM devices tested did not show any SEE sensitivity in the cell array. Further, no stored values were lost over 1.5 MRad(Si) of exposure with stored data being rewritten, over 900 kRad(Si) of exposure without rewriting, and over 7 MRad(Si) with isolated storage cells. These results indicate the cells and associated circuitry do not have a significant risk if they are used in an RHBD device with a custom controller that is also robust to radiation effects. It should be noted that SEE testing of the storage cells in full devices (chip-level), to very high exposure levels, is easily achieved because of the non-volatile nature of the MRAMs, where the device was programmed and then powered-down during SEE exposure (for cell-level SEE tests only – other SEE tests required power applied). In this way the cell-level results are separated from corruption due to SEFIs in SEE data.

The DUTs did, however, show a device-wide SEFI that resulted in loss of most, if not all, of the programmed data. Because all of the data are lost, it is inferred that this SEFI is not located in the cell array, because smaller sub-blocks of the cell array would be expected to exhibit this behavior independently. Instead, because the entire device is affected, this SEFI is most likely due to a device-wide control error. We also observed that under certain circumstances, this behavior could be caused by manipulating device pins only (with no radiation present), further suggesting the SEFI is a device-controller behavior.

Because of the device-wide SEFI, we are somewhat limited in establishing cell-array SEFI sensitivity, however the results do not show an obvious problem with cell-array-level SEFIs. Ideally, a future test could focus irradiation to regions of a DUT that contain only cell-arrays and limited risk of causing device-wide SEFIs. Such a test could show whether the cell-arrays have other SEFI risks below visibility in this dataset.

The collected MRAM radiation data indicates that the actual MRAM cells and memory array are hard against SEE and TID. This was not unexpected. There were, however,

general concerns for an increase in radiation sensitivity as the memory arrays are scaled to higher densities. At this time, however, the biased SEE SEFI sensitivity is problematic and we are looking for ways to isolate the memory-array macros in the device in order to perform biased testing that does not include potential device-level SEFI sensitivity.

One limitation of the MRAM TID data is that it was collected with the DUTs unbiased. This significantly reduces the potential damage to the support circuitry. While we expected that TID damage to readout circuitry would accumulate quickly with biased TID and limit cell-level TID data collection, it is also possible that memory-array circuitry that cannot be removed may also have significant biased-TID sensitivity. Because of this, the biased TID performance is also a risk that should be evaluated in future work.

B. DRAMs

The DRAM test results showed that the cells have relatively good SEE performance, with a per bit cross section of around 1×10^{-14} cm² at low LET (below 5 MeV-cm²/mg), rising to about 1×10^{-10} cm². This is consistent with the expected performance of DRAM cells and indicates no obvious problems with MBUs or localized SEFIs (giving small numbers of errors) because the observed SBUs occurred with only one bit being observed in error during any read transaction (i.e. burst operation).

These devices did, however, show SEFIs, with a relatively low saturation, overwhelming the SBU data at LETs below 10 MeV-cm²/mg, as the device-level cross section for SEFIs and SBUs were both about 1×10^{-5} cm². The SEFIs observed were included the MSEFI variety where communication with the device appears to be lost. This bodes well for the development of a rad hard memory device because MSEFIs are device-wide and are expected to be caused by SEEs in control circuitry that is replaced if an RHBD controller is mated to the cell-array. Smaller SEFIs did occur, however, with a few 100 to a few 1000 errors occurring in the SEFI. These SEFIs may be located in the memory array, and may require care in RHBD controller design to avoid allowing these SEFIs to impact stored data. It is possible that some of these smaller SEFIs are not located in the memory array, and may be ignored in an RHBD product based on these DRAM memory arrays.

Device TID performance showed essentially no change to the operation of the device to 900 kRad(Si), with some stuck bits showing up by about 400 kRad(Si). The stuck bits, however, were highly transitory and appeared to recover so quickly that stuck bits were fully recovered from one TID exposure before the next exposure began. It should be noted, however, that this recovery behavior was not entirely expected and further data collection is recommended to conclusively prove the nature of the stuck bit recovery. It is also recommended to increase the statistical significance of the TID data on the DDR2 test devices by the inclusion of additional test devices.

VI. CONCLUSIONS

We have presented recent data collected on MRAM- and DRAM-memory arrays, with the intent of determining if the

cell-level and memory-array-level technologies might be usefully mated to a radiation-hardened controller.

In this study, we have shown that a STT-type MRAM technology achieves significant TID (>1 MRad[Si] at device-level, and >7 MRad[Si] at the cell-level) and SEE hardness (no lost data when tested unbiased to $>2 \times 10^7/\text{cm}^2$ at LET of 33.7 MeV-cm²/mg for a >10 Mb device) at the memory-array-level with the caveat that device-wide-biased SEFIs (at relatively low cross section) may be a significant risk.

We have also shown that DRAM memory arrays in candidate devices perform very well for TID (>400 kRad[Si]) and SEE (memory-cell performance is in-line with modern DRAM cell performance). SEFI performance of the test devices showed expected sensitivity (cross section on the order of $1 \times 10^{-5} \text{cm}^2$ at higher LETs) indicating that radiation-hardening of controller logic is expected to improve SEFI performance significantly.

The presented results are targeted at evaluating technology types as go/no-go in regards to suitability of these technologies for mating with a radiation-hardened controller. For the intended purpose, the radiation results have been positive and do not indicate any show stoppers.

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