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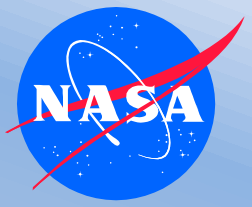

Expanded P2020 SEE Testing – Ethernet, Watchdog, and Static Debugger

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Outline

- Background and Motivation
- Test Setup
- Results
- Discussion/Findings
- Conclusions

Motivation

- Several programs interested in using P2020 processor
- Also used in Space Micro Proton 400k-L computer
- Some discussions of using P2020 include running in configurations where error rates may be very high
  - Need to know about rare events that accompany common events like L1 cache bit errors
- New revision of the die – is the radiation response the same?

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Earlier Testing

- NASA has reported on P2020 in the past
  - Around 2012 NEPP had several reports on P2020 testing – heavy ion, proton, single core, dual core, caches, registers, and crash data
  - In 2014 NASA/JPL as part of MISSE-X work, reported on relative sensitivity of many different algorithms estimated for ISS deployment of a Space Micro P400k-L
    - Found more than 95% of events would be caused by caches
    - Showed that almost all on-chip code sensitivity would be ~1-5% of any space rate, depending on register usage
- Earlier testing was on earlier revision

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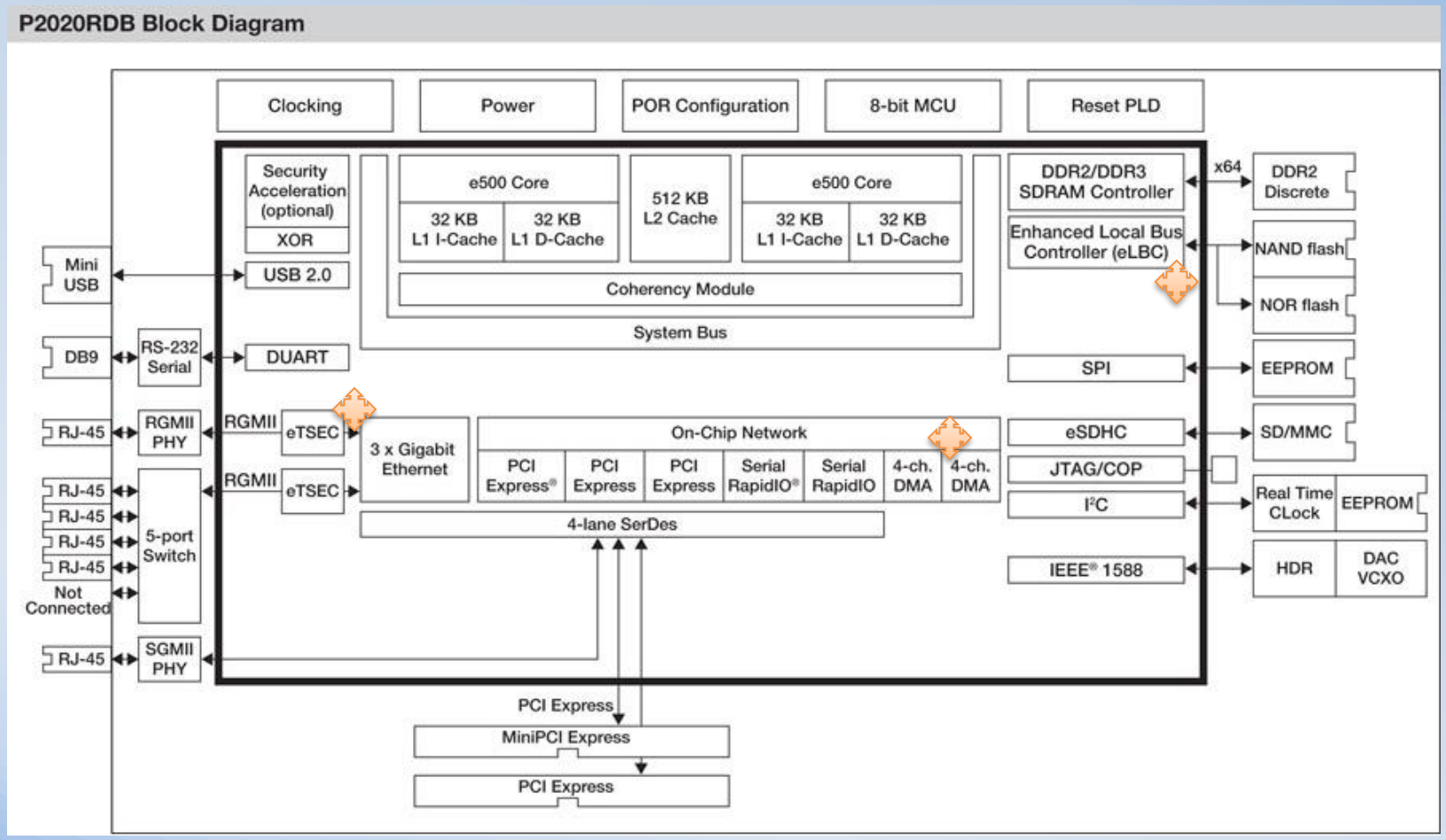
P2020 & RDB



- Many different IP blocks
- Markers indicate new structures tested here

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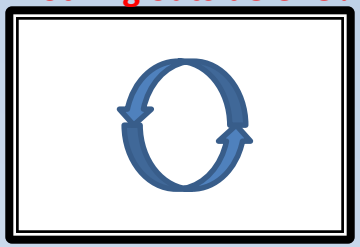
Background: Crashes, Strange, and Rare Events

- Orient the discussion…
- Crashes and hangs are the same here –
  - Code Execution → Stop!
  - If we can figure out what it is doing then its not a crash – so this can be visibility limited



- Strange events are those where the DUT operation is different than expected
  - Not just an SBU or an exception – but rather, incorrect branching, doing the wrong thing
- Rare events are those are simply much less likely to occur than the events usually seen

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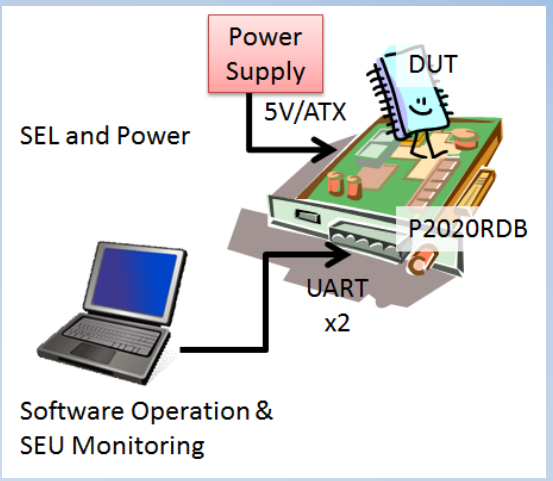
Test Setup: Hardware

- P2020RDB-PCA unit used for testing



- Two serial connections used – 1 for each CPU core
- Utilized U-Boot software to start up the DUTs
- Used power system on board, with power supply from unit - Earlier testing showed no risk of SEL
- Also used BDI3000 debug cable plugged into debug port to allow direct communication
  - Supported on-board flash programming
  - Allowed direct readout of registers

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Testing/Details

- Proton and Heavy Ion Testing
  - TRIUMF 11/2015
  - MGH 12/2015
  - LBL 12/2015 and 5/2016
  - TAMU 5/2016

Board	Energy (MeV)	Proton Exposure
17	100	2.00E+10
44	100	3.30E+10
28	100	1.00E+10
14	100	2.10E+10
32	100	1.80E+10
32	200	9.10E+09

- 5 boards/DUTs tested with protons

- 5 boards/DUTs tested with heavy ions

# Boards	Ion	LET (MeV-cm^2/mg)	Fluence (#/cm^2)
3	Ne	1.1	6.20E+08
3	O	3	3.00E+08
4	Ar	8.2	1.30E+07
3	Kr	24	1.00E+07
2	Kr	28.7	3.00E+06
2	Xe	53	2.30E+05

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Test Software

1) **Register SBU** – SBU in a processor register – also w/ external debugger
2) **Register MBU** – a register completely changes – also w/ debugger
3) **L1 invalidates** – an L1 cache line (with parity protection disabled) is lost
4) **L1 SBU** – this is a reported parity error when parity is enabled
5) **L1 parity invalidations** – parity-protected L1 cache loses valid line of data
6) **L2 SBU** – a SBU observed in L2 data (L2 tested w/ EDAC disabled)
7) **External memory errors** – not reported here
8) **Watchdog** – monitor the watchdog system for correct operation
9) **Ethernet packet error** – test for DUT packets received or transmitted
10) **Flash Memory** – errors reading or writing flash memory w/ external debug tools

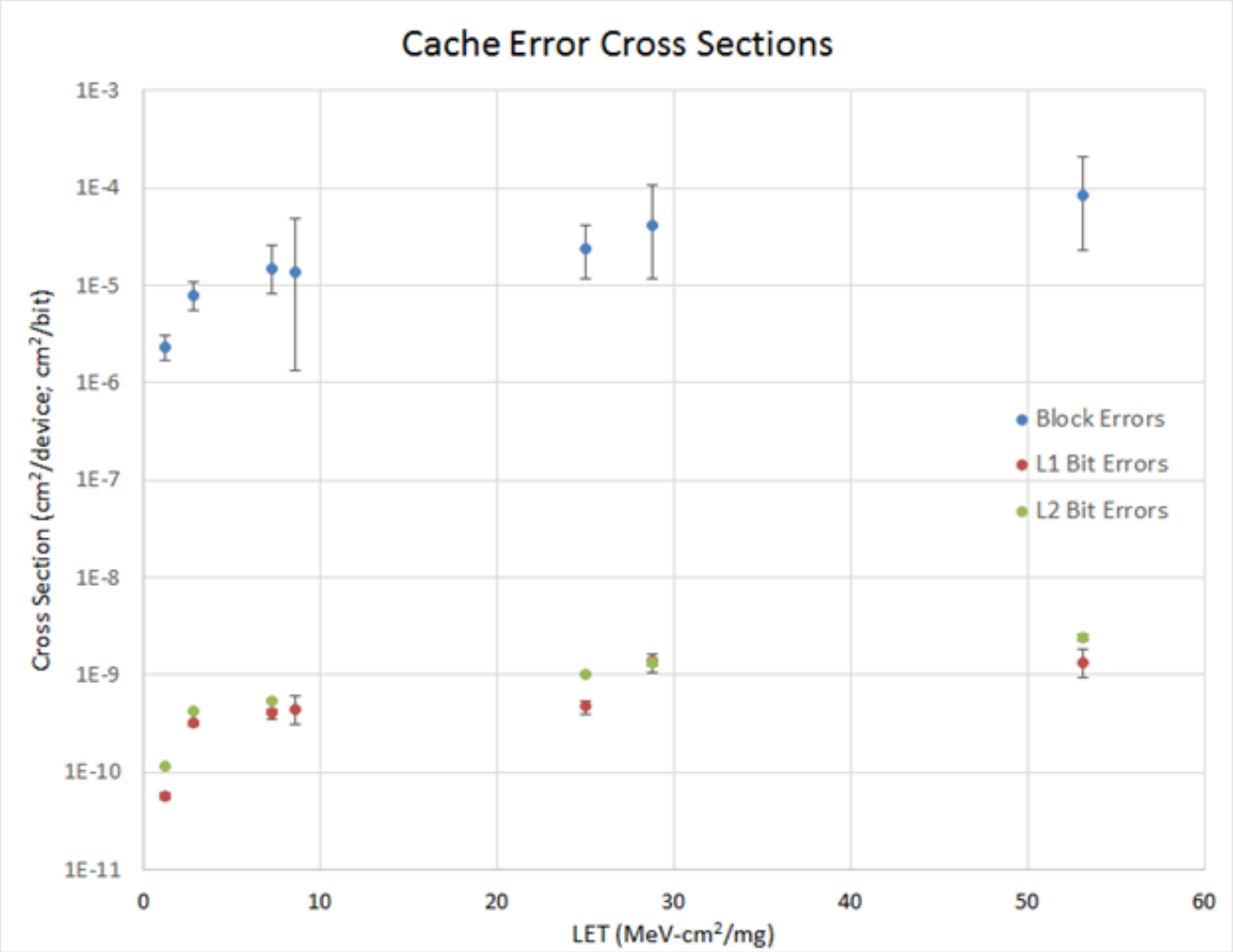
Results: Cache Errors

L1 Errors will cause app/OS crash unless in "write-through"

Bit errors are per-bit.

L1 bit errors are about 10x worse than block errors - 5×10^5 bits
- L2 is 100x worse

L2 block errors not tested but bit errors are EDAC-protected



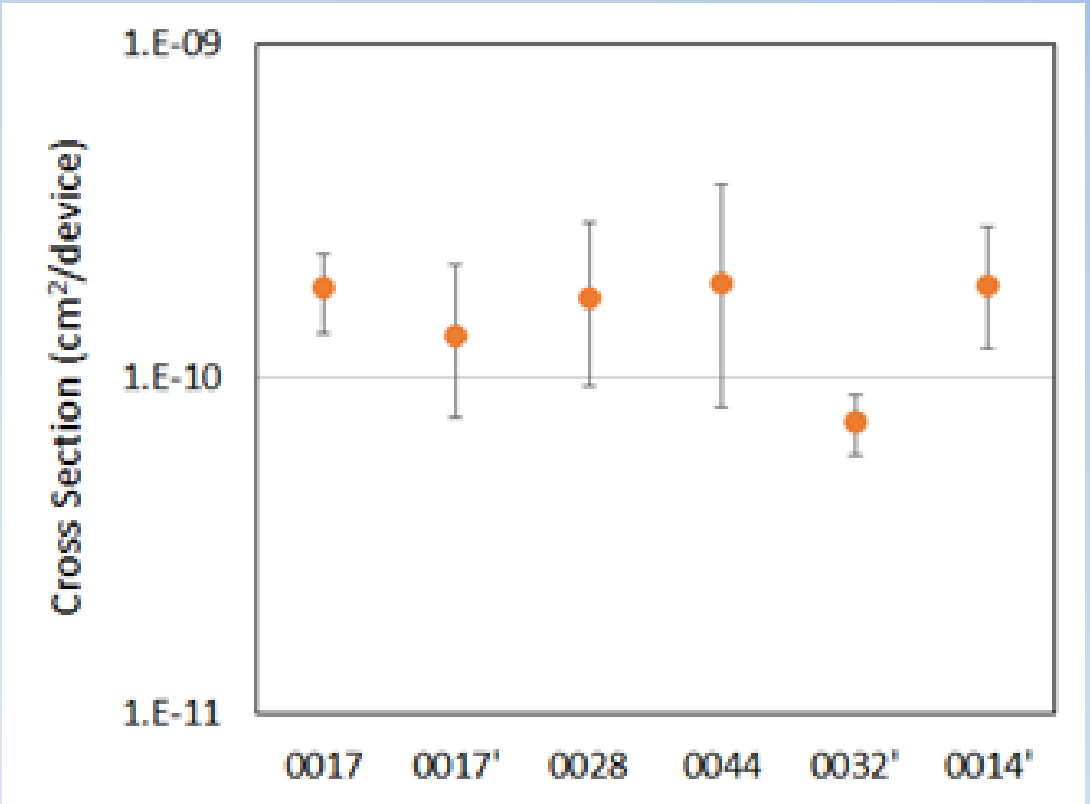
Register sensitivity (per bit) is similar to L1 & L2 cache bit sensitivity…

Proton Cache Errors

Block errors also occurred with proton exposures

Shows consistency across board-to-board results

These errors would be silent even with parity protection.



Block errors with 100 MeV protons across 5 DUTs and two test facilities.

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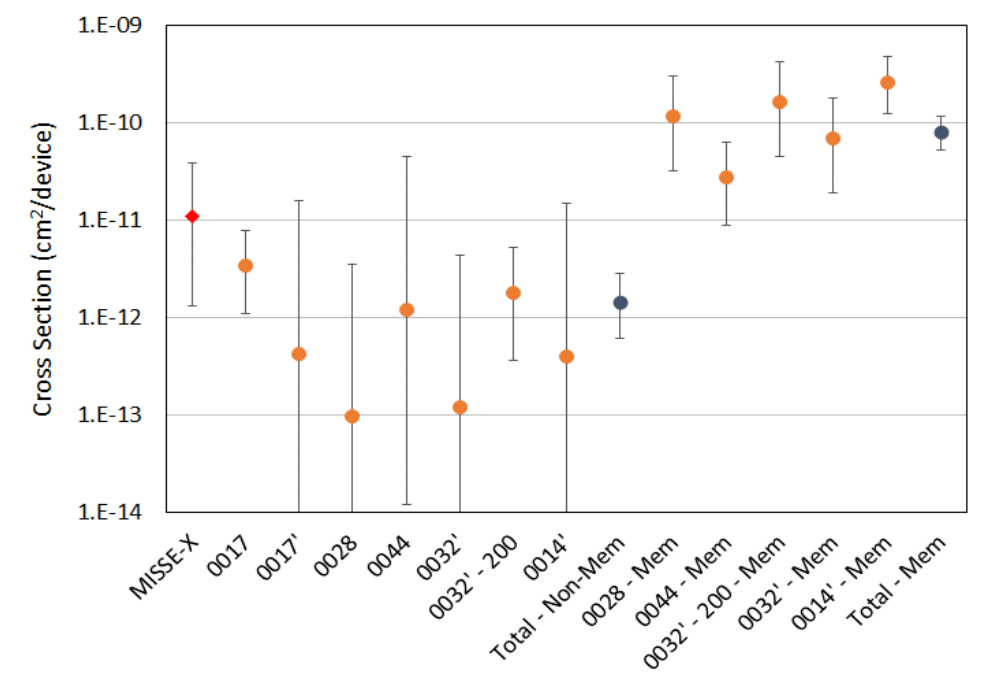
Results: Registers and Debug…



Proton crash sensitivity – many parts/conditions

- Consistent with older tests
- Highlights that when using the memory system, crash rate increases significantly

- Strange Events…
  - Bit error in test control register
  - Latent error cause readout problem after run was over
  - Bit error in test compare register caused runaway error reports
  - CPU showed delay and eventually recovered (though possibly slower than before)

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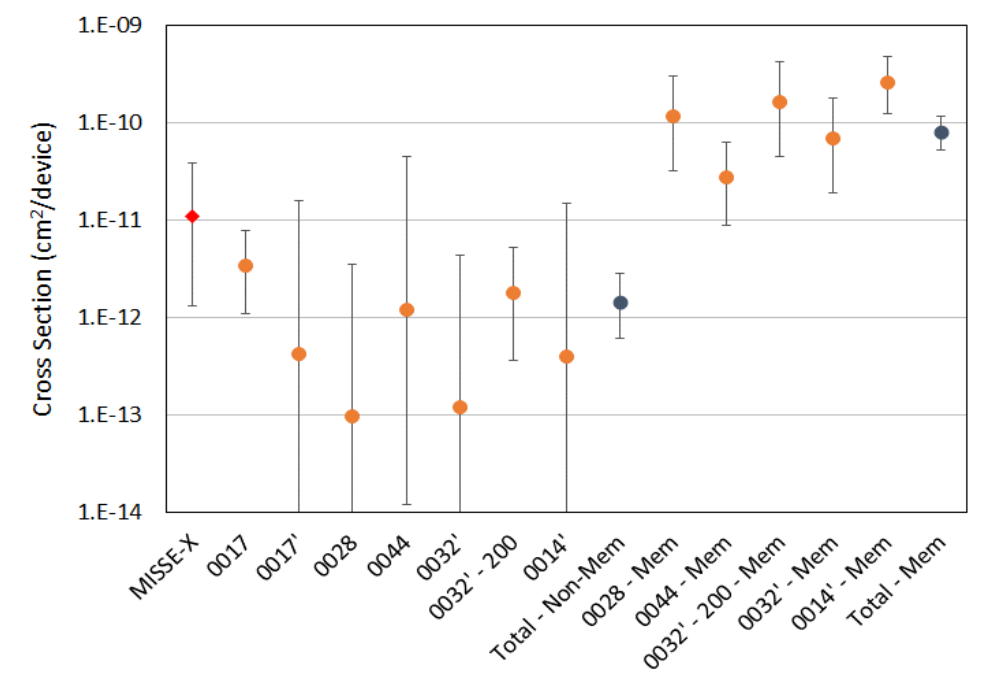
Results: Crashes & Strange Events



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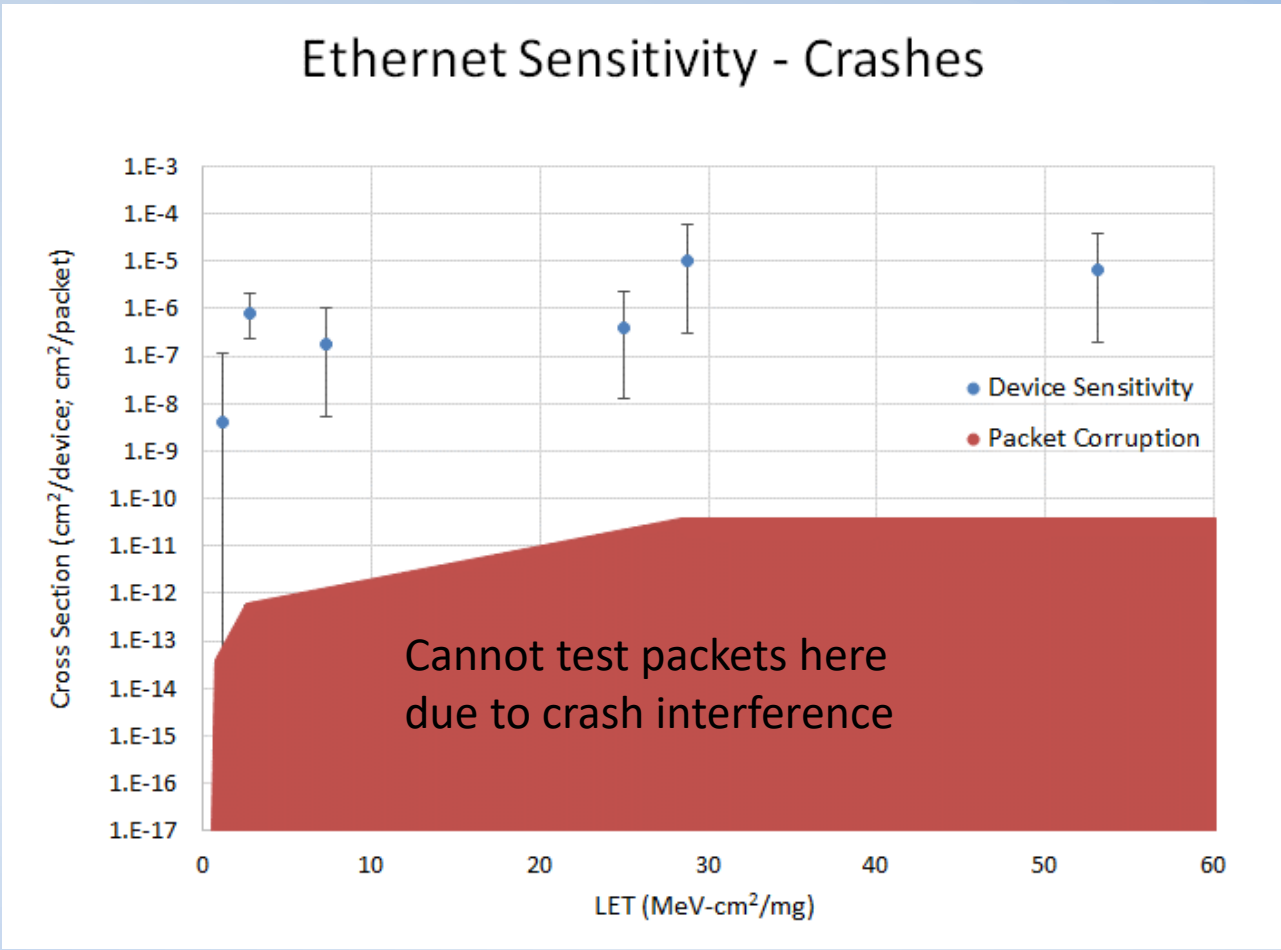
To be presented by Steven M. Guertin at NEPP ETW, June 14, 2016.

Results: Ethernet Testing

- No corrupt packets observed
  - 768-byte payload
  - 44 Mbps rate
- While testing for packet corruption, sensitivity limited by device crashes
  - unrelated to Enet
- Packet loss about the same in/out of beam ~ 0.01-0.1%



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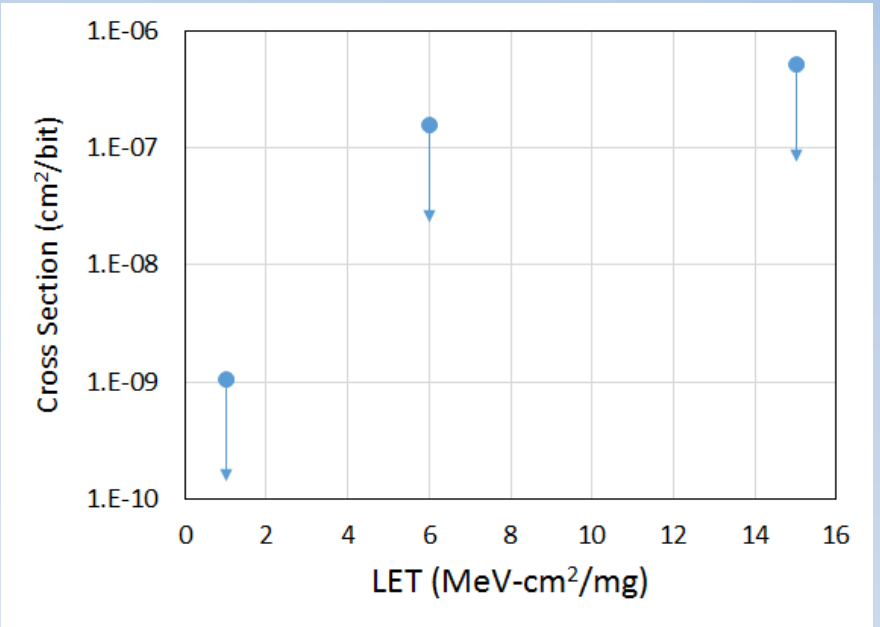
Results: Flash Memory

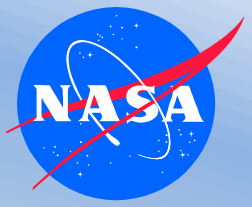
- Debugger was able to read and write during exposure
- Tested with the system suspended, just to check how the Flash interaction circuits responded
- Debugger connects through the processor flash memory interface (not directly to the Flash)
- Did not see evidence of any errors written or read from the Flash memory in any testing



Limiting cross section for Flash memory errors during heavy ion testing

Results: Watchdog

- Monitored for correct change of states in the watchdog system
  - Has multiple states it can get into – with different types of exceptions that are called
- Tested for various LETs
- No indication, in all testing, of any error in watchdog system except:
  - Some indication of register errors changing timeframes for watchdog behavior
  - But the event rate was consistent with register upsets, not indicative of true watchdog sensitivity
- Highlights same problem as Ethernet – data limited by more common event types



Discussion - Findings

- L1 cache bit errors lead the error rates, with cache line/block errors in second place
  - Even with parity protection (which only causes thread termination), block errors occur about 10% the rate of parity exceptions
- None of the other tested event types yielded measurable error rates
  - Watchdog, Flash, and Ethernet tests failed to show any real errors during testing
- Strange events and crashes are next.
  - Crashes do not give incorrect actions
  - Strange events result in incorrect actions
  - Both are on the order of the sensitivity of the registers

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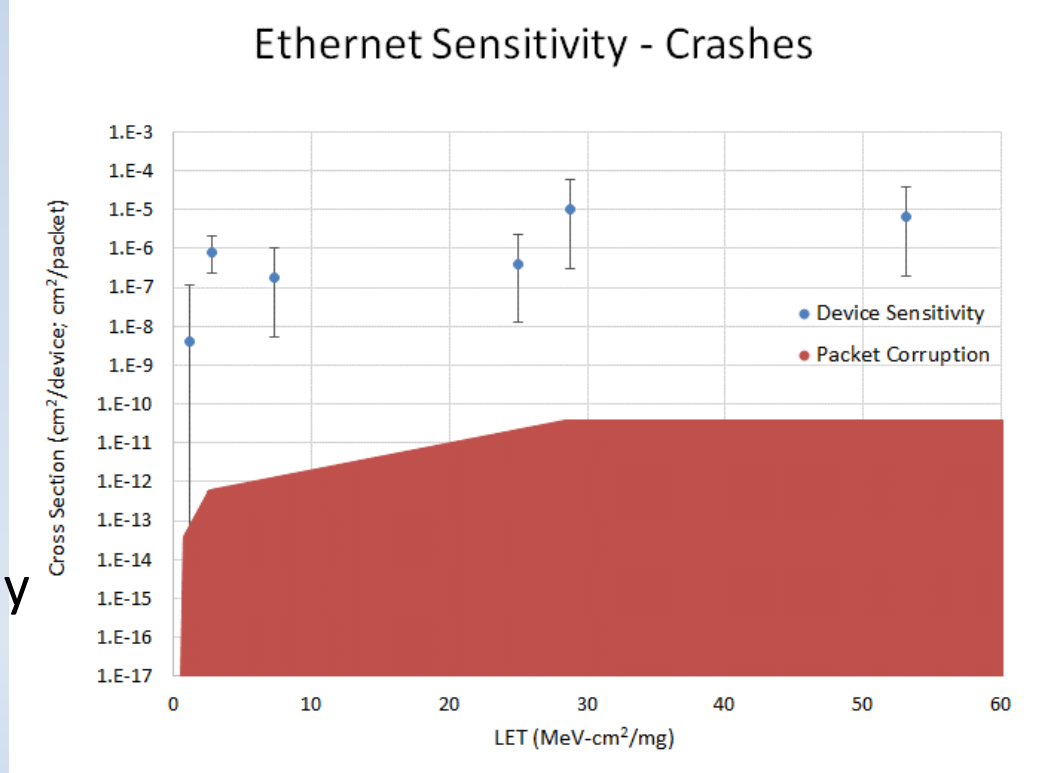
Discussion: Rare Events

- By definition, these are rare compared to other event types
- Ethernet is a great example – how often might you actually get undetected, corrupt data?
  - Compared to dropped packets, corrupt packets that fail consistency checks, dropped connections
- In this case it was relatively easy to test, because we had a lot of expertise already
- But what about other processor types?



Conclusion

- Improved/Expanded P2020 dataset
  - Extended to recent die revision
  - Increased test samples
  - Tested with protons and heavy ions
  - New test targets, updated test methods
  - All duplicate data consistent with old results

- Results on New Targets
  - L1 parity protect found to no eliminate loss of cache lines (this is the most likely error mode for these devices deployed)
  - No significant issues from Watchdog, Flash Memory, or Ethernet testing
  - Showed that static (debugger) test results same as when testing with in-situ code