Hermetic and Non-Hermetic QML Space ICs – Status and Challenges

CMSE 2017
Components for Military and Space Electronics

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Curiosity Rover Finds and Examines a Meteorite on Mars
The dark, smooth-surfaced rock at the center of this Oct. 30, 2016, image from the Mast Camera (Mastcam) on NASA's Curiosity Mars rover was examined with laser pulses and confirmed to be an iron-nickel meteorite.)

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Contents

- **Parts Standards - NASA's NEPAG Program**
  - What is NEPAG
  - How we interact with the user community, manufacturers and others
  - Process to resolve major issues
- **QML Space ICs**
  - Hermetic (Class V)
  - Ceramic based vented packages (Class Y)
- **Concluding Remarks**

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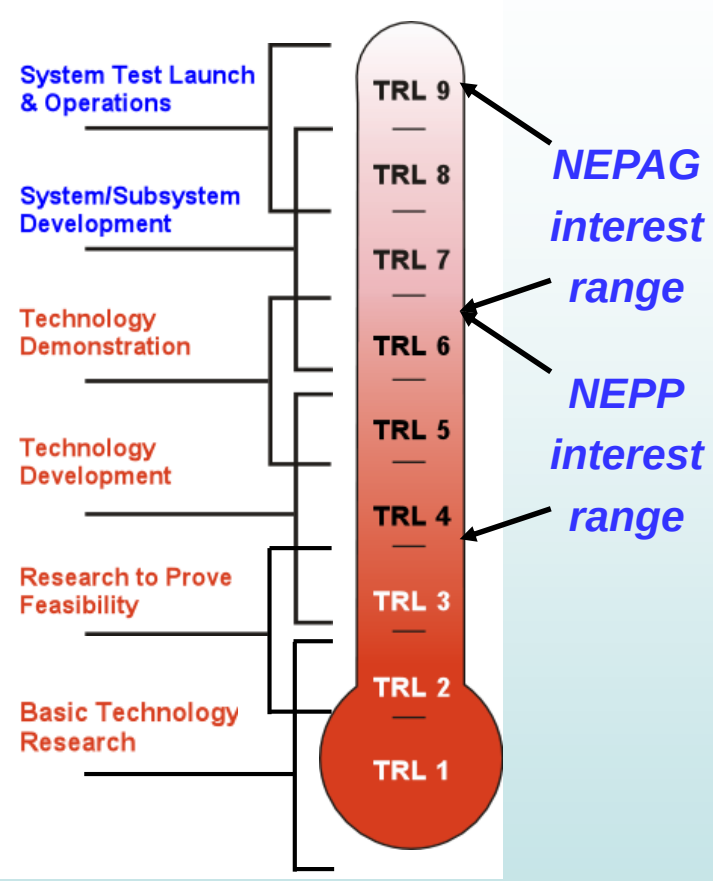
NEPP/NEPAG Focus

- NEPP = NASA Electronic Parts and Packaging Program
- NEPAG = NASA Electronic Parts Assurance Group
- Funded by NASA Office of Safety and Mission Assurance (OSMA)
  - Co-managed by Mike Sampson and Ken LaBel
  - JPL funding comes through 5X Assurance Technology Program Office (ATPO) managed by Doug Sheldon



NASA Technology Readiness Levels (TRLs)

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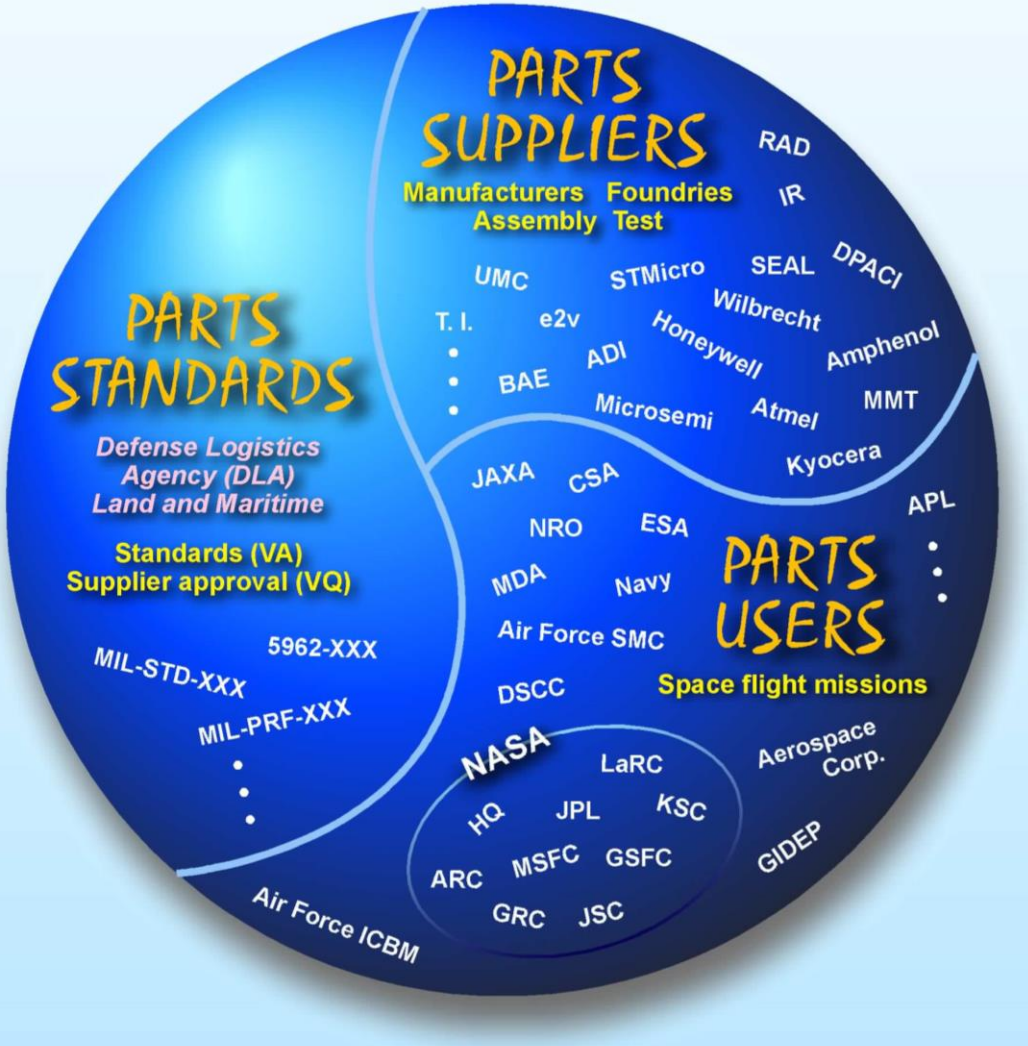
NEPAG Activities

- **Weekly Telecons**
  - A forum for effective exchange of information on electronic parts used on flight projects across NASA (OneNASA) and the space parts community (OneSpace). In its 17th year of operation, NEPAG is comprised of 25 organizations including 7 NASA centers, JPL and 3 international partners from Europe, Japan, and Canada (ESA, JAXA, CSA, respectively).
  - These telecons drive the NEPAG program:

- **Support to Defense Logistics Agency (DLA) – Audits, SMD Reviews**
  - The Defense Logistics Agency (DLA), the Aerospace Corporation and NASA form the space microcircuits qualifying activity (QA). Therefore, NASA is actively involved in the audits and standards activities.
  - Audits: VQ is the audits branch of DLA. NASA supports about 25% of the audits DLA does. We lead audit teams in areas such as burn-in and electrical test program reviews.
  - Standard Microcircuit Drawings (SMDs): VA is the standards/documentation branch of DLA. We review SMDs for new space products. The SMD program is going strong with about 18–20 new space SMDs created every year.

Space Parts World

Develop/Maintain Standards for Space Electronic Parts



The parts users and standards organizations work with suppliers to ensure availability of standard parts for NASA, DoD and others. **For Space microcircuits, DLA, NASA/JPL (S. Agarwal) and the U.S. Air Force / Aerospace Corp. (L. Harzstark) form the Qualifying Activity (QA).**

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A Changing Landscape (Shipping/Handling/ESD Challenge)

A New Trend – Supply Chain Management
Ensuring gap-free alignment for each qualified product
(All entities in the supply chain must be certified/approved)

Manufacturer A	Die design
Manufacturer B	Fabrication
Manufacturer C	Wafer bumping
Manufacturer D	Package design and package manufacturing
Manufacturer E	Assembly
Manufacturer F	Column attach and solderability
Manufacturer G	Screening, electrical and package tests
Manufacturer H	Radiation testing

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An Example of SMD Boiler-Plate Update

TABLE IIA. Electrical test requirements.

Line Number	Test requirements	Subgroups (in accordance with MIL-PRF-38535, table III)	
		Device class Q	Device class V
1	Interim electrical parameters (see 4.2)	1,2,3,7,8A, 8B,9,10,11 1/	1,2,3,7,8A, 8B,9,10,11 1/
2	Static burn-in I and II (method 1015)	Not required	Required
3	Same as line 1	- - -	1, 7 Δ 1/ 2/
4	Dynamic burn-in (method 1015)	Required	Required
5	Same as line 1	1, 7 Δ 1/ 2/	1, 7 Δ 1/ 2/
6	Final electrical parameters	1,2,3,7,8A,8B,9, 10,11 1/	1,2,3,7,8A,8B,9, 10,11 1/
7	Group A test requirements 3/	1,2,3,4,7,8A,8B,9,10 ,11 4/	1,2,3,4,7,8A,8B,9, 10,11 4/
8	Group C end-point electrical parameters 3/	1,2,3,7,8A,8B, 9,10,11 Δ 2/	1,2,3,7,8A,8B, 9,10,11 Δ 2/
9	Group D end-point electrical parameters 5/	2,3,8A,8B	2,3,8A,8B
10	Group E end-point electrical parameters 3/	1,7,9	1,7,9
11	Column attach 6/	1,7,9	1,7,9

- **For Flip-chip column attach**
  - Add room temperature electricals (subgroups 1, 7, 9) after column attach – step 11 above

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Partnering with Industry Groups, NASA Centers, Space Agencies

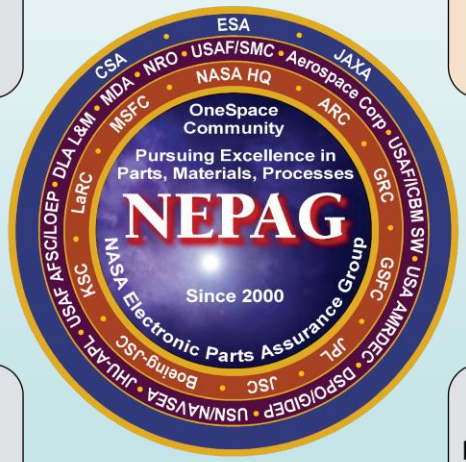
JEDEC JC-13
(Manufacturers)

JC-13	Solid State Devices for Government Products
JC-13.1	Discrete Semiconductors for Government Products
JC-13.2	Microelectronics for Government Products
JC-13.4	Radiation Hardness
JC-13.5	Hybrids and MCMs for Government Products
JC-13.7	New Electronic Device Insertion for Government Products

Joint meeting held
3 times a year

SSTC G-11/G-12
(Industry Users, Primes, Subs)

SAE SSTC G-11	Users of Passive Components
SAE SSTC G-12	Users of Solid State Devices
	G-12 Management: **Chair – A. Touw** **Vice Chair – S. Agarwal**
SAE SSTC G-11 & G-12	Space Subcommittee Chair – S. Agarwal



NASA Centers:

ARC
GRC
GSFC
JPL
JSC
KSC
LaRC
MSFC

Weekly Telecons

Partners from Outside NASA:

U.S. Air Force, U.S. Navy,
U.S. Army, DLA,
The Aerospace Corp,
JHU/APL, ESA, JAXA, CSA

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JEDEC/G-11/G-12 Grid (January 2017)

San Antonio, TX

FINAL
Meeting Schedule

NEPAG MTG.

January 2017

Day	Room	7:30 AM	8:00 AM	9:00 AM	10:00 AM	11:00 AM	12:00 PM	1:00 PM	2:00 PM	3:00 PM	4:00 PM	5:00 PM	6 PM	7PM
Mon 1/9	Regency East 1-3 (Ballroom Level)							G-12 Derating/ Wear-out and Profiles	G-12 Terrestrial & Avionics Subcommittee	G-12 PEM TG Qual and Screening Flow	G-12 Plastics / PEMS Subcommittee	ESD EP Study	**	
	Chula Vista (Lobby Level)							MIL-PRF-19500R		JC-13.1 should attend PEMs Screening flow	JC-13.1 Technical 750 Test Method Review			
	Live Oak (Hill Country Level)						JC-13 ExCo Mtg. (by invitation) *	JC-13.5 TG 175 - PI / QML Task Group						
Day		7:30 AM	8:00 AM	9:00 AM	10:00 AM	11:00 AM	12:00 PM	1:00 PM	2:00 PM	3:00 PM	4:00 PM	5:00 PM	6 PM	7PM
Tues 1/10	Regency East 1-3 (Ballroom Level)	New Member Orientation	JC-13.1/JC-13.7/G-12 New Technology Appendix in 19500	JC-13.1 GaN Working Group	JC-13.1/JC-13.7/G-12 SiC Tech Insertion	JC-13.7 >2D Packaging		JC-13/G-12 Joint Meeting	JC-13.7 Copper Wire Bonds	JC-13.2 Elec Parameters & B/I Stand.	JC-13 X-Ray Seal Voids	JC-13 Leak Rate Issues in 883 and 750	G-12 & G-11 Counterfeit Mitigation Subcommittee	
	Pecan (Hill Country Level)				JC-13.2 JEP121	JC-13.1 should attend >2D Packaging				JC-13.1 MIL-PRF-19500 Appendix J		JC-13.1 should attend leak rate		
	Chula Vista (Lobby Level)		JC-13.5 TG158 - Element Evaluation		MIL-STD-883 Inspection and Interpretation	JC-13.5 TG 172 QML Reqs.				TM2017 End termination inspection				
	Live Oak (Hill Country Level)		JC-13.4 Subcommittee Meeting						JC-13.4 Extended Session					
Day		7:30 AM	8:00 AM	9:00 AM	10:00 AM	11:00 AM	12:00 PM	1:00 PM	2:00 PM	3:00 PM	4:00 PM	5:00 PM	6PM	7PM
Wed 1/11	Regency East 1-3 (Ballroom Level)		G-12 & G-11 1580 DPA Revisions	Joint JC-13.2/G-12 Meeting		Joint JC-13.1/G-12 Meeting		Joint JC-13.7/G-12 New Electronic Device		Joint JC-13.5/G-12 Meeting		G-12 & G-11 Space Subcommittee		
	Chula Vista (Lobby Level)		JC-13.5 Meeting					JC-13.5 Meeting		Chaired by NASA				
	Pecan (Hill Country Level)		Joint JC-13.1/JC-13.4 Meeting		G-12 Radiation RHA Subcommittee			G-12 Radiation RHA Subcommittee						
	Live Oak (Hill Country Level)		G-11 should go to 1580	G-11 Committee Meeting				G-11 Commmittee Meeting					Reception - Lori's Retirement - CASH BAR - ALL INVITED!	
Day	Room	7:30 AM	8:00 AM	9:00 AM	10:00 AM	11:00 AM	12:00 PM	1:00 PM	2:00 PM	3:00 PM	4:00 PM	5:00 PM	6PM	7PM
Thurs 1/12	Regency East 1-3 (Ballroom Level)		JC-13 General Session		Tech Talk: How Does Automotive Achieve and Validate High Quality and Reliability?	JC-13 ExCo Meeting (by invitation) *								
	Chula Vista (Lobby Level)		G-11 Committee Meeting											

* Attended by NASA; NASA is G-12 Vice Chair.

** Effort to update and harmonize ESD standards; A new JC-13 Task Group on ESD has been formed.

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NEPAG and JEDEC/G-11/G-12

- **January 2017 Meeting**
  - Held NEPAG@JEDEC
  - Attended executive committee meetings
  - Chaired Space subcommittee meeting
  - Responsible for G-12 meeting notes (Roger)
  - Co-lead task group on burn-in (Shri)
  - Meetings with manufacturers
    - Including State of the Art (SotA)
  - Meetings with OEMs
  - Provide Class Y status report
  - ESD related Support (Shri)
    - DLA Engineering Practice (EP) Study on electrostatic discharge (ESD)
    - New JC-13 task group on ESD
  - Active participation (Shri, Leif, Jennifer, John, Dale)
    - JC-13.2 (monolithic microcircuits)
    - JC-13.4 (radiation)
    - G-11 (passives)
    - G-12 (actives)

- **Telecons**
  - Plastic encapsulated microcircuits (PEMs) for Space
  - PEMs for Terrestrials/ Avionics
  - JESD 625B and ESDA 20.20 Harmonization

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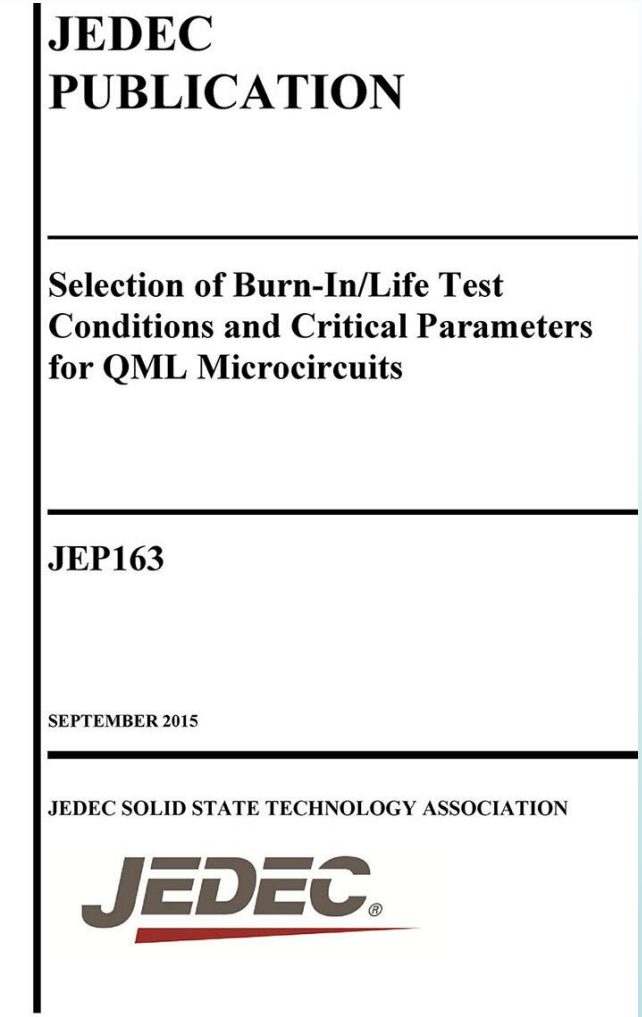
Example of Updated Requirements, Microcircuits Burn-in (BI)
(NASA Inputs 12 September 2016)

- **Status**
  - Task Group until recently was chaired by B. Rhoton. Taken over by N. Shindler going forward.
  - Published Guideline document JEP163.
  - DLA's Engineering Practice (EP) study on BI is complete.
  - Task group is still open to address new concerns

- **A New Concern**
  - BI of high-speed devices (frequencies approaching gigahertz range)
    - What about hot spots on the die? For example, Serializer/Deserializer (SERDES) in a field-programmable gate array (FPGA) may run much hotter than the rest of the die.
      - Practically no data on hot spots (no verification of models)
    - Ambient vs. case vs. junction temperature


JEDEC PUBLICATION

Selection of Burn-In/Life Test Conditions and Critical Parameters for QML Microcircuits

JEP163

SEPTEMBER 2015

JEDEC SOLID STATE TECHNOLOGY ASSOCIATION

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Other JEDEC/G11/G12 Major Activities Supported by NASA

- Leak rate and residual gas analysis (RGA)
- New technology insertion (>2D packaging)
- GaN, SiC Working Groups
- Hybrid element evaluation
- Passives
- Radiation hardness
- Plastic encapsulated microcircuit (PEM) screening and qual flows
- Copper bond wires qualification, testing

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NASA Electrostatic Discharge (ESD) Surveys of Manufacturers

- **Microcircuits:**
  - Candidate companies for NASA ESD survey are identified during the DLA audit.
  - This is an independent survey by NASA--Not a part of the DLA audit process.
  - The purpose of the survey is to better prepare smaller manufacturers with plans to develop space products.
  - The findings of the survey are non-binding.
  - There has been good feedback from companies that went through it.

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Electrostatic Discharge

- NASA EEE Parts Bulletin (January – July 2016)

National Aeronautics and Space Administration

EEE Parts Bulletin

Electrical, Electronic, and Electromechanical

A periodic newsletter of the JPL/OSMS Assurance Technology Program Office (ATPO), NASA EEE Parts Assurance Group (NEPAG), and Section 514, of the Jet Propulsion Laboratory.

January–July, 2016 · Volume 8, Issue 1, Revision A, January 26, 2017
Special Edition on Electrostatic Discharge (ESD)
(The NASA *EEE Parts Bulletin* has been published since 2009)

Note: This revision adds a number of details and corrects ambiguities in the original issue that was released August 31, 2016 (the K. LaBel article on partnering and the back-page material were not changed).

Damage from ESD is a major cost to the microcircuit industry in terms of time, money, and mission risk. We plan to release two issues. This first special issue deals with the need to upgrade specifications related to ESD and suggestions for better ESD practices wherever parts are manufactured, stored, or prepared for shipment. This issue also includes an article about partnering in radiation and reliability testing. The second special issue will describe examples of ESD-related problems. Figure 1 is an example of damage caused by ESD.

(a) (b)

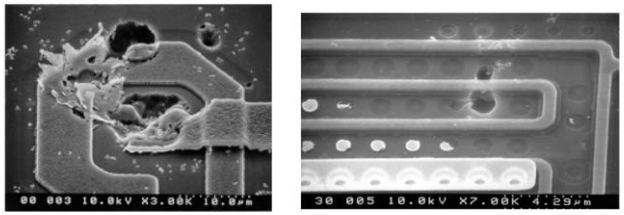

Figure 1. Examples of ESD damage to microcircuits (Images courtesy of JPL Analysis and Test Laboratory):
a) A static random access memory (SRAM) device with 5-micron features was deliberately exposed to an 8000-volt pulse from a 100-picofarad capacitor. This produced an approximately 5.3-ampere peak current pulse lasting just under one microsecond. Melting of conductive traces is typical of such ESD damage and creates an open circuit path.
b) An undefined microcircuit with 1-micron line widths that failed in service after being exposed to a pulse of approximately 500 volts. This caused a breakdown of the SiO_2 layer and a short circuit in the part.

Upgrading ESD Control: Its Importance and Possible Strategies

A. What Is ESD and How Are ESD Controls Applied?

Electrostatic discharge or ESD in electronic parts is an electrical sparking event that functions like a tiny version of lightning. When two objects with different potentials are brought sufficiently close, a current flows toward the ground equalizing the potential. These differences can be caused by friction of dissimilar materials (shoes on a carpet is a classic example), but even the difference in potential between a human body and an object may be enough to initiate an ESD event.

For electronic parts, built to carry minute amounts of current, tiny lightning bolts are a cause for concern. If such an errant current flow of an ESD goes along the outer case of a part or the outside of an ESD-resistant (anti-

1

tatic) bag or shipper, there may be no problem. However, such a current goes through the part, serious damage ay result. ESD damage can include catastrophic damge and/or latent damage. Catastrophic damage is immeiately detectable by the resulting loss of function and ofn visible damage. Latent damage is not immediately dectable because there is no loss of function and often no sible sign of damage. However, the part has been weakned and may fail in the field or (worse) in space.

his has always been a serious concern for electronic arts, but it has grown steadily more urgent.

he purpose of this article is to sensitize the entire space ommunity, and in particular, the standards-developingodies to the fact that the ESD requirements must be early specified in such standards documents so that verybody handling microcircuits, from manufacture to fial use can minimize ESD damage. Furthermore, the tandards must be updated to reflect the present level of echnology.

this context, the role of DLA (Defense Logistics gency) for the department of defense (DoD) becomes tal. The standardization branch of DLA develops and aintains the military (MIL) standards, which are used for aintaining high-reliability quality parts production for the oD and for NASA. In addition, manufacturers and nonIL standards organizations provide inputs to the standrds

hese standards are often enforced by periodic audits of arts manufacturers and their supply chains. The audit ranch of DLA officially conducts official enforcement. ASA actively supports DLA in both of these activities.

or the purposes of this article, we are focusing on monlithic microcircuits. The standard most commonly used y the U.S. space community for high-reliability microcirits is MIL-PRF-38535, *Integrated Circuits (Microcirits) Manufacturing, General Specification for*. Any mirocircuit parts produced under the military system must e in compliance with the requirements of this document.

he 38535 is the periodically changing overall document ontrolling microcircuit quality and reliability. The ESD asects of the document clearly need updating. For auditg, the requirements must be flowed down to the working udit, and it must be reflected in each manufacturer's uality management (QM) plan.

addition, the ESD-related standards used by other oranizations may provide ideas for upgrades to the MIL tandards. Conversely, it would be highly beneficial if the IL standard upgrades could be coordinated with those f the other standards bodies so that practices throughout e industry might be as similar and interchangeable as ossible.

B. Why Improved ESD Control Practices Are Crucial

Microcircuit densification has increased pin counts significantly in the last decade, particularly for communication and computing products. NASA and the space community are using 1752-pin counts, and higher counts are growing more common in the general market.

Current ESD rating methods were developed with typical pin counts in the twenties. Applying these old device testing standards to modern high-pin count products can cause severe problems. Testing times increase dramatically. Worse, wear caused by repeatedly stressing the same path and the increasing influence of tester parasitic losses (parasitics) can lead to false-positive failures.

The increased capabilities attained by increasing parts density has come at the cost of greater sensitivity to ESD. Thus, it becomes increasingly important to implement better methods of controlling potential damage from ESD. A wide assortment of books and journal papers provides information on methods for mitigating ESD.

For high-reliability microcircuits (where a part may cost as much as tens of thousands of dollars), organizations often develop and enforce required policies and procedures designed to mitigate ESD. These policies and procedures are codified in standards.

Furthermore, the landscape of microcircuit part production, handling, and shipping has changed radically. Because of the increased complexity of parts, the paradigm of a manufacturer shipping directly to a customer has largely given way to a highly dispersed production environment, which in turn, often requires highly dispersed ESD control among a number of organizations. Table 1 shows all the steps at which production or use of a microcircuit might be done by shipping to another facility. (The most extreme cases of maximum dispersion are more likely with new products such as flip chips.) Moreover, each of the steps involves at least one environment each for working on the part, storing the part, and shipping the part to the next step in the production.

Much as increased pin counts increase the susceptibility to ESD, increasing the number of shipping steps in the supply chain increases the number of points where ESD damage may occur.

It is important to recognize and fully address all the risk points to which ESD sensitive parts are subjected: from when they are fabricated and delivered from the original component manufacture's (OCM) site; through supply chain avenues to user inventories; then on to kitting and upper-level printed circuit board (PCB) level assembly, test and verification; and eventually to final box level assembly, test and final system level test. This is particularly important for handling, packaging, and shipping of ESD Class 0A devices (<125 volts in the Human Body Model).

2

- Are all three commonly used ESD models still valid or should the standards focus on one or two models?: Those models are 1) human body model (HBM) based on people accumulating electric charges; 2) charged device model (CDM) based on materials becoming charged after they rub against other materials; and 3) machine model (MM) [designed to simulate a machine discharging through a device to ground].
- Do we want a standard for reducing the number of pin combinations required for testing?
- Would statistical pin testing be a good approach?
- How can the testing time be reduced without losing useful information (and significantly impacting the test data)?
- Should the MIL standards be expanded to include charged device model (CDM) testing?
- How do the new 2.5D and 3D configurations affect ESD testing?

We need to consider future trends when revising test standards. This issue is growing more important because the unit cost of contemporary devices are very high (and are growing costlier as more functionality is added), on the order of several tens of thousands of dollars per unit. Poor ESD environment for such products creates possibility of damage/ latent damage to them, both of which could be very expensive. Costs for implementing an ESD-prevention program are miniscule compared to the overall cost incurred in dealing with ESD damage.

The above concerns were presented by NASA representative Michael Sampson at the June 2016 G12 Space Subcommittee meeting. He proposed that the military documents that control the ESD requirements for testing and rating ESD event severity be reviewed and updated as a first step. As part of this update process, he suggested that Defense Land and Maritime (DLA), which serves as the qualifying authority to maintain the MIL system of parts qualification, perform an engineering practice (EP) study on ESD to detail these issues and compare possible specification changes with those being implemented or proposed by other organizations, in particular the NASA Inter-Agency Working Group related to ESD (NASA IAWG-ESD). Ideally, coordination among the various standards-setting organizations would result in updated ESD standards with a great deal of commonality. DLA shared the results of their EP study at the JEDEC meeting held in January 2017. Based on the EP study and responses to it, JEDEC (JC-13) has opened a task group to resolve issues related to ESD.

These document changes will require review and coordination with associated reference documents from other organizations to bring consistency.

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Issues from Microcircuit / Other Audits and Methods of Resolution

Audits						
Class Y	New Technology Infusion		NASA Parts Bulletin	DLA Engineering Practice (EP) study	G-12 Task Group (TG)	MIL-PRF-38535 Revision K
Burn-in	Varied interpretations of requirements			DLA Engineering Practice (EP) study	JEDEC Task Group (TG)	JEP163. TG still open
Underfill	Difficulties in meeting requirements		NASA Parts Bulletin – Special Edition on Underfills	DLA Engineering Practice (EP) study	JEDEC Task Group	Resolved
ESD	Old/inconsistent requirements (e.g. 3 zaps vs 1 zap per pin)	NASA ESD Surveys	NASA Parts Bulletin – Special ESD Edition	DLA Engineering Practice (EP) study	DLA presented EP results in January 2017	A JEDEC ESD task group formed
Crystal Oscillators	Per manufacturers, practically no sales for QPLS oscillators		NASA Parts Bulletin – in preparation	DLA EP study planned	DLA talk at Space meeting last September	New issue

Process Flow:

*DLA Audits: Major issues uncovered during DLA audits

*NASA Parts Bulletin – Special Edition: Gives subject matter background. Provides results of NASA evaluations, ESD surveys, etc.

*DLA EP Study: A large survey of manufacturers, users, others.

*JEDEC/G11/G12 Meetings: Where discussions are held.

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Microcircuits
Moving with the Times

- **NASA Class Y experience:**
  - NASA-led new technology infusion
    - A new way to conduct business
    - Supplier offered a product of system-on-a-chip (SOC) complexity,
      - Xilinx Virtex-4 and -5 FPGAs (ceramic-based flip-chip non-hermetic construction)
      - Of great interest to hardware designers
    - It represented advances in packaging, smaller feature sizes
      - Flip-chip, CGA. 65nm–90nm feature sizes.
    - But, it didn't fit any of the existing categories
      - So, a new Class Y was introduced
    - It also made us realize that we had reached an unchartered area
      - Somewhere near the boundary of parts and boards
    - Suppliers and space community had considerable discussion on developing requirements for Class Y (some of which would also apply to Class V).
    - Examples of new requirements put in 38535K:
      - Post column attach electricals (screening)
      - Package integrity demonstration test plan (PIDTP) quality conformance inspection (QCI)
    - The concept of doing screening and qualification testing remained intact

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Infusion of New Technology into MIL/Space Standards PIDTP and Its Applicability

- **Issue**
  - How to address the manufacturability, test, quality, and reliability issues unique to new non-traditional assembly/package technologies intended for space applications

- **Solution Proposed**
  - Introduced a new concept called package integrity demonstration test plan (PIDTP)
  - Each manufacturer shall develop a PIDTP that shall be approved by the qualifying activity after consultation with the space community.
    Ref: MIL-PRF-38535K, Para B.3.11.

- **The PIDTP requirement would apply to:**
  - Non-hermetic packages (e.g., Class Y). Ref: 38535K, H.3.4.4.1.1.
  - Flip-chip assembly. Ref: 38535K, H.3.4.4.1.2.
  - Solder terminations. Ref: 38535K, H.3.4.4.1.3.

- **Microcircuits employing more than one of above technologies shall include elements for each in the PIDTP.**

  Ref: 38535K, H.3.4.4.1.

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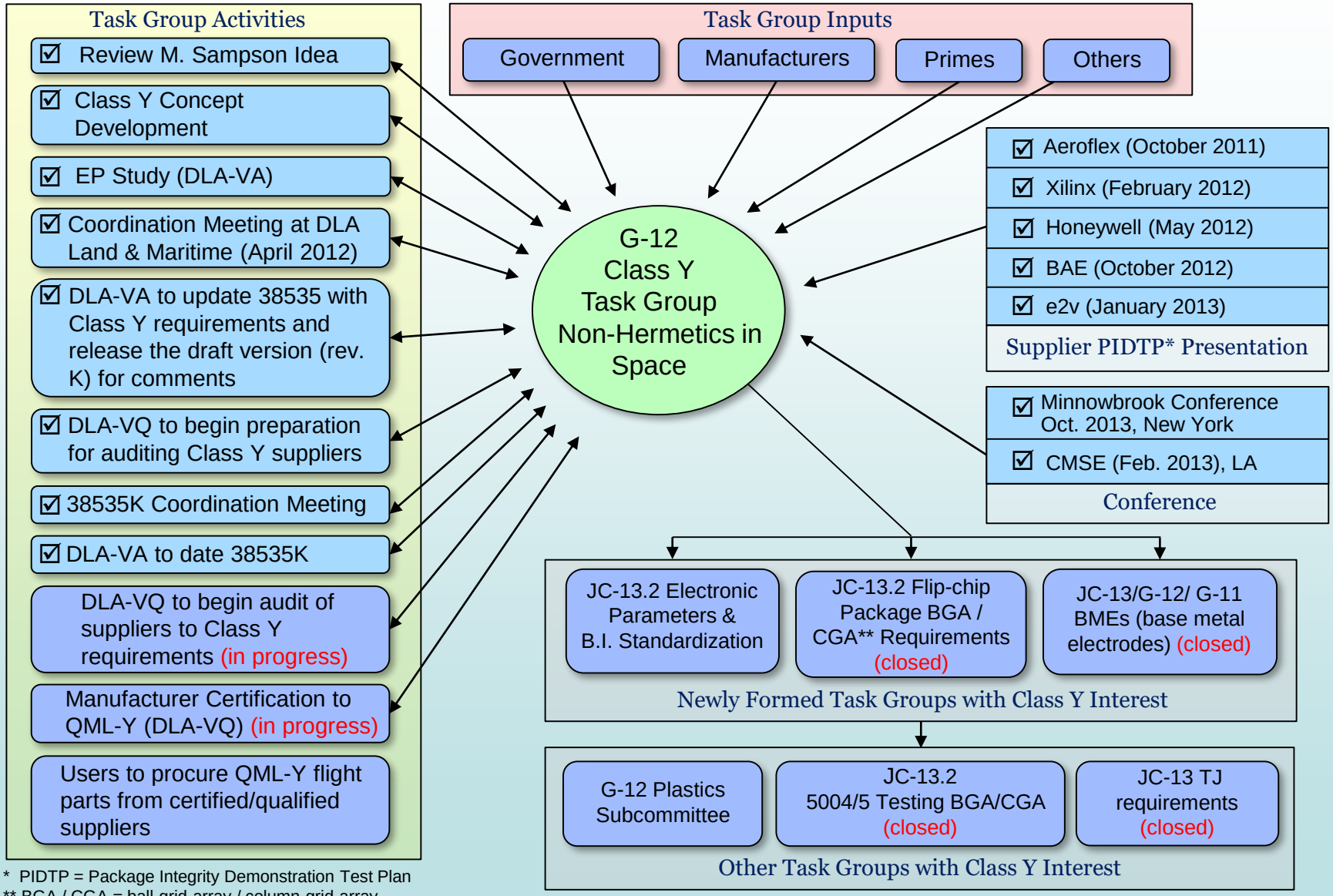
Infusion of the New Class (Y) Technology into the QML System for Space



* PIDTP = Package Integrity Demonstration Test Plan
** BGA / CGA = ball-grid array / column-grid array

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Class Y Qualification / Certification Status

- **Qualified Manufacturers**
  - Honeywell, Plymouth, MN.
- **Certified Column attach service providers**
  - Six Sigma, Milpitas, CA
  - Micross, Crewe, UK
  - BAE Systems, Manassas, VA
  - Honeywell, Plymouth, MN
- **Certified Manufacturers**
  - Cobham, Colorado Springs, CO
- **Certification Planned**
  - Xilinx, San Jose, CA
    - Still **no specs for BME (Base Metal Electrode) IDCs** (Inter-Digitized Capacitors)
  - e2V, Grenoble, France
  - Cypress, San Jose, CA

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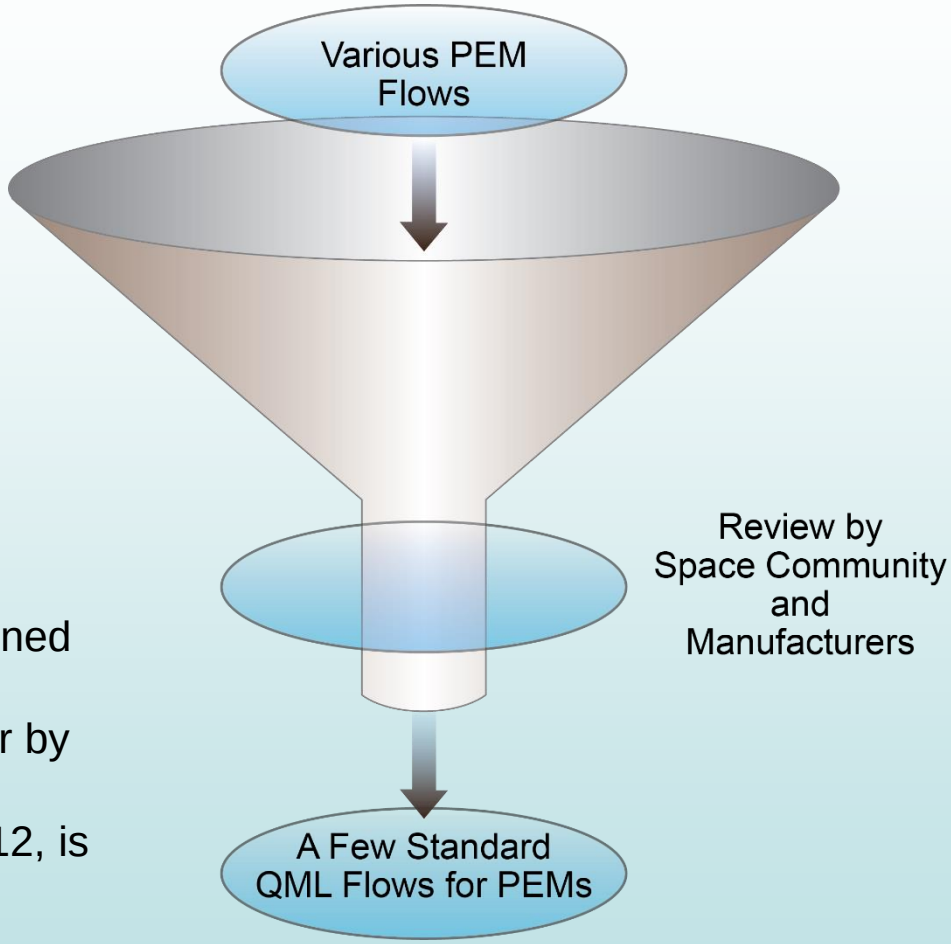
PEMS for Space

- **Working toward Standardized Flows for NASA CubeSats and SmallSats**
  - There are many new NASA flight missions categorized as CubeSats and SmallSats. During the weekly NEPAG telecons, the group has discussed what kind of standard products would fit those applications, including commercial-off-the-shelf (COTS) plastic encapsulated microcircuits (PEMs). NASA is supporting SAE SSTCG12 committee activities with the goal of developing PEM standard flows for avionics, and space applications.
  - At least three parts manufacturers have recognized the need for this newly developing market and are offering customized parts. Cobham Aeroflex has several flows assigned based on extent of testing to assist users in picking the best parts. Similarly, Texas Instruments offers parts in five different versions, including their QML offerings. Linear Technology plans to offer PEM products with guaranteed total dose radiation (rad tolerant, RT) ratings. Also, there is an existing QML N flow for standard non-space PEM devices.
  - These are all good developments. However, it would be cumbersome to manage multiple nonstandard flows. Moreover, some of these approaches may or may not apply to NASA missions depending on acceptable risk levels. The ideal situation would be for the space community and manufacturers to agree on a limited number of standard QML PEM flows to offer solutions for small missions (CubeSats, NanoSats, SmallSats, etc.). In addition, there are DLA's Vendor Item Drawing (VID) program and parts built for automotive applications.
  - All this needs to be discussed.

PEMs for Space

- **Newer Applications**
  - CubeSats
  - SmallSats



Standardizing on a few well-defined flows rather than multiple flows defined by each manufacturer or by each standards group.
SAE AS6294, developed by G-12, is one candidate.

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DLA's VID (Vendor Item Drawing) Program

Vendor Item Drawings

Current Supplier's Program Benefits

1. Single Standardization Document
2. Controlled baseline.
3. Enhanced product change notification of processes, materials, electrical performance, finish, molding compounds and manufacturing locations.
4. Extended temperature performance.
5. Enhanced Pedigree - Reliability and electromigration checks, electrical characterization over temperature and confirmation of package performance over temperature.
6. Enhanced Obsolescence management.
7. No pure tin.
8. No copper wire bonds.

See the attached listing or check our website for an up to date list of product coverage.

DSCC ANNOUNCES THE RELEASE OF A NEW TYPE OF STANDARDIZATION DOCUMENT.

DSCC

DSCC is releasing new Vendor Item Drawings (VIDs) almost daily. These documents have been created to provide a procurement vehicle for enhanced commercial products. Specifically, commercially available microcircuit products are being documented for the first time on a standardization document. Use of these DSCC VIDs will avoid the use of manufacturer generated specification control drawings (SCDs) or manufacturer's VIDs and avoid the potential proliferation of non-standard products. The participating manufacturers have agreed to provide information and services that have not traditionally been associated with commercial products. See our website for a list of documents that are currently available.

All Vendor Item Drawings are ***NOW*** available on the DSCC web site

http://www.dscc.dla.mil/Programs/MilSpec/

- Analog and digital functions offered.

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Evaluation of Automotive Microcircuits

- **Existing automotive parts market**
  - Plastic packages
  - No screening is done
  - Much testing is done at the wafer level
  - Limited qualification
  - The customer must enforce any desired requirements
  - Manufacturers self certify — no DLA-type regulators
  - The system works because of **high-volume production** — That is the customer's power to enforce upgrades

- **Evaluation is in progress at Navy Crane**
  - Screening and qualification are planned
    - Tight budget
    - Qualification will be limited to life test

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Current Status of Hermetic and Non-Hermetic QML Space ICs

- **Classes V and Y**
  - The demand for standard hermetic space products (Class V) continues to stay strong. We review 18–20 new SMD drawings every year, many of which include guarantee for radiation hardness. It shows that despite a push towards COTS to address CubeSats, SmallSats, and other applications, the standard space parts are still pretty much in demand.
  - Development of a new QML Class (such as the Class Y we did for ceramic based non-hermetic microcircuits) takes a fair amount of work.
  - The screening and QCI requirements for Class V and Y are similar except for Class V is hermetic, Class Y is not.
  - In the process of developing requirements for Class Y for Xilinx Virtex FPGAs and other products of similar complexity, system-on-a-chip (SoC) with a large number of columns (1752 for Xilinx), it was realized that we had reached an unchartered area: somewhere near the boundary of parts and subassemblies. Many compromises had to be made, such as room temperature (rather than over temperature) electrical testing post column attach.

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Hermetic and Non-Hermetic QML Space ICs in Near Future

- **Concluding Remarks**
  - The extent of support to flight projects/programs/experiments provided by parts engineers working at NASA would broaden: it would cover a much wider spectrum of parts, from COTS and automotive to traditional standard products.
  - The next generation of parts, 2.5D and 3D, will require considerable work in developing standards.
  - The boundary between monolithic and hybrid microcircuits is going to keep getting fuzzier. At some point we would wonder if it wouldn't make sense to have one performance specification for all microcircuits, including those in 2.5D/3D configurations (combine MIL-PRF-38535 and MIL-PRF-38534)?
  - Higher chip speeds and increasing chip densities will require a shift in the paradigm for electrical testing and burn-in.

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NASA Workshop

- **Workshop**
  - NASA Electronic Technology Workshop (ETW) combined with Small Missions Workshop is held in June every year
    - The next ETW will be June 26-29, 2017
  - Venue: Goddard Space Flight Center, Greenbelt, MD
  - Past papers posted on NEPP Website:
    nepp.nasa.gov
  - See above website for other details

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http://nepp.nasa.gov

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