



Jet Propulsion Laboratory
California Institute of Technology

High Density Packaging Technologies for RF Electronics in Small Spacecraft

Fernando Aguirre (author)
Don Schatzel (co-author)

Jet Propulsion Laboratory
Presented at IEEE Aerospace Conference in Big Sky, Montana
March, 2017



How does Packaging Enable Small Spacecraft?

- Allows for the reduction in electronics modules
- Allows for reducing hardware volume on a limited budget where custom chips cannot be afforded
- Allows for quick turn solutions which many times small spacecraft need

***Typically: Small Spacecraft = Small Budget & Short Schedule
This limits opportunities to use Application Specific Integrated
Circuits (ASICs) and System On Chip (SOC) solutions***



Iris V2 for MarCO

Jet Propulsion Laboratory
California Institute of Technology

Packaging Challenge:

What can we do with packaging to fit what is typically on
> 100 in² of PCB real estate onto < 32 in²

Packaging Response:

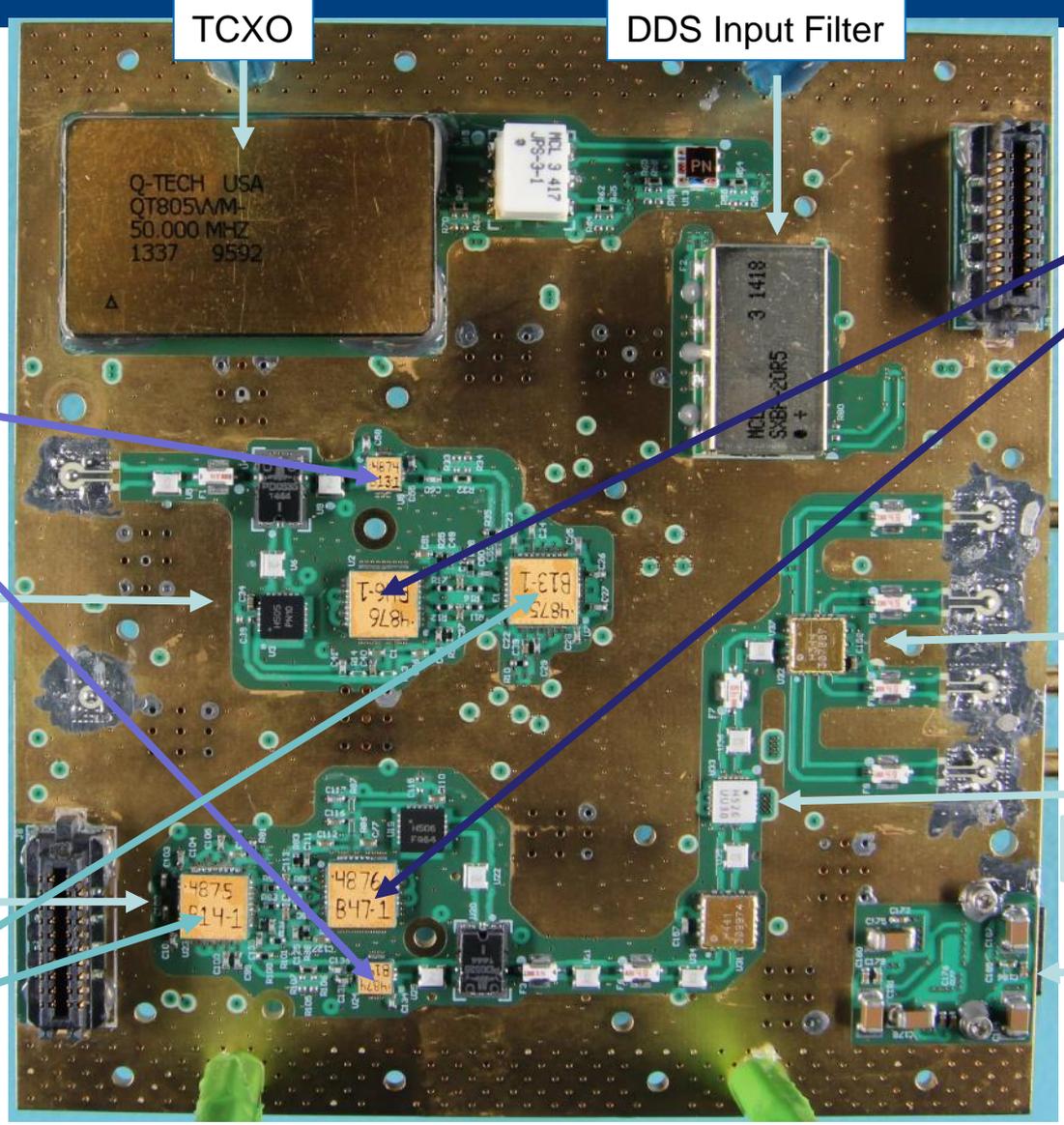
Remove bulky packaging and replace with smaller
Quad Flat No-leads or QFN packages

Note: In terms of RF heterodyne architecture, optimized the exciter with the use of a direct carrier modulator and the receiver with the use of an image reject mixer.

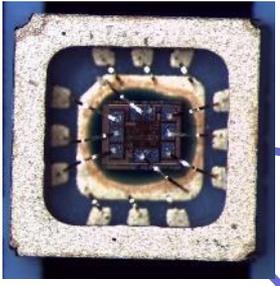


Jet Propulsion Laboratory
California Institute of Technology

Iris V2 Exciter Repackaging

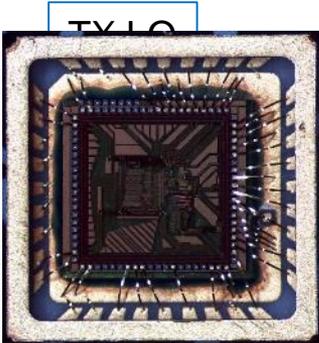


PE9309 pre-scaler
in custom 3mm
QFN package to
save real estate

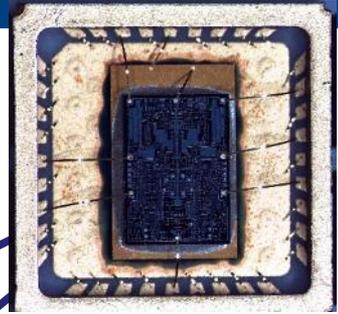


RX LO

PE97632 PLL in
custom 6mm
QFN package to
save real estate



DDS Input Filter



RH1498
opamp in
custom 6mm
QFN package
to save real
estate

SP4T Switch

IQ Mixer

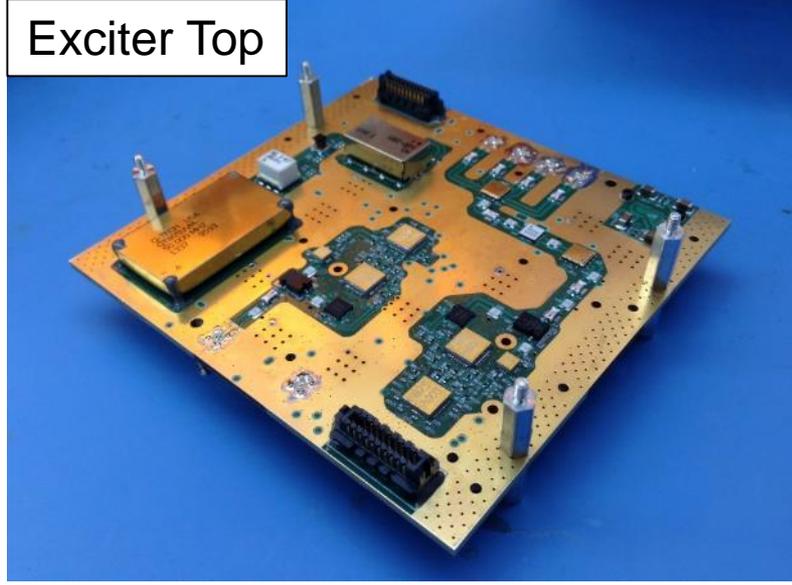
Relative package sizes



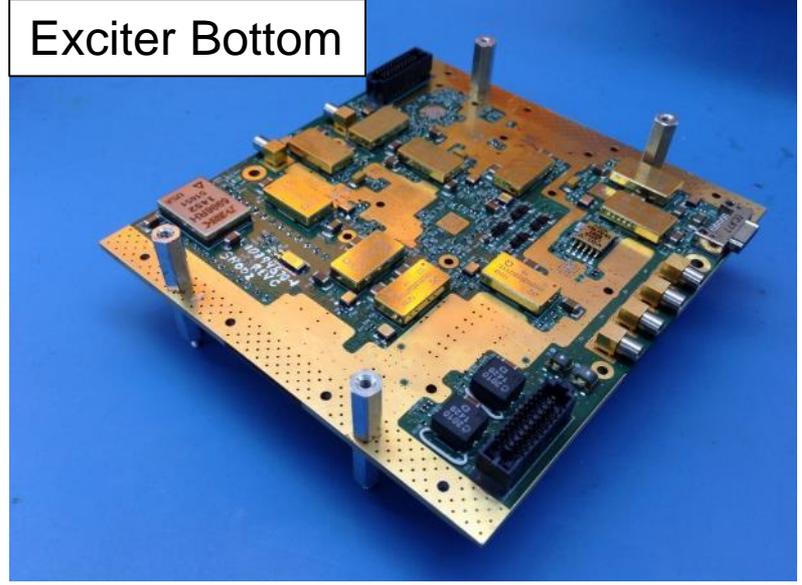


Iris V2 Exciter and Receiver

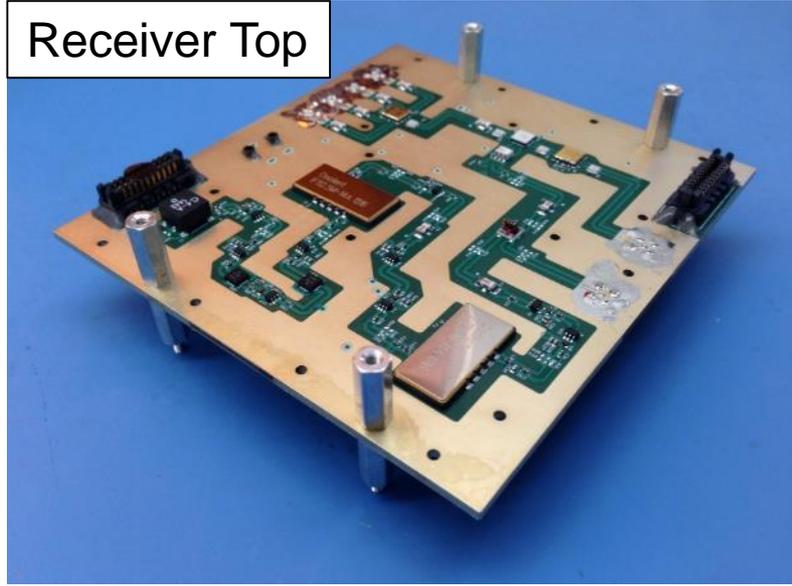
Exciter Top



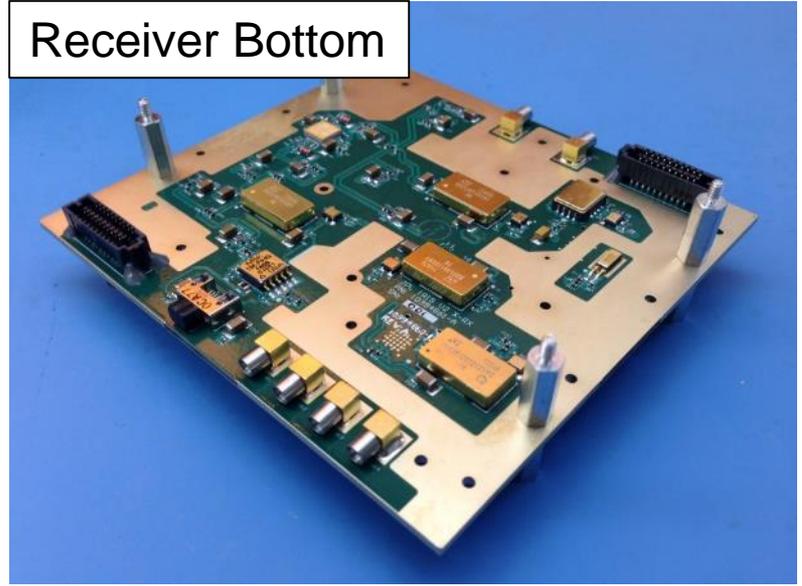
Exciter Bottom



Receiver Top



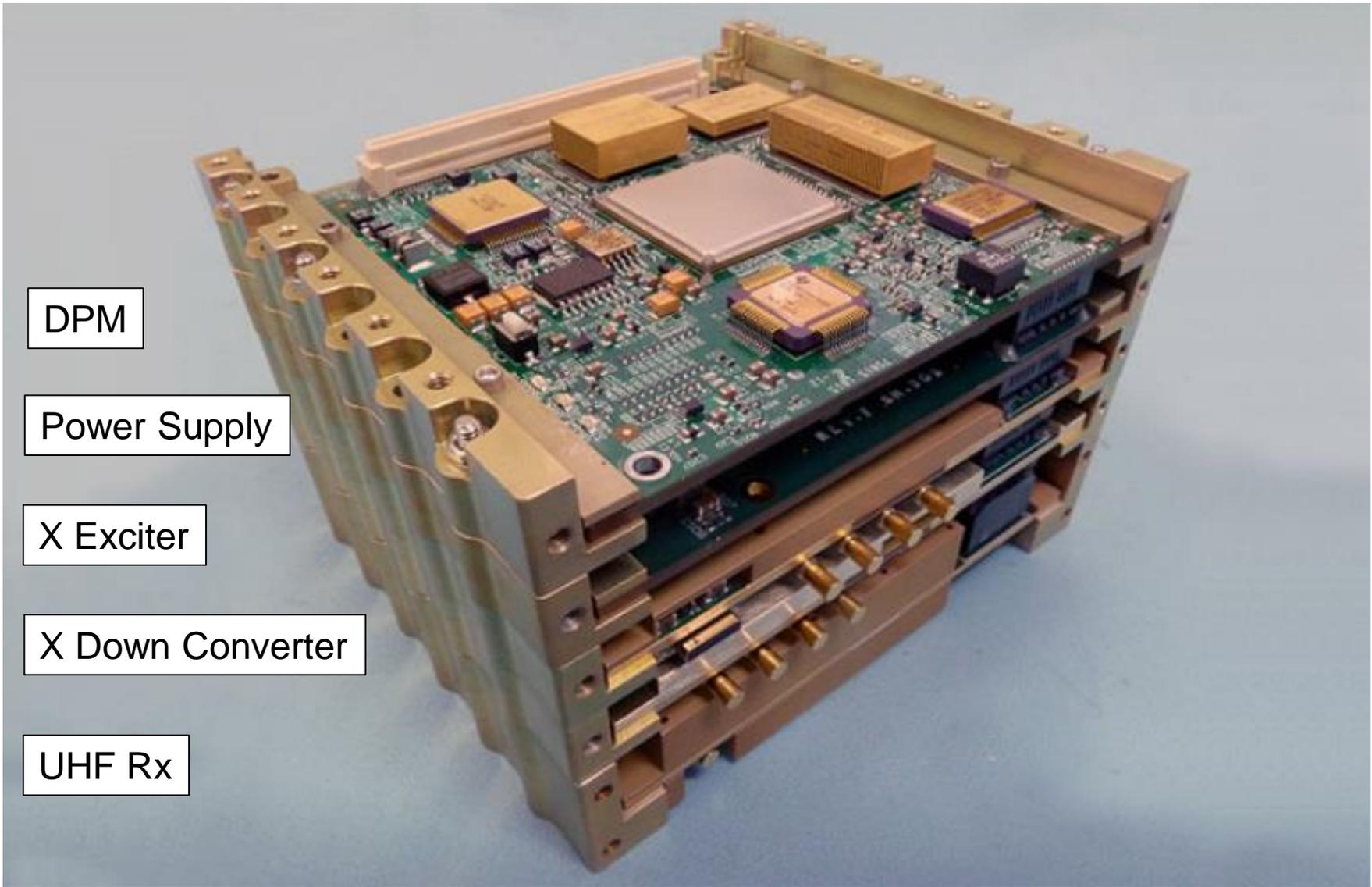
Receiver Bottom





Iris V2 Stack

Jet Propulsion Laboratory
California Institute of Technology



DPM

Power Supply

X Exciter

X Down Converter

UHF Rx



Iris RTD Proposed Packaging Approach

Packaging Challenge:

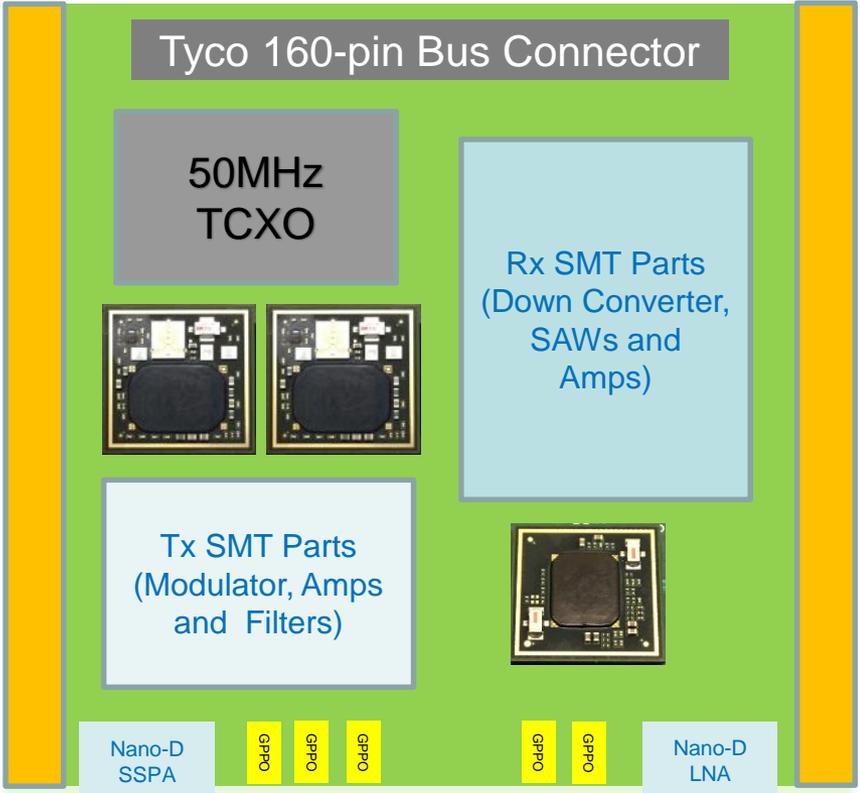
What can we do with packaging to fit what is on 96 in² (3 slices) of PCB real estate onto 16 in² (1 slice)

Packaging Response:

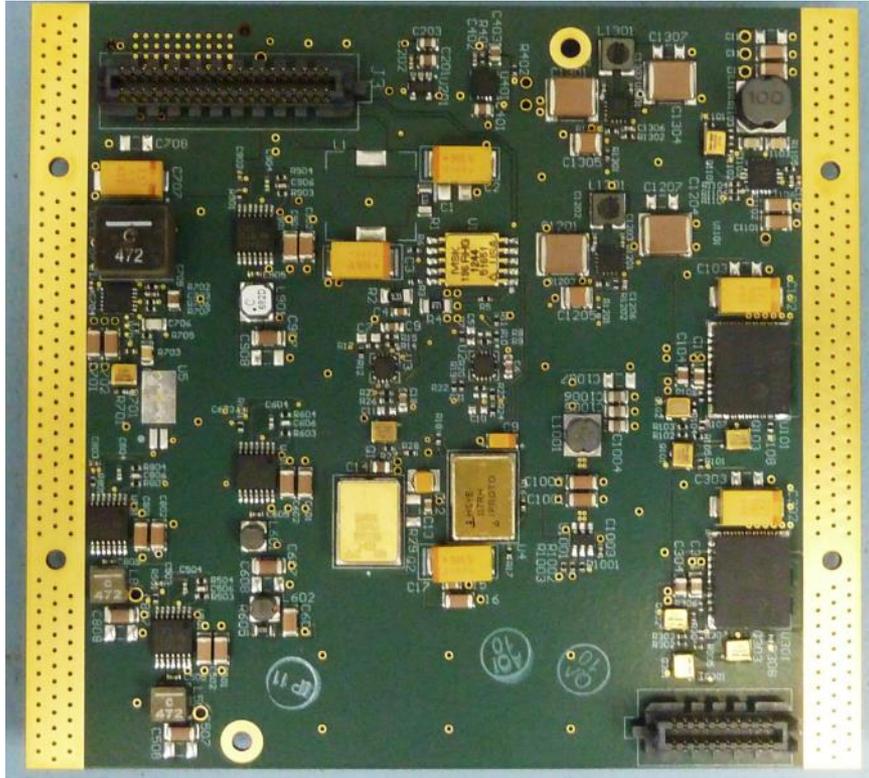
Remove all packaging wherever possible and package die on high density laminate Multi-Chip Module (MCM)



TOP



BOTTOM (PSB)



- Reduction from 3 slices to 1 slice.
- An ASIC would be the ideal case but the cost would be about an order of magnitude more just for the LO.

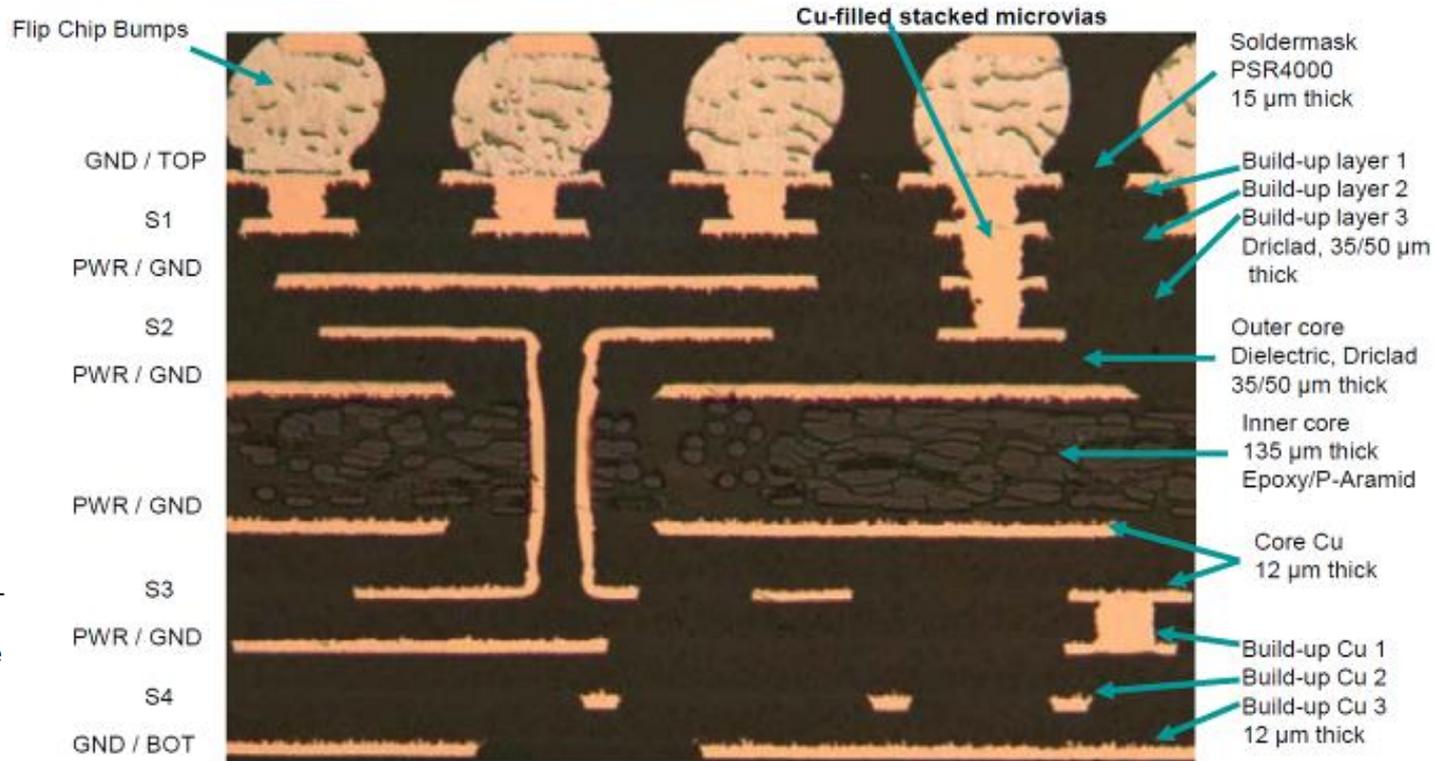


CoreEZ Description

Jet Propulsion Laboratory
California Institute of Technology

Thin Core Build Up

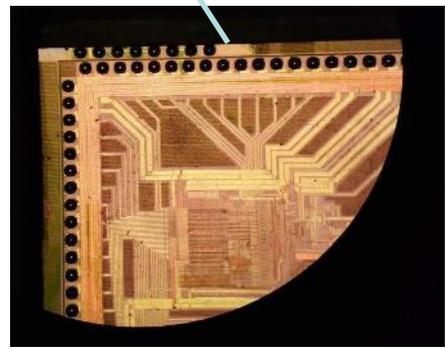
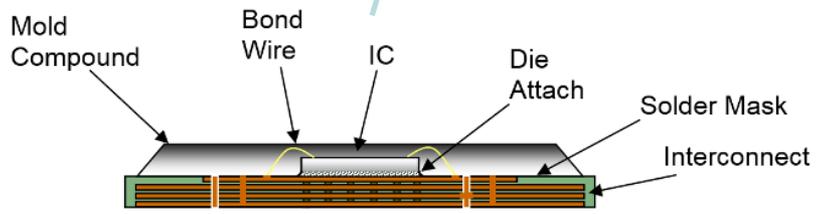
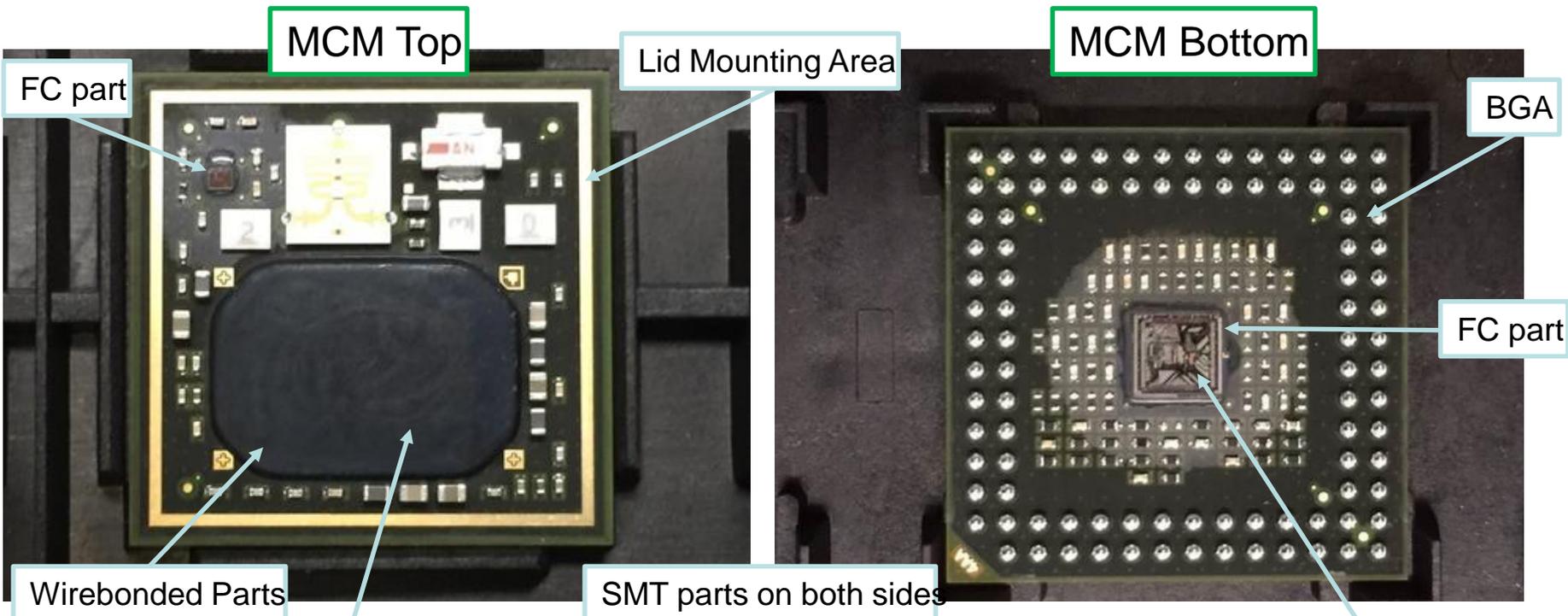
- Cost performance
- Particle filled epoxy
- Thin core (coreless)
- **Laser drilled core**
- **Laser drilled build up**
- 25 micron trace
- 25 micron space
- Buried resistors
- Flip chip, Wirebond, SMT
- **Radiation Hard Capable**
- $\epsilon_r = 3.7$



- 3-4-3 Stack up (10 copper layers)
- Substrate thickness 0.7 mm



MCM Description



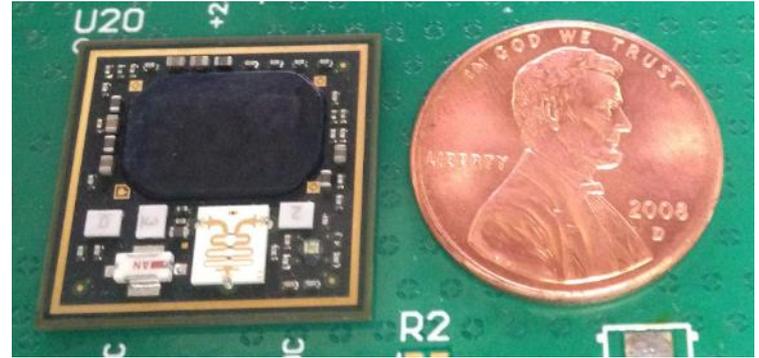
- FY'15 effort to explore reliability of MCM modules by i3electronics.
- Effort to miniaturize PLL Synthesizer from Iris V2 Exciter design to a 19mm² package.
- FY'16 effort to miniaturize the RF IF chain (VVAs, fixed amplifiers and corresponding LDOs)



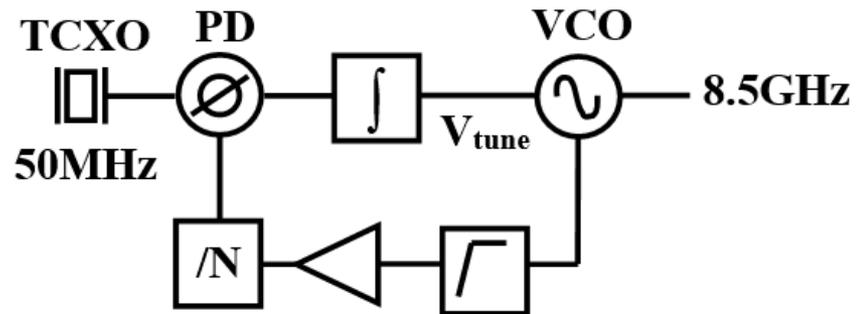
Approximate PCB layout area:
24mm x 37mm for top side and
slightly larger for bottom side



>80% area
reduction



Miniaturized MCM chip:
19mm x 19mm takes up one side
of PWB and include the LDOs.





Packaging Challenges

Jet Propulsion Laboratory
California Institute of Technology

- This slide is in the works but will be similar to that in slide 7 but for UST / NISAR

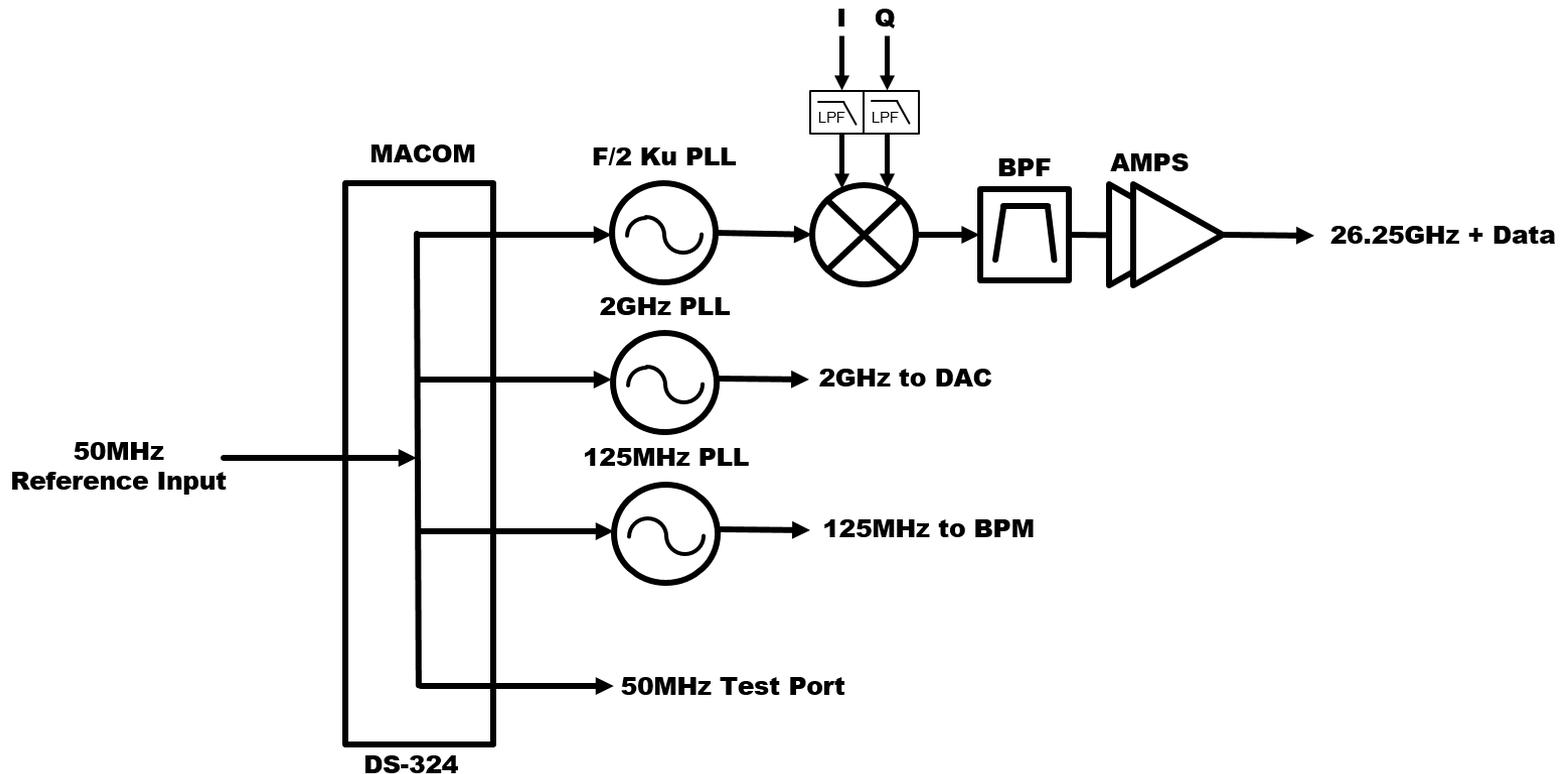


NISAR UST Ka-Exciter

Jet Propulsion Laboratory
California Institute of Technology

Generates the following:

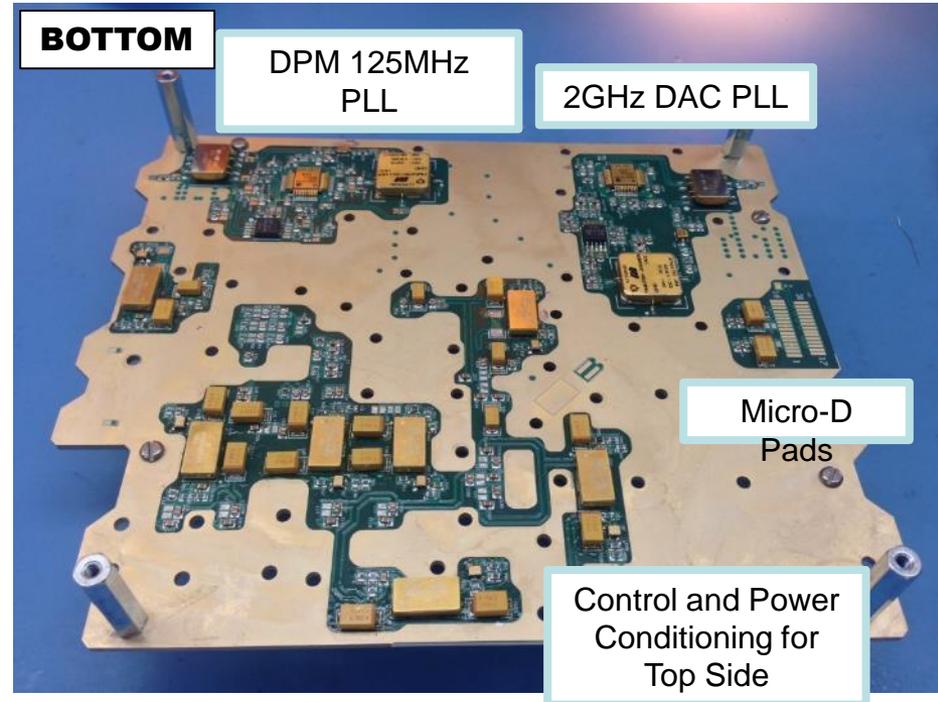
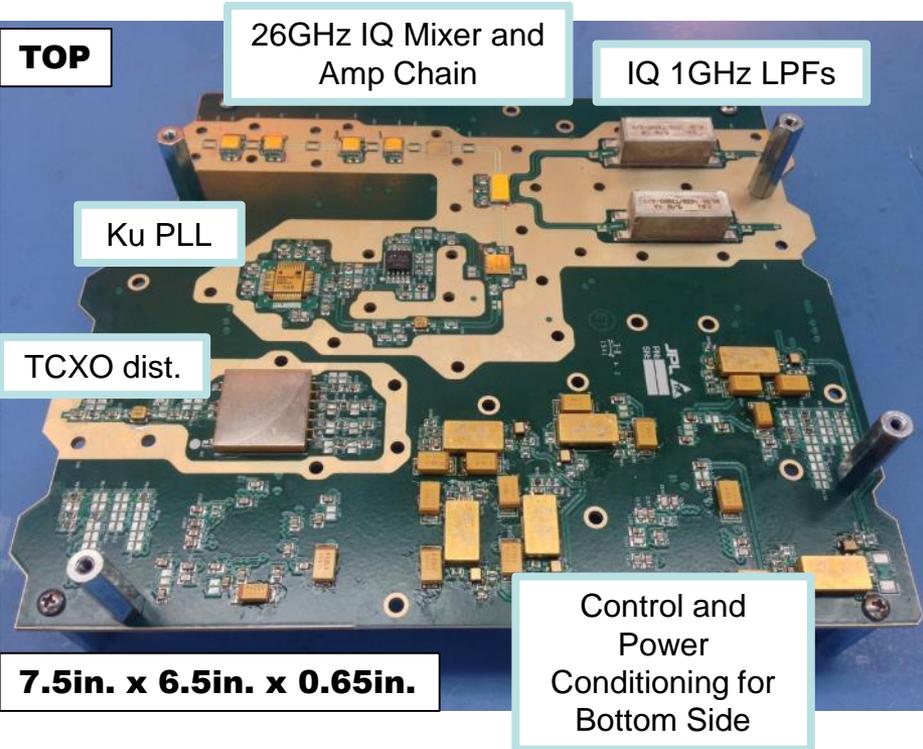
- High rate QPSK modulated 26.25GHz signal
- 2GHz clock for high rate DACs
- 125MHz clock for BPM
- Distributes the 50MHz reference





Jet Propulsion Laboratory
California Institute of Technology

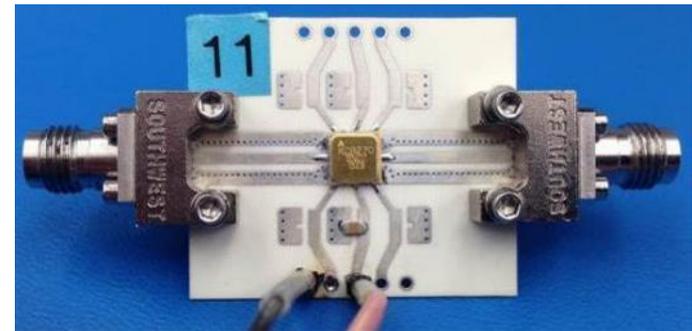
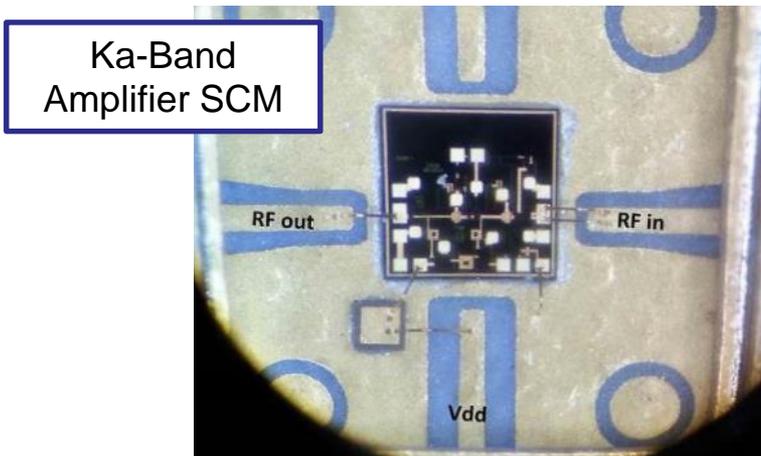
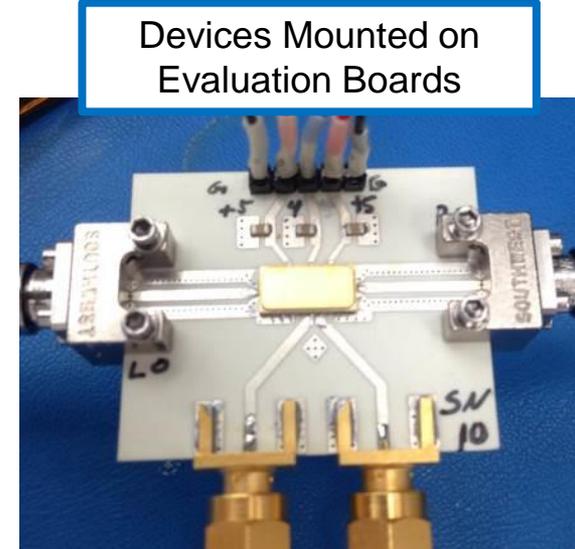
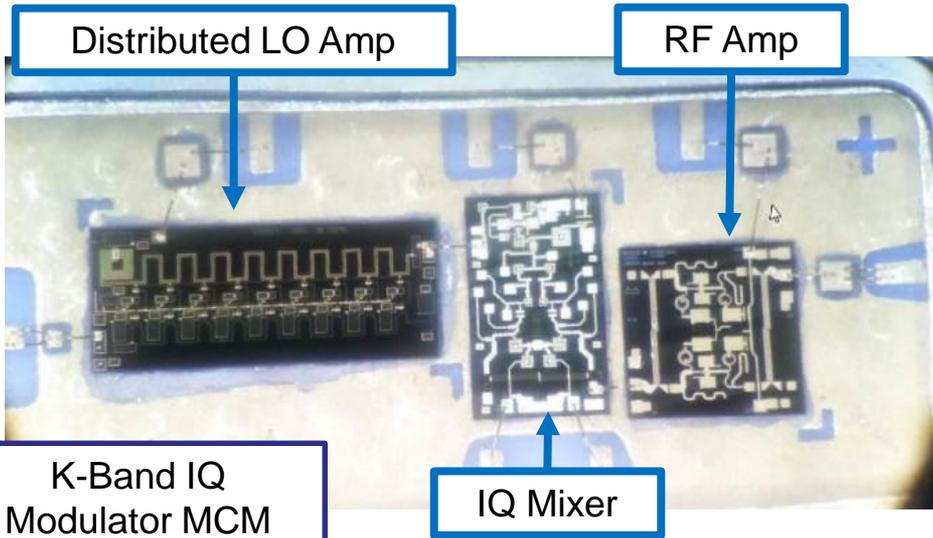
Ka Band Exciter Detailed PWA View



- Top side contains the 26GHz RF Circuits, 50MHz TCXO distribution and both the 125MHz & 2GHz PLL power conditioning.
- Bottom side contains 125MHz PLL, 2GHz PLL and power conditioning for top side 26GHz circuits & TCXO distribution.



KTM RF Chain Custom Packaged Devices





UST KTM RF Packaging Approach Trade-off

Advantages:

- All SMT hence low cost and quick to build
- Less tuning time
- Rugged assembly, no exposed die or bond wires

Disadvantages:

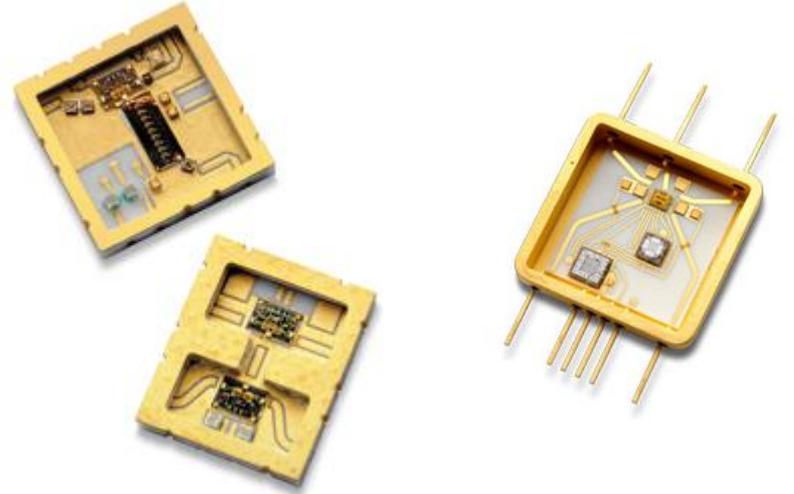
- No access to MIC level tuning
- Developing packages requires some NRE costs
- More engineering time goes into PWB layout for isolation
- If there is serious damage to the PWB, the complete PWA may have to be scrapped
- Internal covers can be costly and take time to manufacture



KCB Solutions

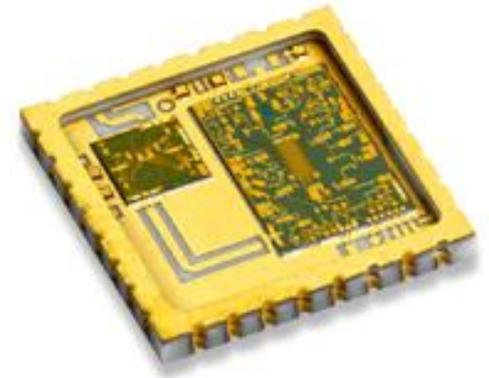
Flight Heritage Examples:

- Maven
- DSAC
- TDRSS



S-Level screening per:

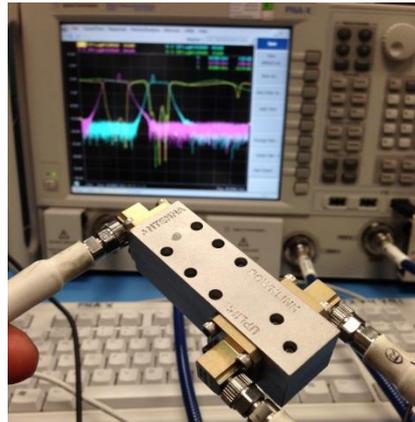
- MIL-PRF 38534 Class K (MCMs)
- MIL-PRF 38535 Class S (SCMs)





Cubesat Ka-Band Waveguide Diplexer

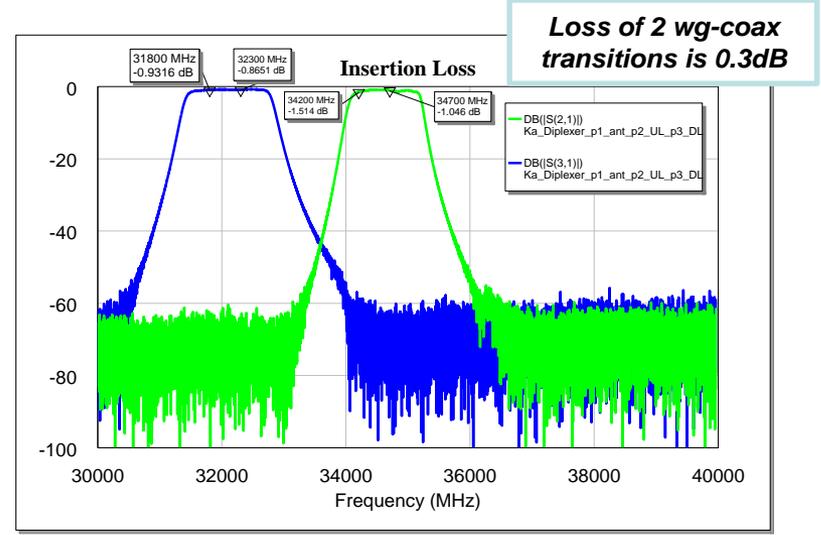
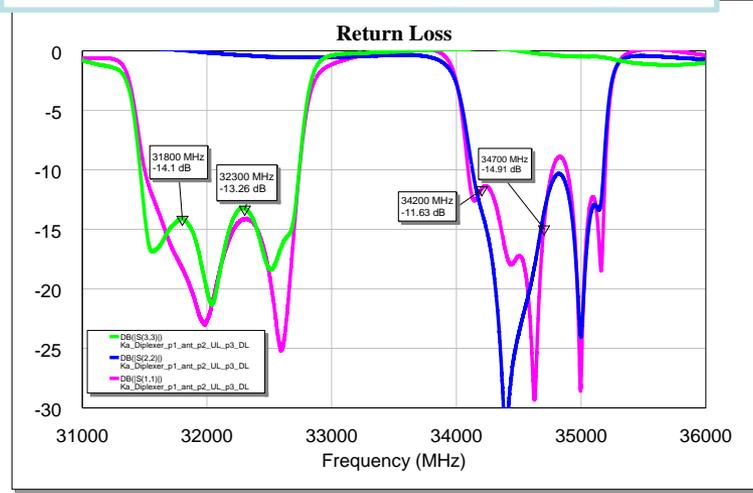
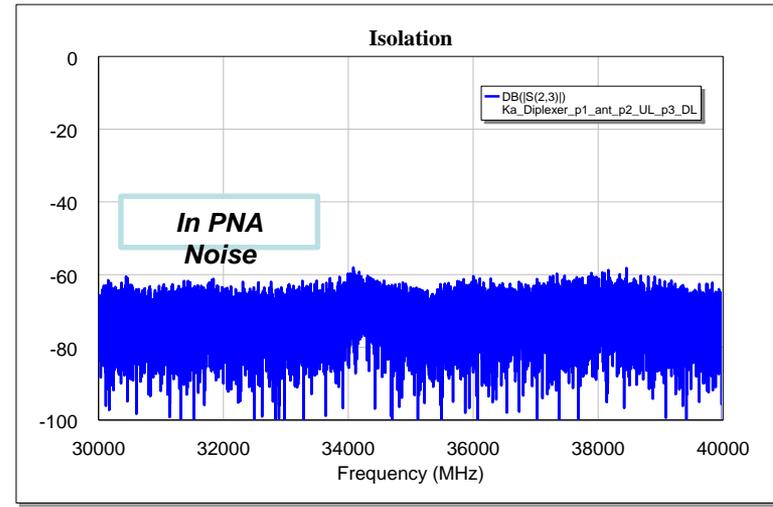
Jet Propulsion Laboratory
California Institute of Technology



**Assembled Dimensions:
0.8"x0.8"x2.7"**



**Cost of <\$1K to 3-d print vs. >\$5K for CNC
2-3 weeks 3-d print vs. > 1 month CNC
CNC machine produces significantly better accuracy
DMLS Direct Metal Laser Sintering of AlSi10Mg**





- Show MIC comparison to show size reduction from say THz Radar to SMT MCM
- Show SC which are currently and planning to use this technology



Iris V1 RF Packaging Approach Trade-off

Advantages:

- All SMT hence low cost and quick to build
- Less tuning time with all SMT design, less variation due to interconnects and cover effects
- Rugged assembly, no exposed die or bond wires
- Highly integrated design

Disadvantages:

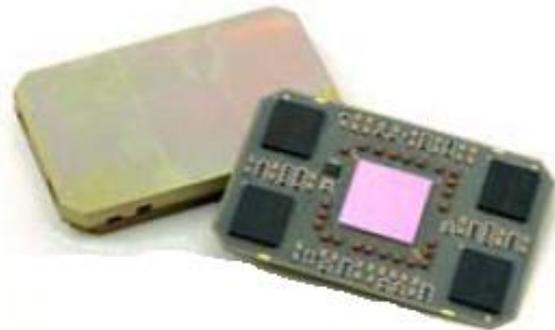
- More in-house packaging effort has a learning curve
- Smaller parts make for more tedious handling
- If there is serious damage to the PWB, the complete PWA may have to be scrapped



I3 Electronics

Jet Propulsion Laboratory
California Institute of Technology

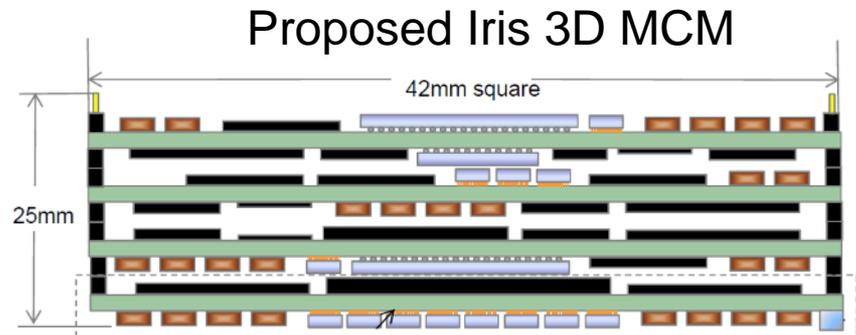
- IBM Spinoff.
- They were the IBM packaging solution for their super computer MCMs.
- 10+ years of high density packaging experience
 - First fabricated an MCM with them in 2004
- Over 3,000 modules in space applications
- Proven High Reliability



To Conclude, Other Future Packaging Options

Other packaging approaches we have explored but didn't talk about here:

- TSV (through Silicon Vias)
- ASIC / MMICs / RFICs
- Nuvotronics Polystrata
- 3D MCMs

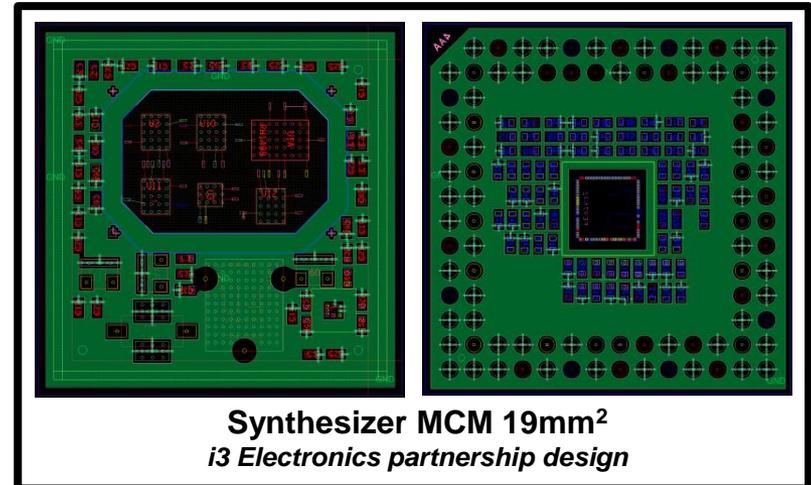
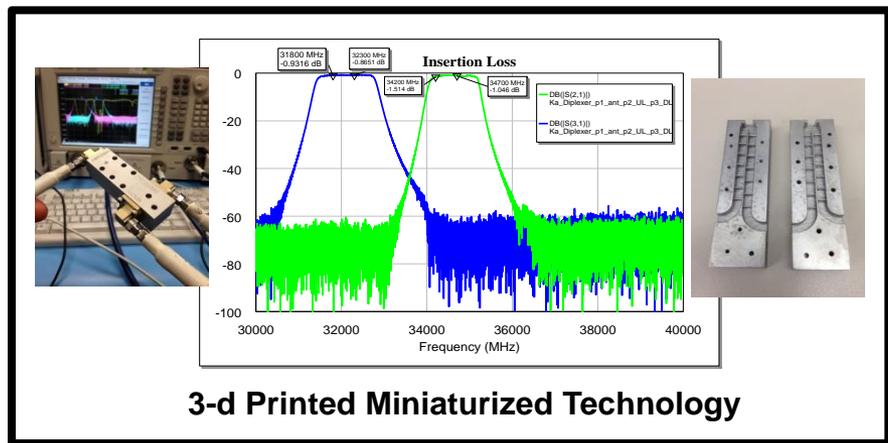


End results of ultimate miniaturization will likely be a combination of packaging and IC technology.



Present RF Packaging Tasks

➤ FUTURE WORK – THIS SLIDE FORMATTING WILL BE UPDATED





Jet Propulsion Laboratory
California Institute of Technology

Thank you!



Backup Slides