



Organic Flip Chip Reliability Study for Space Applications

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1.0 INTRODUCTION

1.1 Background

High temperature co-fired ceramic (HTCC) is the current standard flip chip substrate material for space applications. Low temperature cofired ceramics (LTCC) has been sometimes used for flip chip packaing for specialty applications, such as radio frequency (RF). For commercial applications, organic substrates have become the mainstream technology over the ceramic substrates about two decades ago. When flip chip technology was first introduced in the 1960s, high temperature co-fired ceramic (HTCC) was the standard substrate material for flip chip packages. In the 1990s, organic substrate technology was implemented for commercial applications. The initial driving force for the change from ceramic to organic substrate was to reduce the cost of flip chip parts for low-end products. Later, the organic substrate became necessary to accommodate fine feature size. While organic substrates offer advantages over ceramic substrates in feature size and speed, the ceramic substrates have advantages over the organic substrate, such as the ability to offer hermeticity, low coefficient of thermal expansion (CTE) mismatch with silicon, good co-planarity, and high thermal conductivity. In addition, the high temperature stability of the ceramic substrate allowed the use of high melting temperature solder as the flip chip bump material, which does not reflow during the subsequent reflow processes. The widespread and the popularity of the organic substrates enabled rapid maturation and improvement of the technology, and organic substrate parts are currently used for high end products, such as mainframes and supercomputers.

The main advantage of the ceramic substrate is its capability to provide hermeticity. The introduction of the space field programmable gate array (FPGA) with non-hermetic ceramic flip chip configurations, such as Xilinx Virtex 4 and 5, triggered studies on whether the hermeticity is critical for underfilled flip chip devices, since the underfill material provides protection to flip chip bumps from the environment. The mil-std-38535 class-Y requirements were setup to bring non-hermetic ceramic flip chip packages into the Qualified Manufacturers List (QML) system. A number of reliability studies were done on class-Y type packages to support the class-Y standards and showed that non-hermetic ceramic flip chip packages have sufficient reliability for space applications. The high reliability of the class-Y parts were mainly attributed to the use of underfill. The fact that the hermeticity is not critical for the reliability of flip chip devices suggested that organic flip chip packages could be reliable enough for space applications. The current report summarizes the result of collaboration between JPL and Cobham semiconductor space solutions through the FY16 to FY18 to study the reliability of the organic flip chip packages.

1.1.1 *Ceramic vs Organic flip chip*

When the organic substrate was first introduced in the commercial sector in 1990's, the primary driver of transition from ceramic to organic substrate was the cost. The modern organic substrates for flip chip devices are manufactured with High Density Interconnect (HDI) technology. The typical construction of the most commonly used type of organic substrate is shown in Figure 1. HDI layers with microvia are built up on the core using lithography and laser drilling process. Table 1 compares typical feature size and materials properties of HTCC and organic substrate [1, 2, 3, 4]. The organic substrates can offer smaller feature sizes than HTCC substrates. The organic substrate can potentially provide higher signal speed than the HTCC

substrate due to its low line resistance and low dielectric constant, although the actual signal integrity is design-dependent.

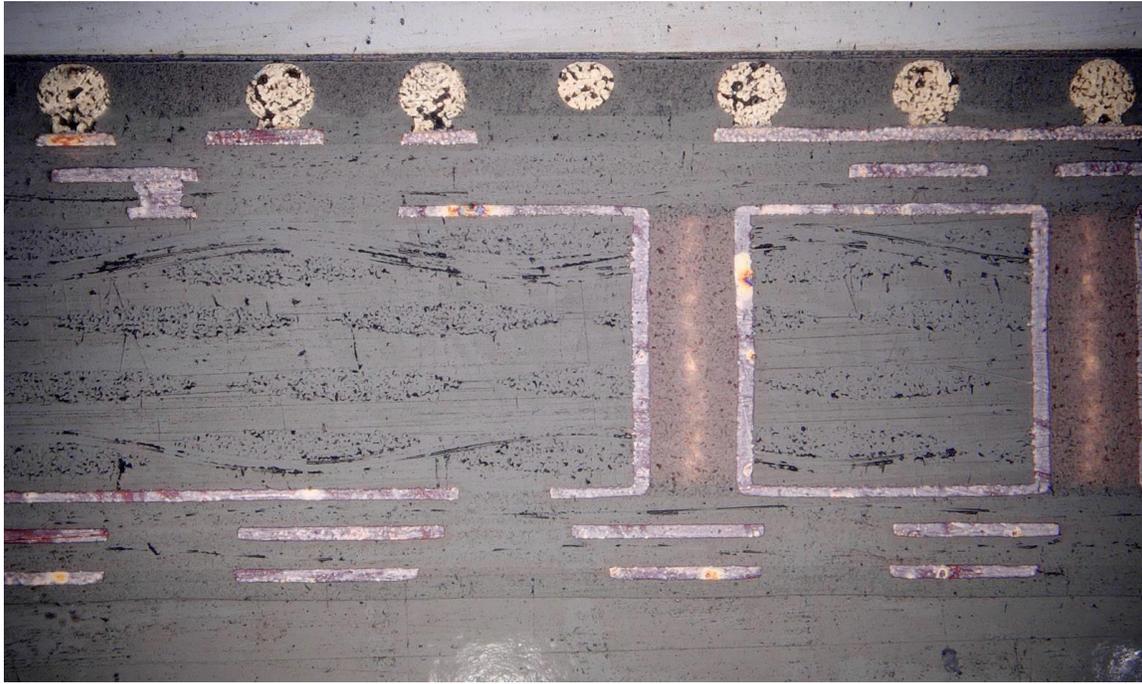


Figure 1. Cross-section of a typical organic substrate.

Table 1. Comparison of typical feature sizes and materials properties between HTCC and organic substrates

	HTCC Substrate	Organic Substrate
Bump Pad Diameter (μm)	~150	>60
Bump Pad Pitch (μm)	~250	>120
Trace Line Width (μm)	100~125	9~15
Trace Line Spacing (μm)	100~125	12~15
Via Diameter (μm)	125~200	50~65 (12mil for core)
Via Pitch (μm)	250~640	100~125 (40mil for core)
Dielectric Const.	8.5~10	3.2~4.8
Dielectric Loss Angle	0.0005~0.007	0.019~0.248
Trace Sheet Resistance ($\text{m}\Omega/\text{sq}$)	8~17	3

1.1.2 Organic substrate technology and underfill

Organic substrates have a higher CTE mismatch to the Si die compared to ceramic substrates, although it has lower CTE mismatch with the circuit board. When the organic substrate was first being developed in 1990s, premature failure of solder joints during the thermal cycling was the major issue. Underfill solved the premature solder joint failure issue, and enabled organic flip chip packages. The underfill reduces the stress on the flip chip solder bumps and increases solder joint fatigue life by 10 to 100 times. In addition, it eliminates the need of hermetic sealing by protecting solder bumps from external environments. Since underfill

eliminated the need of hermeticity, it enabled the Class-Y non-hermetic ceramic flip chip parts for space applications.

When the underfill was first introduced, they were typically formulated to have T_g (glass transition temperature) above 120°C , high elastic modulus (above 9-10 GPa), CTE similar to solder (25 ppm/ $^\circ\text{C}$), and good adhesion. All of these property preferences were focused around enhancing the underfill's capability to reduce stress in flip chip bumps, although there has been continuing debate on optimal CTE of underfill. However, these property criteria for underfill have changed as the flip chip technology has evolved. Widespread use of low-k material, increased wafer thickness (due to the increased wafer size), reduced bump pitch size, increased die size, lead-free bumps, and diversification of substrate structure made the classic underfills not compatible with some of the modern devices [5]. The industry concluded that the underfill properties can be rather flexible and good reliability can be achieved through balancing different properties. The only property requirement that still stands valid today is having good adhesion with all materials the underfill is attached to.

In addition to the inherent properties of the underfill, workmanship and quality during the production also have a great impact on the underfill reliability. The dispensing needs to be developed to minimize the void and achieve a good underfill fillet. Voids can form inside an underfill during dispensing process if air is trapped inside. Voids can also form during the cure due to the shrinkage of underfill. A fillet of at least 50% up the all die sidewall is required for organic flip chip packages [13]. Details in the application and cure process, such as dispensing machine temperature drift, thawing and storage life control, and moisture control can also cause voiding [6].

2.0 EXPERIMENTAL

In the current task, test vehicles were assembled using 3 different underfill materials. The test vehicles were subjected to various reliability tests.

2.1 Description of test vehicle

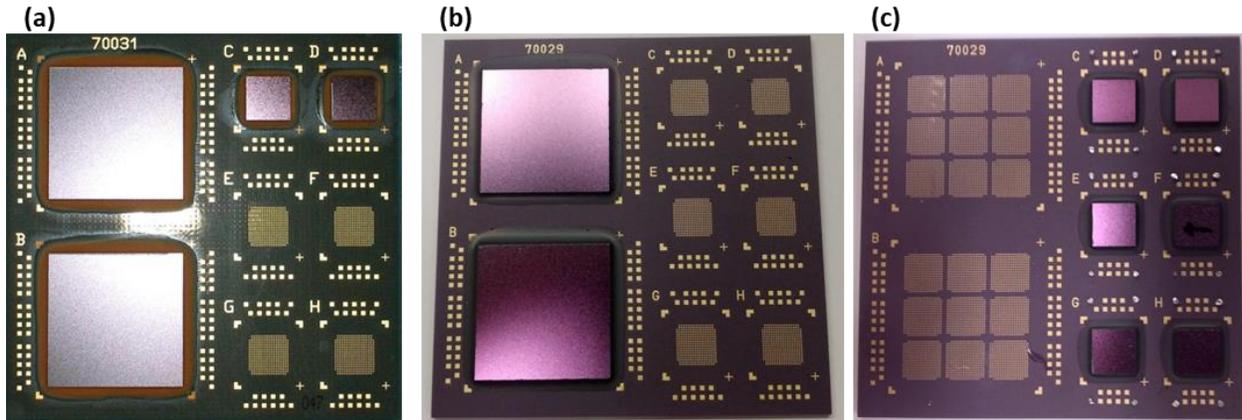


Figure 2. The test vehicle used in the current task. (b) and (c) The test vehicle used in FY13 joint task between Cobham and NEPP.

The test vehicle was designed to have an identical layout as the class-Y samples that Cobham and NEPP had evaluated during the FY13 NEPP task [7] to compare the reliability of the organic packages with class-Y packages, as shown in the Figure 2. The daisy chain dies had two different sizes, 5x5mm and 15x15mm. The 5x5mm die had 317 I/Os and the 15x15mm die had 2853 I/Os. The die's metallization was Al/Ni(V)/Cu. The flip chip solder bump material was Sn63Pb37. The organic substrate was 45x45mm large and had 1-2-1 build-up construction with BT (Bismaleimide-Triazine) core and an ABF (Ajinomoto Build-up Film) build-up material. The pads were solder mask defined and had ENIG (electroless nickel-gold) finish. Three different underfill materials were tested. The first one designated as the "Control" underfill is the material that was qualified during the previous study between Cobham and NEPP [7]. The other two materials, material A and B, were selected based on their Tg and CTE. The underfill fillet was longer at one edge than other edges of the dies, as shown in the Figure 3, as a result of the single edge line dispensing.

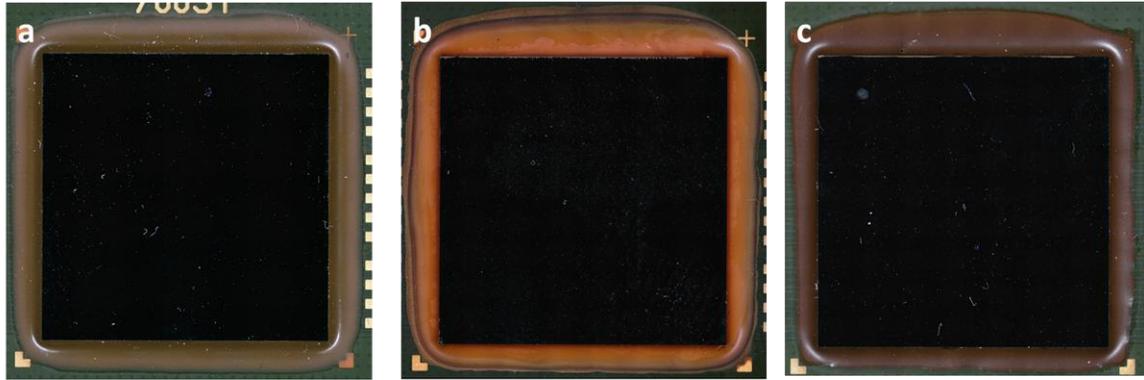


Figure 3. Underfill fillets of the 3 underfills, (a) Control underfill, (b) Underfill A, (c) Underfill B. The upper edges have longer fillet.

2.2 Materials Properties

2.2.1 Outgassing Properties

Outgassing properties of the ABF material and underfill were evaluated per ASTM E595. The total mass loss (TML) and collected volatile condensable material (CVCM) results are shown in the Table 2. The Control underfill had been tested for outgassing during the previous task. All materials met the NASA requirement of <1% TML and <0.1% CVCM. Both underfill materials had very low outgassing. The ABF material also had low outgassing. The ABF material is the de facto standard material for the organic build-up substrate in the industry and there are many different versions of the ABF material [8].

Table 2. Outgassing properties of ABF material and underfill materials

Sample	TML %	CVCM %
ABF Material	0.40	0.01
Control Underfill	0.24	0.01
Underfill A	0.38	0.00
Underfill B	0.28	0.01

2.2.2 Thermomechanical properties of underfill

Tg and CTE of the 3 underfill materials are summarized in the Table 3. The TMA (Thermomechanical Analysis) results of the underfill A and B are in the Figure 4.

Table 3. Tg and CTE of the 3 underfill materials

	Tg (°C)	CTE (ppm/C)
Control Underfill	120	28
UF A	135	27
UF B	115	23

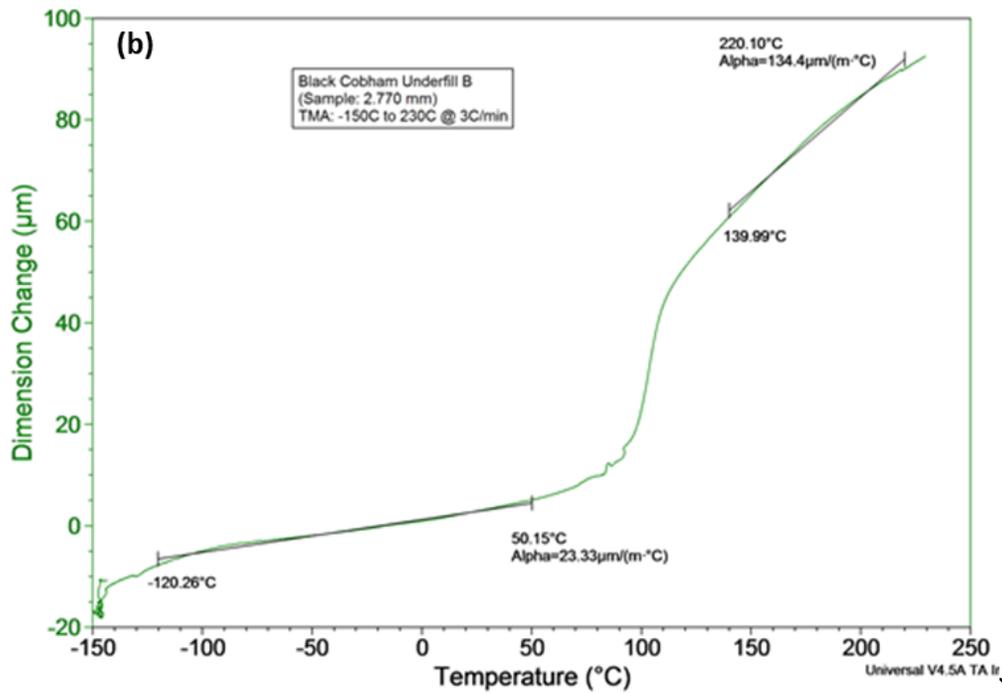
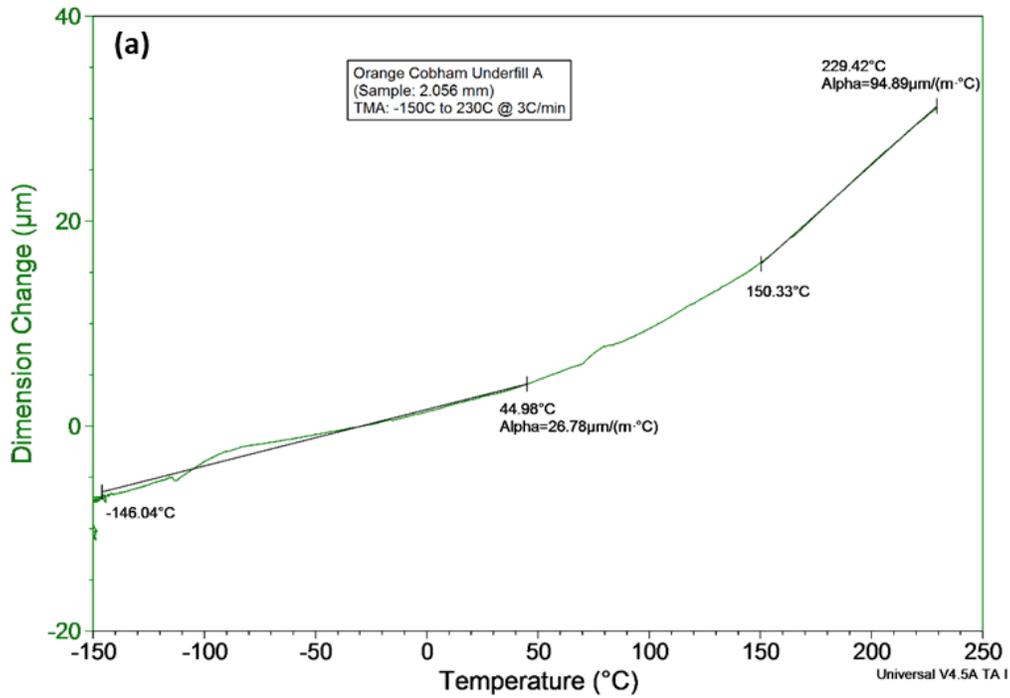


Figure 4. TMA result of the Underfills, (a) A and (b) B.

Dynamic Mechanical Analysis (DMA) was also performed at both 1Hz and 0.01Hz, over a temperature range of -145 to 210°C, as in the Figure 5, to characterize the Storage and Loss

moduli. The reason for performing DMA tests at 0.01Hz was to simulate the strain rate of the underfill during the temperature cycling [9].

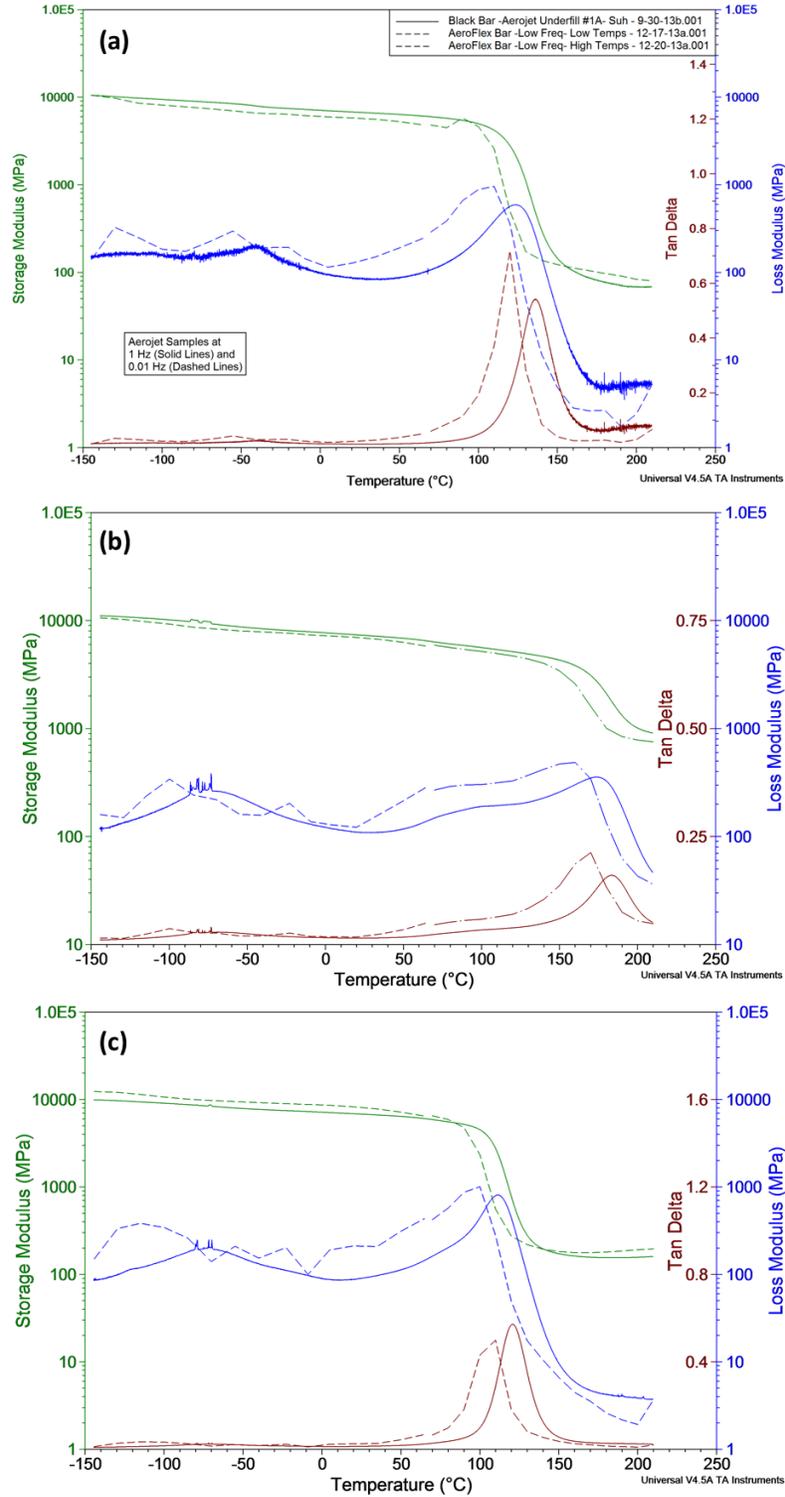


Figure 5. DMA results of the underfill samples, (a) Control, (b) Underfill A, (c) Underfill B, acquired at two frequencies: 1 Hz – Solid Lines; 0.01 Hz – Dashed Lines.

2.3 Test Matrix

Table 4 summarizes the test matrix. The numbers in the table indicate the quantity of sample assigned to each test. The main purpose of the tests was to compare the reliability of organic substrate samples with the previous Class-Y samples [7], rather than to perform industry standard tests.

Temperature cyclings were done at two different thermal cycling profiles, up to 4250 cycles. The dual zone chamber thermal cycling was done at Cobham from -55 to 125°C, with 15 minute dwell time. The ramp rate was about 214°C/min, as the samples were traveling between hot and cold chamber. The single zone chamber thermal cycling was done by JPL from -55 to 125°C, with 12°C/minute ramp rate and 15 minute dwell time. Some samples were preconditioned at 85°C/85%RH for 1000hours prior to temperature cycling to test underfill’s resistance to moisture. The temperature cycling was done without baking out the samples to test for the worst case condition where packages are being stored in a humid environment then thermal cycled. The industry standard procedure for preconditioning non-hermetic packages prior to reliability tests is to first perform 5 cycles of -40 to 60°C temperature cycling, bake out, expose parts to humidity according to their moisture sensitivity levels, and to perform 3 simulated reflows within 4 hours after humidity exposure, per JESD22-A113 [10]. Although the industry standard preconditioning tests ensures a device’s capability of withstanding multiple assembly cycles and the field conditions prior to accelerated tests, the tests can be potentially inadequate for flip chip devices [11]. Application of the JESD22 preconditioning to flip chip devices can cause popcorning of the underfill during the simulated reflow, which can be excessively damaging to the flip chip solder joints.

The continuity was checked by manually probing the samples at room temperature every 250 cycles. Sometimes cracked solder joints can exhibit electrical discontinuity only at a certain range of temperature while showing “false pass” at other temperature ranges. The false pass can take place more easily if solder joints are encapsulated as the underfilled flip chip bumps. It would have been ideal if resistance of samples had been continuously monitored, as the false pass can be avoided by the continuous monitoring. However, the probing pad geometry and quantity of sample did not easily allow for a continuous monitoring.

Table 4. Test matrix

Solder Material	Underfill	Dual Zone TC -55/125	Single Zone TC -55/125	85°C/85%RH 1000hr + Dual Zone TC -55/125	85°C/85%RH 1000hr + Single Zone TC -55/125	High Temperature Storage (125C)	High Temperature Storage (150C)	85°C/85 %RH 1000hr + Stud Pull/Die shear
Sn63Pb37	Control	6	5	6	5	3	3	2
	A	6	5	6	5	3	3	2
	B	6	5	6	5	3	3	2

3.0 RESULTS AND DISCUSSION

The test results in this report will mainly focus on the temperature cycling test results.

3.1 Temperature cycling test

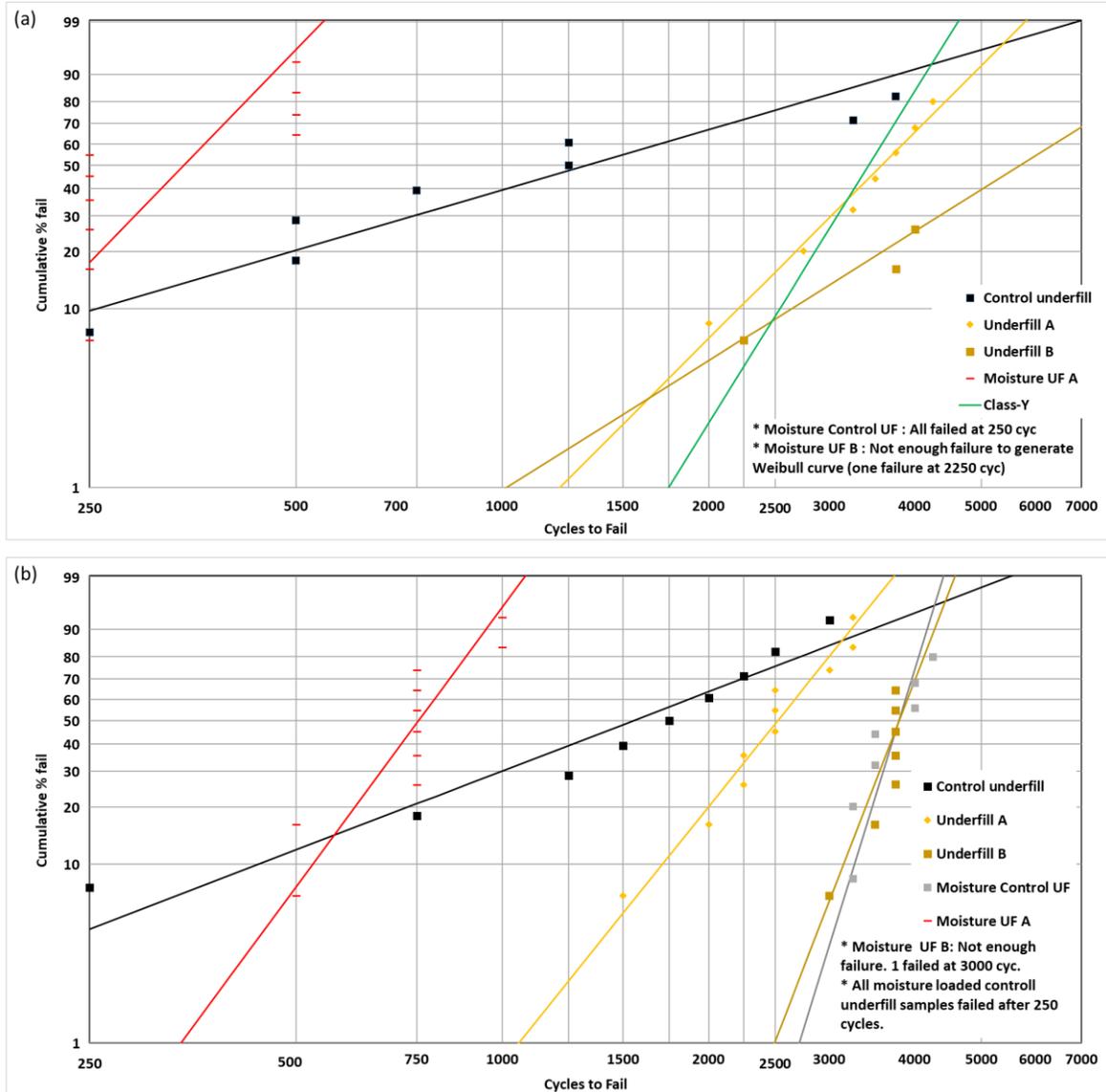


Figure 6. Weibull plots of 15x15 mm dies, during (a) Dual-zone (fast ramp rate, chamber-to chamber) thermal cycling, (b) Single-zone (slow ramp rate) thermal cycling.

Temperature cyclings were done from -55 to +125°C with 15 min dwell time, at two different ramp rates. One set of samples temperature cycled using a dual-zone chamber, with estimated ramp rate of ~210 °C/min. The other set of samples were temperature cycled using a single zone chamber, with ramp rate of 12 °C/min. Figure 6 (a) and (b) shows the Weibull plots of temperature cycling life of the samples with 15x15mm die size at different ramp rates. In the plot of dual-zone temperature cycling data, Figure 6 (a), a Weibull plot of the FY13 Class-Y sample reliability is shown as a reference. The temperature cyclings were done up to 4250

cycles. The characteristic life and beta of the Weibull distribution is summarized in Table 5 and Table 6. The samples using underfill B exhibited remarkably longer life than samples with other 2 underfills. The 5x5mm die samples also had some failures mainly at underfill A samples pre-conditioned with 1000 hours of 85°C/85RH, as in Table 7 and Table 8.

Table 5. Dual-zone (fast ramp rate) temperature cycling results of 15x15 mm die samples.

	Characteristic Life	Beta	R2
Control Underfill	1822	1.15	0.91
Underfill A	3927	3.92	0.98
Underfill B	6608	2.46	0.93
Moisture loaded Control UF	All failed after 250 cycles		
Moisture loaded UF A	376	4.04	0.60
Moisture loaded UF B	One failed after 2250 cycles		

Table 6. Single-zone (slow ramp rate) temperature cycling results of 15x15mm die samples.

	Characteristic Life	Beta	R2
Control Underfill	1981	1.50	0.93
Underfill A	2719	4.87	0.95
Underfill B	3897	12.69	0.78
Moisture loaded Control UF	3929	10.14	0.84
Moisture loaded UF A	808	5.32	0.82
Moisture loaded UF B	One failed after 3000 cycles		

Table 7. Dual-zone temperature cycling results of 5x5 mm die samples.

	Characteristic Life	Beta	R2
Control Underfill	No failure		
Underfill A	No failure		
Underfill B	No failure		
Moisture loaded Control UF	3 out of 10 failed at 2750 cycles		
Moisture loaded UF A	1449	5.26	0.75
Moisture loaded UF B	No failure		

Table 8. Single-zone temperature cycling results of 5x5mm die samples

	Characteristic Life	Beta	R2
Control Underfill	4 at 3750		
Underfill A	No failure		
Underfill B	No failure		
Moisture loaded Control UF	No failure		
Moisture loaded UF A	1589	2.28	0.87
Moisture loaded UF B	No failure		

As stated earlier, the flip chip solder joint life is mainly determined by the underfill performance. When the solder joint failure is due to the underfill delamination, the fatigue model for solder joints is no longer effective for underfilled flip chip bumps. Underfilled flip chip bump failures are known to take place after the underfill starts to breakdown and stops redistributing stress around solder bumps [12]. During our FY13 study on class-Y packages, some of the samples were current stressed to reduce strength of solder joints by 20%. The current stressed samples, however, did not exhibit any reduction of temperature cycling life because the temperature cycling life was mainly determined by the underfill. On the other hand, humidity exposed samples showed 33% reduction in temperature cycling life due to the degradation of underfill [7].

Underfill voids are considered undesirable since stress cannot be redistributed from the flip chip bumps to underfill when voids are adjacent to flip chip bumps. Figure 7 shows the CSAM images of underfill voiding of 3 underfills. Each underfill showed unique voiding patterns in the 15x15mm dies, while in 5x5 mm dies showed small amount or no void. The voids, formed according to the flow characteristics of each underfill, can be always minimized through extensive process optimization. One of the possible reasons why the control underfill exhibited least amount of void might be because its application process was better optimized than other materials, as it has been used since FY13 NEPP task. Underfill A mostly formed voids adjacent to the flip chip bumps. Underfill B formed voids mostly at the saw street between the flip chip bump arrays, but still had some voids adjacent to the flip chip bumps. Underfill voids not adjacent to the flip chip bumps are considered benign as long as the adhesion is good. Underfill voids that are adjacent to flip chip bumps can lower the temperature cycling life, cause solder extrusion during the board level reflow process, or induce solder bridging [13].

The Control underfill samples exhibited high rate of early failures (below 250 cycles) compared to underfill A and B, although it had the least amount of void. These early failures due to the assembly process rather than the characteristics of material. Figure 8 shows cross-sections of flip chip bumps failed after 250 cycles. Solder joints are separated and underfill is filled between the separation, indicating the solder joint was poorly formed during the die attach process.

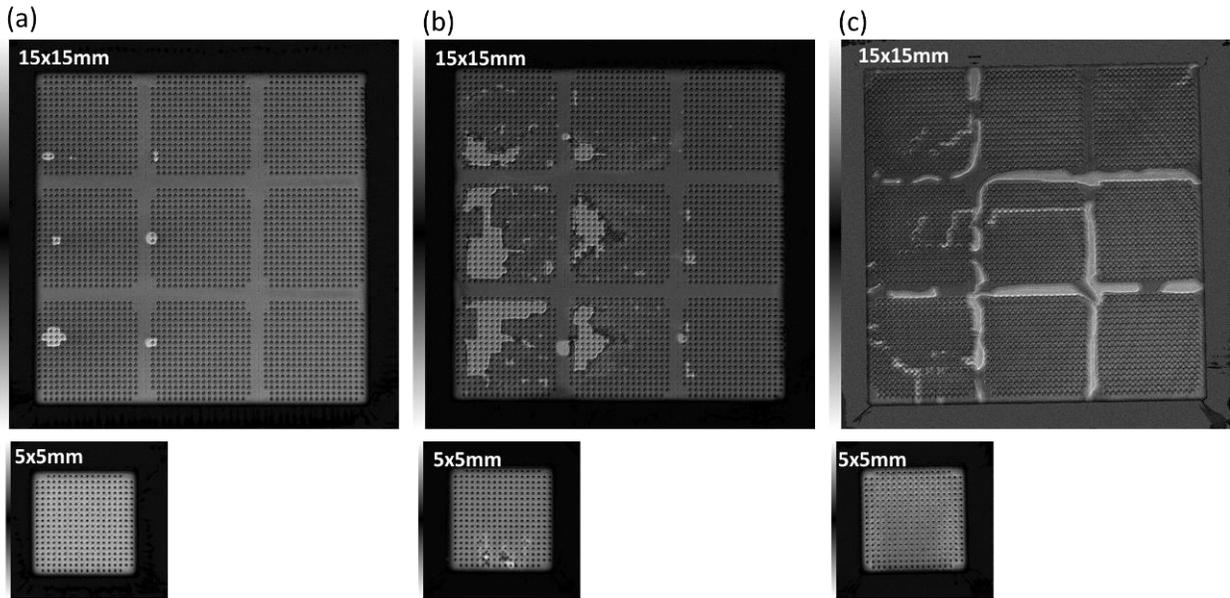


Figure 7. CSAM images showing typical voiding patterns of samples. The upper images are from 15x15mm die samples and lower images are from 5x5mm die samples, with (a) Control underfill (b) underfill A (c) underfill B.

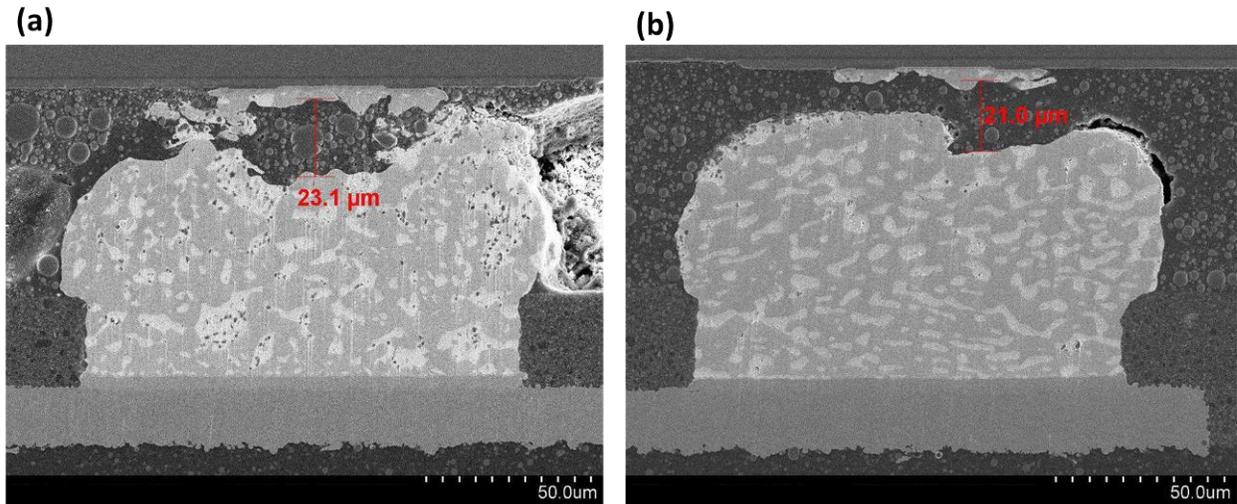


Figure 8. Cross-section of flip chip bumps in the Control underfill samples failed after 250 cycles, (a) without and (b) with 85°C/85%RH preconditioning.

At this moment it is inconclusive whether the overall short thermal cycling life of the Control underfill samples was due to sample assembly process or not. The cross-sections in some of the other samples, which failed early, did not show indication of poor die attach. The lifespan difference between underfill A and B samples can be in part explained by the voiding patterns, as underfill A samples had voids mostly adjacent to the flip chip bumps while underfill B samples

had voids mostly along the saw streets. However, underfill A had greater tendency to delaminate or crack during the temperature cycling.

One interesting aspect of the test result is that the effect of humidity exposure had different effects on all 3 underfills, as in the Table 9. Humidity is known to degrade underfill. Underfill materials can absorb moisture over long term and result in 50% reduction in interfacial fracture toughness [14]. Even after baking to remove moisture from underfill, underfill properties can only be partially recovered once an underfill material suffers degradation by moisture [15]. The underfill used in Virtex 5 CF packages exhibited 23% reduction in lap shear strength [16]. In our FY13 study, the control underfill samples preconditioned with 85°C/85%RH exhibited 31.5% reduction in thermal cycling life during dual-zone thermal cycling test [7]. In the current study, the Control underfill showed opposite effects from the humidity exposure during single and dual-zone thermal cycling. During the dual-zone test, thermal cycling life of the samples decreased as expected. On the other hand, thermal cycling life of the samples were increased during the single-zone tests. As for the underfill A samples, the humidity exposure consistently reduced thermal cycling life regardless of the ramp rate. B samples showed increased the thermal cycling life after humidity exposure, regardless of temperature cycling ramp rate.

Table 9. Moisture loading effect on characteristic temperature cycling life of 15x15 mm die samples

Sample type	Single zone (slow ramp)	Dual zone (fast ramp)
Control Underfill	Increase (1981 → 3929)	Decrease (1822 → less than 250)
UF A	Decrease (2719 → 808)	Decrease (3927 → 376)
UF B	Increase (3897 → Not enough failure)	Increase (6608 → Not enough failure)

The typical failure modes of the samples were underfill delamination, which lead to crack propagation in the flip chip bumps. There were many cracks around the entire fillets. Figure 9 and Figure 10 shows some of the cracks on the underfill fillets after 4250 cycles of single zone temperature cycling. Most of the 15x15mm samples had fillet cracks regardless of underfill type or preconditioning. On the other hand, most of the 5x5mm samples did not have fillet cracks. It must be noted that pictures of cracks shown here are taken from the samples after 4250 cycles, not upon the detection of electrical failure. The samples were thermal cycled up to 4250 cycles even after detection of electrical failure, because there were multiple dies in one sample and temperature cycling was continued to obtain thermal cycling life from as many dies as possible. The fillet cracks were observed both at corner and edge of dies. Underfill A sample had cracks mostly near die corner. In Control and Underfill B samples cracks both vertical and parallel to die edge were present. Underfill B sample had more cracks than other samples, although the samples showed longer average lifespan.

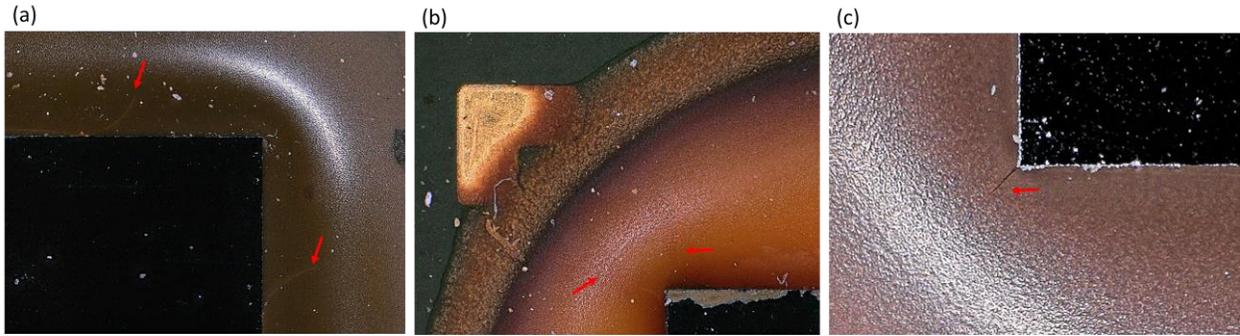


Figure 9. Cracks on underfill fillets after 4250 cycles, (a) Control underfill, (b) Underfill A, and (c) Underfill B.



Figure 10. Cracks on underfill fillets after 4250 cycles with 85°C/85%RH preconditioning (a) Control underfill, (b) Underfill A, and (c) Underfill B

Figure 11 and Figure 12 shows CSAM images of failed samples, after 4250 cycles of single zone thermal cycling. The bright area indicates underfill voids and delamination. In our previous study using ceramic substrate, underfill fillet cracked at the longest fillet and the crack propagated to flip chip bumps located at the edge of the die [7]. In the current study, such direct correlation between fillet cracking and flip chip bump cracking was not observed. Instead, underfill delamination showed more clear correlation with flip chip bump cracking. Figure 13 shows cross-sectional images of solder bumps in the sample shown in

Figure 11 (a). The underfill delamination propagated through the flip chip bump at the corner and reached the 5th bump from the corner. The underfill B samples, which had the longest thermal cycling life, had far less delamination although it had more fillet cracks than other types of samples.

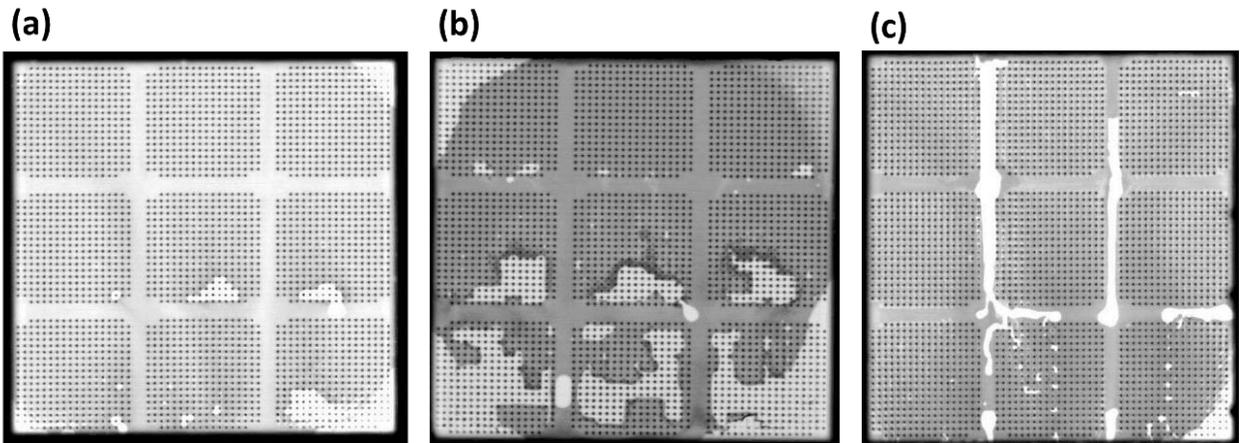


Figure 11. CSAM images of failed 15x15mm samples after 4250 cycles of thermal cycling, (a) Control underfill, (b) Underfill A, and (c) Underfill B.

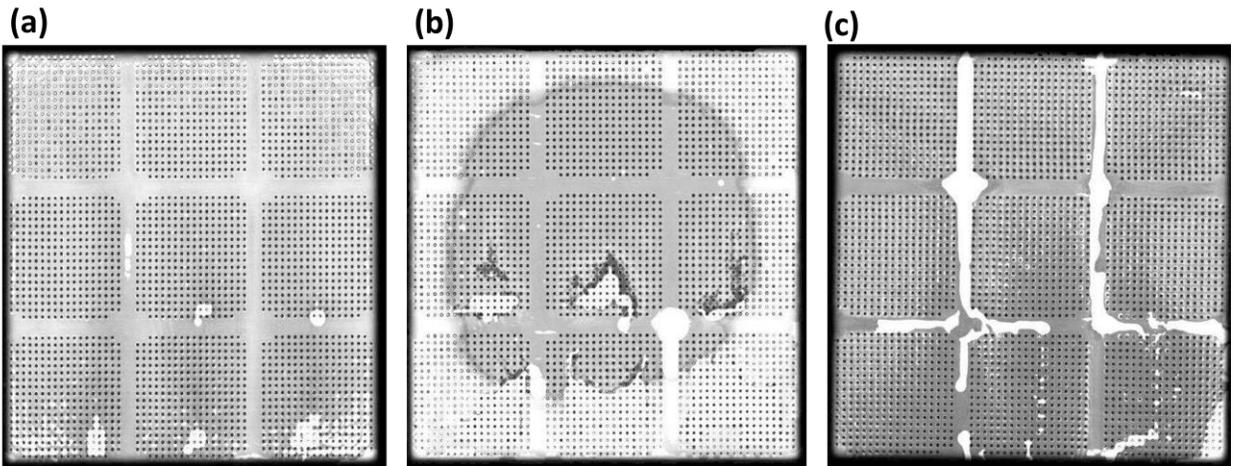


Figure 12. CSAM images of failed 15x15mm samples with 85°C/85%RH preconditioning after 4250 cycles thermal cycling, (a) Control underfill, (b) Underfill A, and (c) Underfill B.

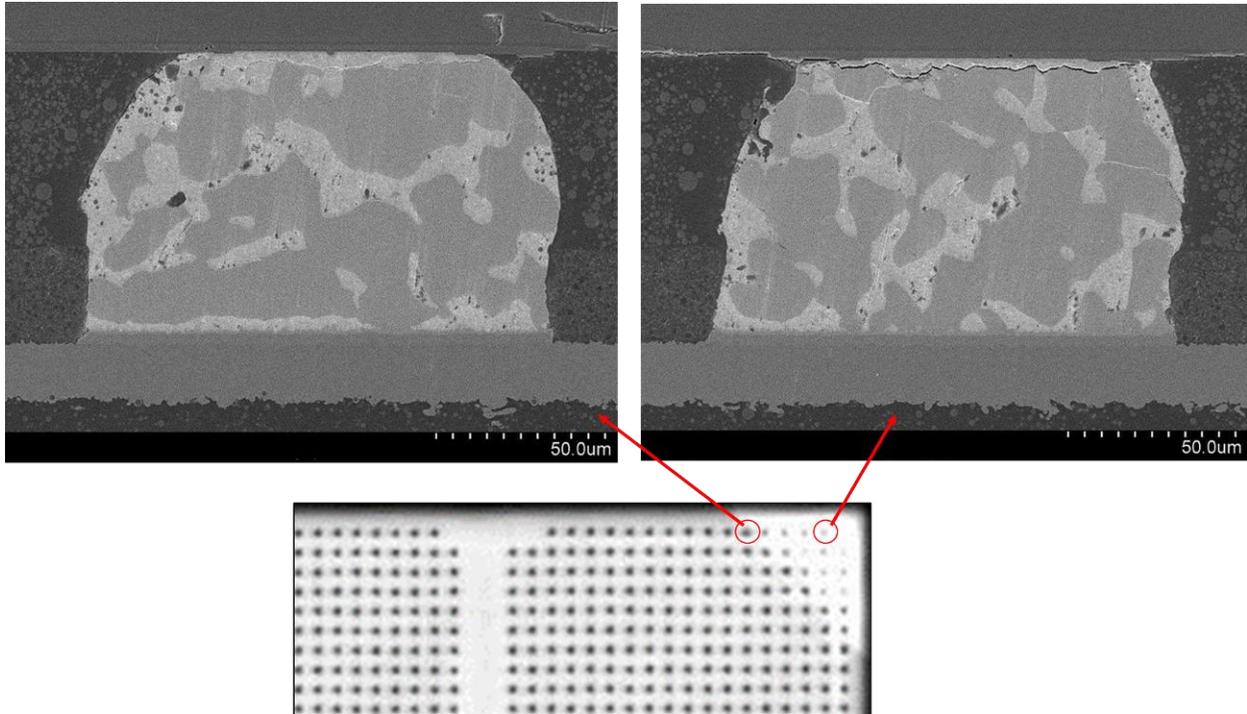


Figure 13. Cross-section images of flip chip bumps with respect to the underfill delamination area in a CSAM image

Some samples passed ohmmeter test after 4250 cycles. The survived samples also had underfill fillets cracks. However, the delamination was minimal in the survived samples. Figure 14 is CSAM images of underfill B samples passed ohmmeter test after 4250 cycles, showing there is almost no delamination. Figure 15 shows cross-sectional images of solder bumps in the sample shown in Figure 14 (a). A microcrack was observed from a solder bump adjacent to an underfill void, as shown in Figure 15. It is possible that this sample generated false pass during the probing at room temperature; one of the bumps along the void may have a microcrack spanning across the entire bump, which can open up at temperatures and close at the ambient temperature.

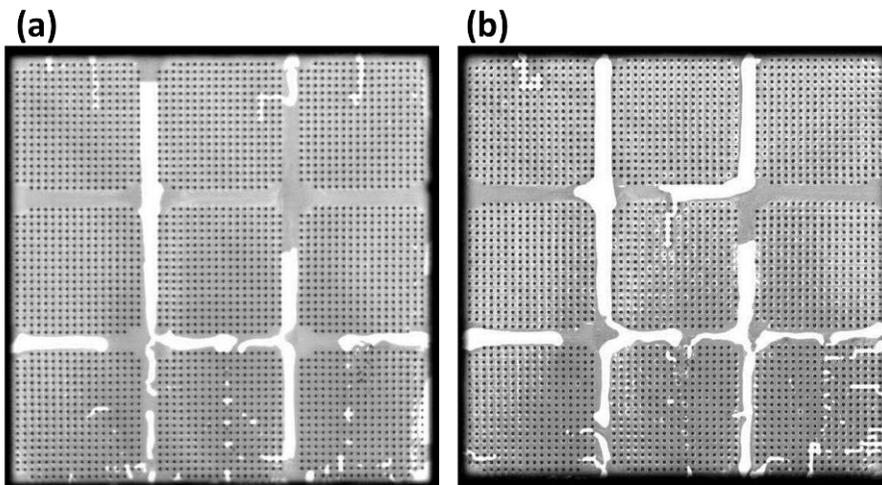


Figure 14. CSAM images of 15x15mm underfill B samples surviving after 4250 cycles thermal cycling, (a) without preconditioning and (b) with 85°C/85%RH preconditioning.

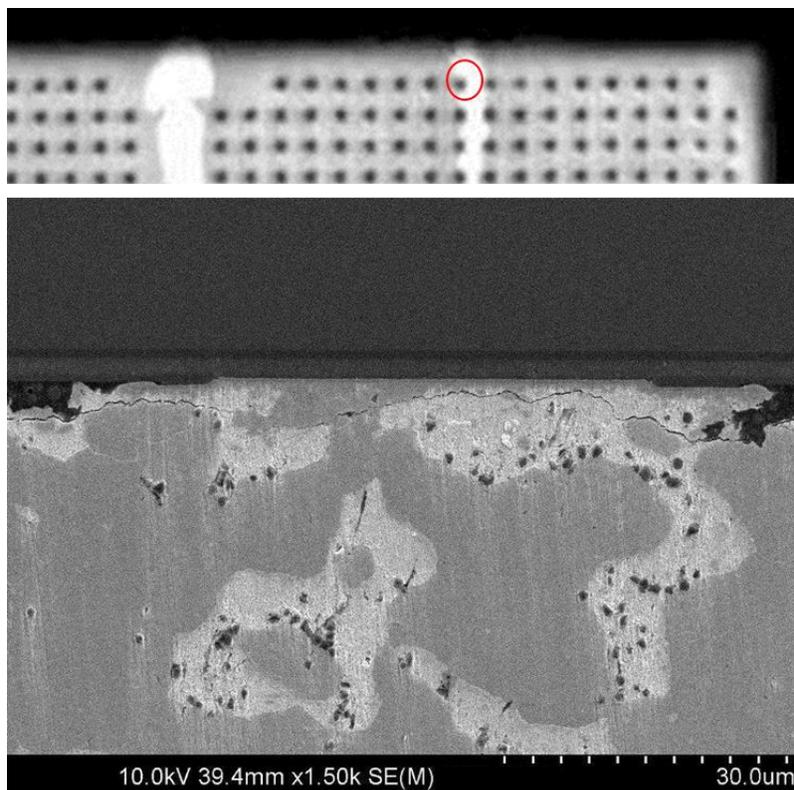


Figure 15. Cross-section images solder bumps near the underfill void of the sample shown in Figure 15 (a).

3.2 High temperature storage test results

Table 10 summarizes number of dies failed during high temperature storage (HTS) tests. The high temperature storage tests were done at 125 and 150°C. Since high temperature storage failure mainly occurs due to interdiffusion between bond pad metal and the solder bump, the high temperature storage life depends on factors related to interdiffusion, such as temperature, solder composition, and bond pad metallization configuration. However, our tests showed different HTS lives according to die size and underfill material, which is not related to diffusion. At this moment, it is not clear what caused such differences in the HTS life. One possible explanation is lot-to-lot variation between samples.

Table 10. Summary of high temperature storage test results. Continuity of the samples were tested every 250 hours.

Temperature	Underfill	Die size (mm)	Continuity test results up to 4250 hours, measured every 250 hours. 6 samples per each condition.
125°C	Control	5x5	0 failure
		15x15	
	A	5x5	
		15x15	
	B	5x5	
		15x15	
150°C	Control	5x5	1 failure at 750 hr. 5 failures at 1000 hr.
		15x15	3 failures at 1250 hr. 1 failure at 1500 hr.
	A	5x5	6 failure at 1000 hr.
		15x15	0 failure
	B	5x5	6 failures at 750hr
		15x15	0 failure

3.3 Comparison of thermal cycling reliability between class-Y samples and organic substrate samples.

As the main purpose of this task was to assess the reliability of organic flip chip in comparison to class-Y packages, the samples had the same die size and foot print as the sample tested during the FY13 task [7]. Table 11 compares -55/125 dual zone thermal cycling reliability between Class-Y and organic flip chip 15x15mm die samples. Depending on the underfill, the organic substrate sample showed comparable or better reliability than the class-Y sample. The first failures out of 8 samples in underfill A and B samples were detected after 2000 and 2250 cycles, respectively. This level of thermal cycling life is sufficiently beyond typical space parts qualification condition, since Cobham’s Package Integrity Demonstration Test Plan (PIDTP) for class-Y package targeted for 1000 cycles at MIL-STD-883 Test Method 1010 condition B [17]. As for the concerns from non-hermeticity, the underfill B showed exceptionally good resistance against moisture exposure. These results suggests that organic flip chip packages are reliable enough for space applications.

Table 11. Comparison of -55/125 thermal cycling life between class-Y and organic flip chip samples.

Sample	Condition	Weibull Life	Weibull Slope	Weibull Fit R2
Class-Y sample	Control underfill, No preconditioning	3629	6.3	0.96
	Control underfill, Moisture loaded.	2438	7.5	0.97
Organic substrate sample	Control Underfill	1822	1.15	0.91
	Underfill A	3927	3.92	0.98
	Underfill B	6608	2.46	0.93
	Moisture loaded Control UF	All failed after 250 cycles.		
	Moisture loaded UF A	376	4.04	0.60
	Moisture loaded UF B	Not enough failure to determine Weibull life. 1 failed after 2250 cycles.		

4.0 SUMMARY AND RECOMMENDATIONS

The test results in the current task indicates organic flip chip packages can be as reliable as class-Y packages. The test results shows that the underfill plays a critical role in the reliability of the organic flip chip packages, which is in line with the fact that historically the underfill was the enabling technology for organic flip chip packages.

Since underfill is critical for the package reliability, mil-std-38535 requirements for organic flip chip packages should be structured to adequately reflect underfill's reliability in the PIDTP. Additionally, the parts manufactures should develop robust supplier audit, quality control, and process/equipment qualification plans for underfill.

The current study mainly focused on the reliability of flip chip solder joints in organic packages. The reliability of microvias and traces of organic substrate will be studied elsewhere.

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