National Aeronautics and
Space Administration

High Performance Spaceflight Computing (HPSC)

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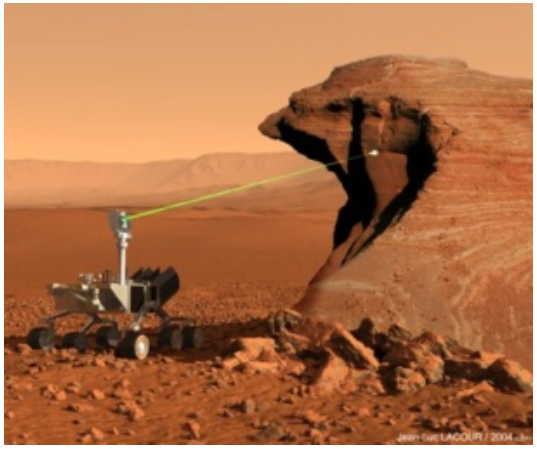
Background
The Problem – The Solution

The Problem

- NASA and USAF require High Performance Space Computing (HPSC) for multiple mission applications associated with both robotic and human space exploration.
- As NASA and USAF consider advanced missions that require both an increase in throughput and wider variations in fault tolerance and power levels, the development of a new processor is needed.



The Solution

- This processor, termed “the chiplet” herein, is needed to provide orders of magnitude improvement in performance and performance-to-power ratio as well as the ability to dynamically set the power-throughput-fault tolerance operating point.

Background

- NASA has conducted a High Performance Space Computing (HPSC) study defining future spacecraft onboard computing needs.

- Several HPSC use cases were identified, broadly addressing both human spaceflight missions and robotic science. As shown below, these were categorized into
    - Vision-based algorithms with real-time requirements
    - Model-based reasoning techniques for autonomy
    - High rate instrument data processing

- Based on these requirements and other key performance parameters (including power/energy management, fault tolerance, programmability, interoperability, evolvability/extensibility, and cost), candidate computing architectures were evaluated. ***This evaluation established that a radiation-hardened, general purpose multi-core processor is best suited to address NASA's future onboard computing needs.***

NASA Flight Computing Drivers
as Derived from the Use Cases

Computation Category	Mission Need	Objective of Computation	Flight Architecture Attribute
Vision-based Algorithms with Real-Time Requirements	• Terrain Relative Navigation (TRN) • Hazard Avoidance • Entry, Descent & Landing (EDL) • Pinpoint Landing	• Conduct safe proximity operations around primitive bodies • Land safely and accurately • Achieve robust results within available timeframe as input to control decisions	• Severe fault tolerance and real-time requirements • Fail-operational • High peak power needs
Model-Based Reasoning Techniques for Autonomy	• Mission planning, scheduling & resource management • Fault management in uncertain environments	• Contingency planning to mitigate execution failures • Detect, diagnose and recover from faults	• High computational complexity • Graceful degradation • Memory usage (data movement) impacts energy management
High Rate Instrument Data Processing	High resolution sensors, e.g., SAR, Hyper-spectral	• Downlink images and products rather than raw data • Opportunistic science	• Distributed, dedicated processors at sensors • Less stringent fault tolerance

Background
NASA Commissioned Study

- Collaborative discussions with AFRL determined that many of NASA's future onboard computing needs have commonality with ARFL's future needs, and that a radiation-hardened, general purpose multi-core processor of the kind envisioned by NASA would also be relevant to AFRL.

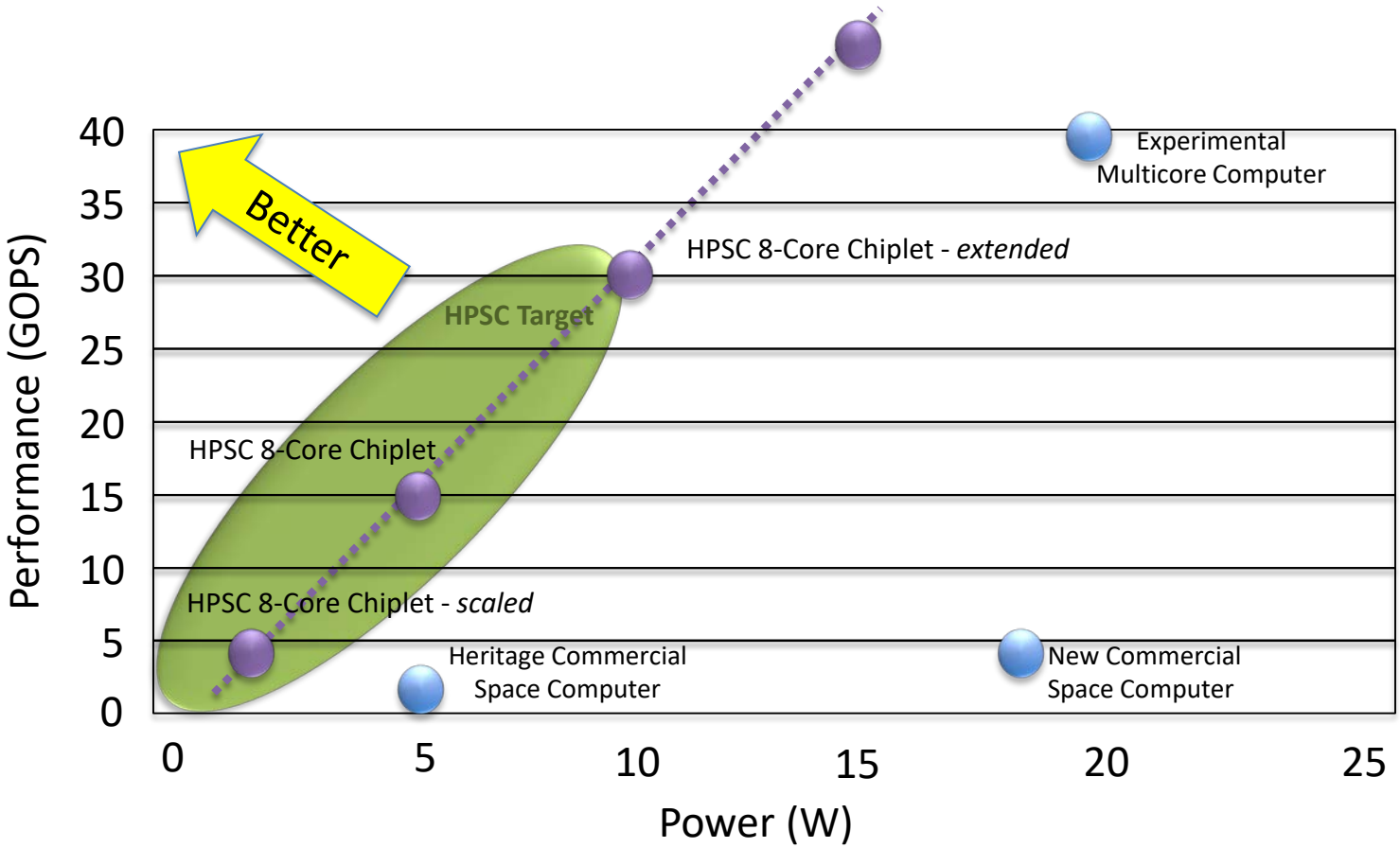
- NASA partnered with AFRL on a Next Generation Space Processor (NGSP) study.
    - This study, led by AFRL, engaged with industry to assess, in greater detail, AFRL's requirements, compare AFRL's requirements with NASA's previously defined detailed requirements, develop processor architectures that would satisfy the superset of NASA/AFRL requirements and evaluate these architectures against a set of government provided benchmarks.

Background
NGSP Study

- The NGSP study provided the government valuable guidance regarding the optimal architecture for a future spaceflight processing device:
  - The use of COTS IP (specifically ARM based IP) provides optimal power-to-performance, extensibility, evolvability, software availability, ease of use, and cost.
  - The use of Radiation Hard By Design (RHBD) standard cell libraries provides required radiation tolerance.
  - The augmentation of RHBD with higher level fault tolerance techniques improves reliability.
  - The use of the ARM A53 processor with its internal NEON SIMD is sufficient for most near term applications.
  - Heterogeneous multi-core architectures using multiple processor core types are not optimal.
  - Architectural flexibility such as the ability to turn on/off cache coherency and use of L3 cache, as well as the ability to dynamically depower unused cores of all sorts, including memory and I/O interfaces, is useful to enable setting of optimal power/performance/fault tolerance operating point.
- ***Based on these findings, the government team devised the HPSC "chiplet" concept.***

HPSC Game Changing Advance

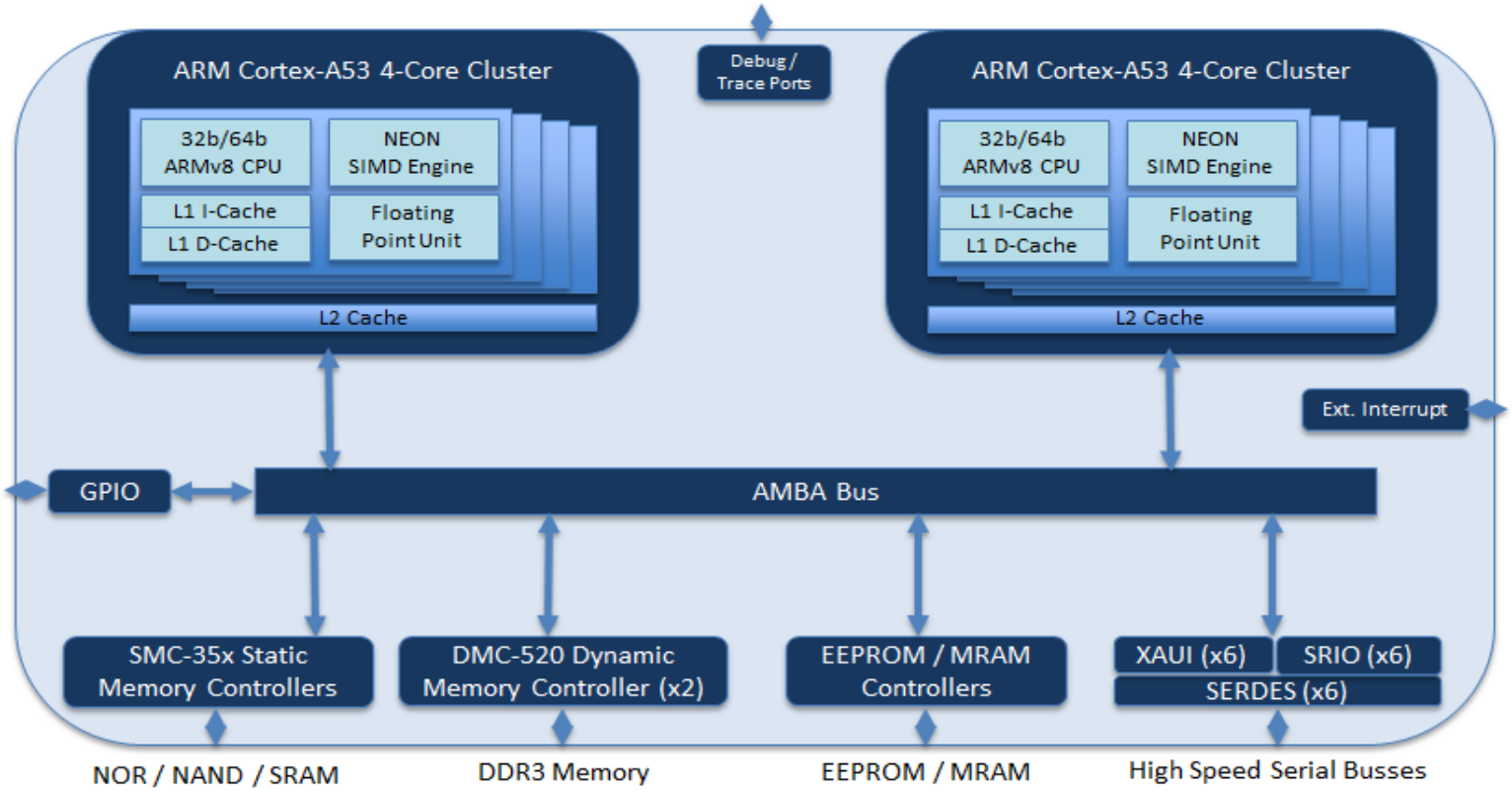
Proposed Performance vs. Power



HPSC will redefine the role of computing in space systems

HPSC Concept
8-Core Extensible Chiplet

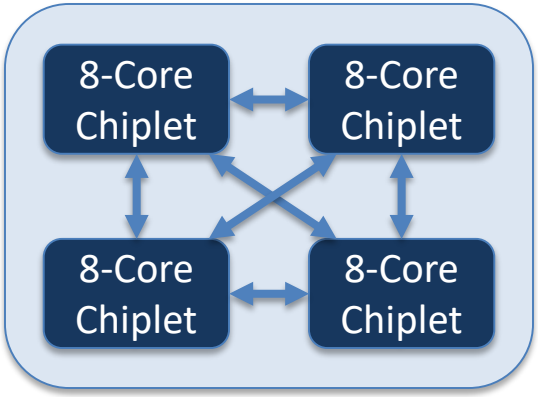
- **The chiplet concept leverages the COTS ARM A53 IP along with other COTS peripheral IP, and can meet NASA's performance, power, and radiation tolerance needs when implemented via existing RHBD technology.**



HPSC Concept
Extensibility

- Chiplet will also provide extensibility to allow the most demanding applications to be satisfied with “multiple-chiplet” systems, implemented either on a multi-chip module (MCM) or on a printed wiring board with multiple discrete chiplets.

- Multiple-chiplet systems can satisfy needs for requirements for increased processing bandwidth, or by needs for increased fault tolerance (i.e. multiple chiplets as separate fault containment regions).



HPSC Concept
Flexibility

- Viewed as an individual chiplet or as a system of multiple chiplets, a key requirement for HPSC is the flexibility to dynamically trade between processing throughput, power consumption, and fault tolerance to meet varying demands and priorities across multiple candidate missions and within the profile of each mission.

- System applications range from small cubesats to large flagship class missions, and can include:
    - Command & Data Handling, Guidance Navigation & Control, Communications
    - Human assist, Data representation, Cloud computing
    - High rate, real time sensor data processing
    - Autonomy, Science processing

HPSC Concept
Software Infrastructure

- The software infrastructure for the HPSC chiplet will support both symmetric and asymmetric processing, and support both real-time operating systems and Unix/Linux based parallel processing.

- The software infrastructure will also support hierarchical fault tolerance, ranging from single chiplet small mission to multi-chiplet highly redundant human missions.

- These advantages could come at the cost of increased hardware and software complexity. As software development and verification is a major cost driver for missions, this increased complexity has the potential to significantly increase cost for future NASA missions.

- NASA will separately develop <u>middleware software</u> providing machine management for multicore processing devices.
    - Resides between the application layer and the operating system to provide intelligent resource, fault, and power management.

HPSC Status

- **Industry Day held at Goddard Space Flight Center on 10/22/2015**
  - NASA (GSFC, JPL) and Air Force Research Lab hosted
  - 13 members of industry were present
- **Request for Proposal released on 6/20/2016**
  - Proposals currently under evaluation
- **HPSC Chiplet will be available for flight qualification in March 2020**

Questions?