Japan Aerospace Exploration Agency (JAXA)
The 29th Microelectronic Workshop (MEWS29)
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National Aeronautics and
Space Administration

Challenges of Adapting Next Generation Microelectronic Devices for Use on NASA Missions

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Atlas V Clearing the Tower in 2011—It Arrived at Jupiter This July

The United Launch Alliance Atlas V-551 launch vehicle carrying NASA's Juno planetary probe, its motors blazing, is off to a roaring start on its five-year journey to Jupiter from Space Launch Complex 41 on Cape Canaveral Air Force Station in Florida. Liftoff was August 5, 2011. Controllers completed insertion into Jupiter orbit on July 4, 2016

Photo credit: Courtesy of Scott Andrews

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- **Thank you Suzuki-san for your invitation. It's always a great pleasure to visit Tsukuba.**
- **Congratulations on the 29th anniversary of the MEWS Workshop!**
- **JAXA is our valued partner in NASA Electronic Parts Assurance Group (NEPAG) activities.**

Introduction

- This talk is about challenges of adapting next generation microelectronic devices for use on NASA missions.
- Advanced technologies provide lower power, higher performance, more functionality, and smaller packages.
- But, there are many challenges, tighter budgets, constrained workforce, and shorter schedules being some of them.
- NASA supports a very wide spectrum of space missions/programs ranging from smallsats/cubesats to flagship missions such as Juno and the planned Europa mission. The success of each mission is important.
- As part of NEPAG, we work with manufacturers and the space parts user community to develop/evaluate new space products.
- The following pages will discuss some of the issues and related activities.

Adapting Next Generation Technology is a Multi-pronged Effort

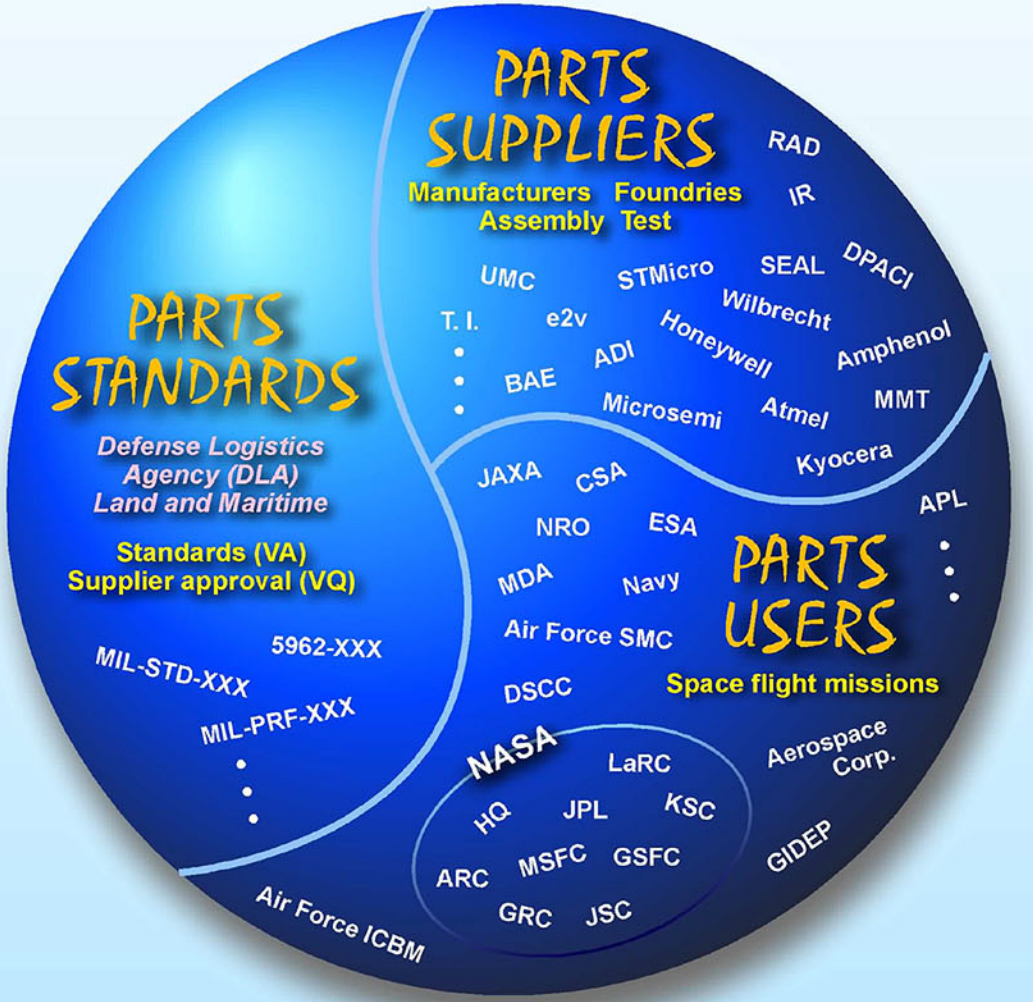
- **New Technology Evaluations**
  - **There are NEPP (NASA Electronic Parts and Packaging) funded evaluations**
  - **NEPP also joins hands with other organizations. For example,**
    - **Working with the Navy Crane (see write up in the latest NASA *EEE Parts Bulletin*)**
    - **Forming groups to understand advanced devices**
      - **Hold periodic telecons**
- **The JC-13 Effort**
  - **About two years back, JC-13 created a new committee, JC-13.7**
    - **JC-13.7 charter is to look into next generation technologies**
      - **List of top candidates**
        - **SiC, GaN (jointly with JC-13.1)**
        - **Copper bonds (with G-12 COTS/PEMs)**
        - **2.5D and 3D microcircuits (with G-12)**
    - **What would it take to infuse new technologies into QML standards**
      - **Identify the gaps**
    - **The JC-13.7 meets three times a year (same time as other JC-13 and G-11/G-12)**
    - **It is supported by NASA, JAXA among others**

Adapting Next Generation Technology is a Multi-prong Effort (Cont.)

- **Preparing to embrace advanced technologies**
  - **Continually Improving the Existing Infrastructure**
    - **The role of Microcircuits Qualifying Activity (QA)**
    - **QML Classes**
      - **Is the current set of Q, V, and Y sufficient to cover new devices?**
    - **Specs and Standards**
      - **Bring them current (more details later)**
    - **Some of the side issues**
      - **Handling/packaging/ESD (electrostatic discharge)**
      - **Burn-in of high speed devices**
      - **Usefulness of the Qualified Products List (QPL) program**
        - **QPLS (space grade) crystal oscillators Limited resources**
        - **Workforce**
        - **Budgets**

Space Parts World

NEPAG helps to Develop/Maintain Standards for Electronic Parts

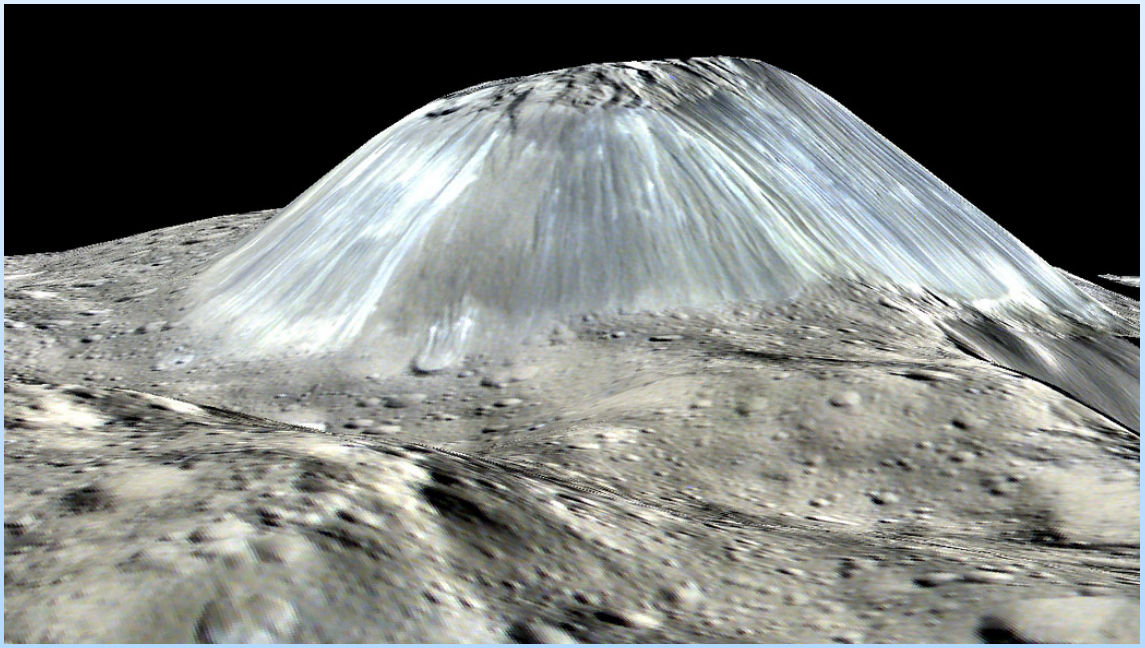


The parts users and standards organizations work with suppliers to ensure availability of standard parts for NASA, DoD, and others. ***For Space microcircuits, DLA, NASA/JPL (S. Agarwal*) and the U.S. Air Force / Aerospace Corp. (L. Harzstark) form the Qualifying Activity (QA).***

**Also Systems, Standards and Technology Council (SSTC) G-12 Vice-Chair.*

NASA and JC-13

- **NASA is an active participant in many JC-13 activities.**
- **Some of the JC-13 Task Groups were started at NASA's request.**
  - **Example: Electronic Parameters and Burn-in Standardization.**
- **The newly started New Technology initiative (JC-13.7) provides an opportunity to look ahead:**
  - **Identify new technologies**
  - **Develop a path for their infusion into military and space.**



Ceres' Mountain Ahuna Mons: Side View

Ceres' lonely mountain, Ahuna Mons, is seen in this simulated perspective view. The elevation has been exaggerated by a factor of two. The view was made using enhanced-color images from NASA's Dawn mission.

NASA and SAE SSTC G-12*

- NASA is an active participant in many G-12 activities.
- When requested, NASA has led the G-12 Task Groups.
  - Example: Infusion of new technology into DoD standards, the Class Y initiative.
- With the appointment of Shri Agarwal as the Vice-Chair of G-12, NASA is helping run the organization.
- Just recently, NASA was asked to take over the G-12 Space subcommittee as its Chair. In addition to the regular presentations from international agencies, two invited talks were given on ESD and the state of crystal oscillators
- * SAE = Society of Automotive Engineers
  SSTC = Systems, Standards and Technology Council
  G-12 = Solid State Devices

Partnering with Industry Groups

- **JEDEC JC-13 (Manufacturers), and**
- **SAE SSTC G-11/G-12 (Users)**

JEDEC JC-13

JC-13	Solid State Devices for Government Products
JC-13.1	Discrete Semiconductors for Government Products
JC-13.2	Microelectronics for Government Products
JC-13.4	Radiation Hardness
JC-13.5	Hybrids and MCMs for Government Products
JC-13.7	New Electronic Device Insertion for Government Products

SSTC G-11/G-12

SAE SSTC G-11	Users of Passive Components
SAE SSTC G-12	Users of Solid State Devices

G-12 Management:

Chair – A. Touw

Vice Chair – S. Agarwal

Joint JEDEC and G-12 meetings are held 3 time a year. NEPAG is an active participant in those meetings. NEPAG's Shri Agarwal was appointed as the vice chair of G-12.

Infusion of New Technology into MIL Standards

Columbus, Ohio

FINAL
MEETING SCHEDULE

September 2016

NEPAG MTG.

Day	Room	7:30 AM	8:00 AM	9:00 AM	10:00 AM	11:00 AM	12:00 PM	1:00 PM	2:00 PM	3:00 PM	4:00 PM	5:00 PM	6 PM	7PM
Mon 9/12	Hayes C					PEMs should go to 19500 App J		G-12 Derating	G-12 Wear-out and Profiles	G-12 PEM TG Qual and Screening Flow	G-12 Plastics / PEMS Subcommittee	G-12 Terrestrial & Avionics Subcommittee		
	Hayes D			JC-13.1 Technical 750 Test Method Review		JC-13.1 MIL-PRF-19500 Appendix J		MIL-PRF-19500R						
	Hayes E						JC-13 ExCo Mtg. (by invitation) *	JC-13.5 PI / QML Task Group						
Day		7:30 AM	8:00 AM	9:00 AM	10:00 AM	11:00 AM	12:00 PM	1:00 PM	2:00 PM	3:00 PM	4:00 PM	5:00 PM	6 PM	7PM
Tues 9/13	Hayes C		JC-13.1/JC-13.7/G-12 New Technology Appendix in 19500	JC-13.1 GaN Working Group	JC-13.1/JC-13.7/G-12 SiC Tech Insertion	JC-13.7 Copper Wire Bonds		JC-13/G-12 Joint Meeting	JC-13.2 Underfill Evaluation	JC-13.7 >2D Packaging	JC-13 Leak Rate/RGA Issues in 883 and 750	G-12 & G-11 Counterfeit Mitigation Subcommittee		
	Hayes B	New Member Orientation	JC-13.2 Elec Parameters & B/I Stand.		JC-13.2 JEP121	JC-13 X-Ray Seal Voids				JC-13.1 should attend >2D	JC-13.1 should attend leak rate			
	Hayes D		JC-13.5 TG158 - Element Evaluation		TG 176 TM2009 Glass Visual				JC-13.5 TG172 QML Reqs.	JC-13.5 QML of Class H vs. K				
	Hayes A		JC-13.4 Subcommittee Meeting						JC-13.4 Extended Session	ASTM Meeting				
Day		7:30 AM	8:00 AM	9:00 AM	10:00 AM	11:00 AM	12:00 PM	1:00 PM	2:00 PM	3:00 PM	4:00 PM	5:00 PM	6PM	7PM
Wed 9/14	Hayes C		Joint JC-13.2/G-12 Meeting		G-11 / G-12 Connector Stop Ship and Unapproved Sources of Supply			Joint JC-13.1/G-12 Meeting		Joint JC-13.5/G-12 Meeting		G-12 & G-11 Space Subcommittee		
	Hayes D		JC-13.5 Meeting					JC-13.5 Meeting						
	Hayes A		Joint JC-13.1/JC-13.4 Meeting		G-12 Radiation RHA SC			G-12 Radiation RHA Subcommittee				Informal Get Together for Outgoing Chairs and Friends No special invitation needed! (Cash Bar)		
	Hayes E		G-11 Committee Meeting		G-11 should go to joint G-11/G-12			G-11 AEM Tech Talk	G-11 Commmittee Meeting					
Day	Room	7:30 AM	8:00 AM	9:00 AM	10:00 AM	11:00 AM	12:00 PM	1:00 PM	2:00 PM	3:00 PM	4:00 PM	5:00 PM	6PM	7PM
Thurs 9/15	Hayes C		Joint JC-13.7/G-12 New Electronic Device		Tech Talk Qualification and Testing for Automotive Product	JC-13 ExCo Meeting (by invitation) *		JC-13 General Session						
	Hayes D		G-11 Committee Meeting											

Chaired by NASA

* Attended by NASA. NASA is G12 Vice Chair.

A Typical Challenge in a Frequent Dialogue

- **Design Engineer:**
  - **Why can't I use the product as soon as it is announced by the manufacturer?**
- **Parts Engineer:**
  - **The part is not available as a standard space product.**

New Technology Qualification
Some Major Activities

- **Technical support to the Defense Logistics Agency (DLA) audits of supply chain:**
  - **Wafer foundry**
  - **Wafer bumping**
  - **Assembly**
  - **Column attach**
  - **Proper shipping/handling/ESD precautions become important**
    - **Per unit costs approaching $100k**
    - **NASA ESD surveys**
      - **NASA *EEE Parts Bulletin*s**

- **Qualifying Activity (QA) Reviews/Approvals:**
  - **NASA is part of the QA**
  - **Manufacturers to perform qualification as required in MIL-PRF-38535.**
    - **For example, 4000-hour life test**
  - **DLA and manufacturers to develop standard microcircuit drawing (SMD)**
    - **Update existing boiler plate to accommodate new features - example on next page**

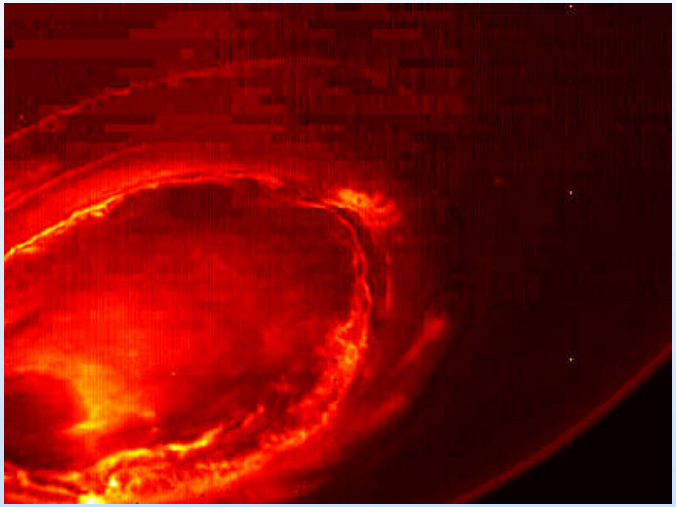
NEPAG DLA Audits

CHANGING LANDSCAPE

A New Trend – Example of Supply Chain Management

(Typical steps in the supply chain flow; all entities used must be approved)

Die design	Company A
Wafer fabrication	Company B
Package design & manufacturing	Company C
Wafer lap and dice	Company D
Assembly	Company E
CGA column attach Solderability	Company F
Screening/electrical/package tests	Company G
Complete electricals per SMD	Company H
Internal water vapor content	Company I
Radiation testing	Company J



Juno's View of Jupiter's Southern Lights

This infrared image gives an unprecedented view of the southern aurora of Jupiter, as captured by NASA's Juno spacecraft on August 27, 2016.

Standards Today

- **Past Standards:**
  - **Were written to accommodate multiple sources.**
  - **Minimal flexibility was allowed.**

- **Current Standards:**
  - **Written to infuse new technology.**
    - **Addressing complexities at both die and package levels**
  - **Introduced PIDTP (Package Integrity Demonstration Test Plan) for Classes V and Y**
    - **Allowing manufacturers to build their products the best way they know how**

NASA's Involvement in Developing New Space Products

- With the Defense Logistics Agency (DLA) and the Aerospace Corporation, NASA participates in the review and approval of new space products:
  - Standard Microcircuit Drawings (SMDs)
  - Characterization and qualification data per Appendix H of MIL-PRF-38535 (for the monolithics)
- During the fiscal year 2016, a total of 16 microcircuit SMDs were approved for release. The mix of new product types included:
  - Digital-to-analog converter from Cobham
  - Analog-to-digital converters from TI and ADI
  - 16-bit and 32-bit switches from Cobham
  - DC/DC converters from VPT, International Rectifier, and Crane Electronics
  - Operational amplifiers from ST Micro and ADI
  - MOSFET drivers from ST Micro
  - Configurable logic gates from Cobham
  - Instrumentation amplifier from ADI

Standard Microcircuit Drawings (SMDs)

- DLA-VA responsible organization
- Supposed to be a self contained document
- Table I. In particular delta parameters
- Table IIa. Electrical measurements
- Table IIb. Delta measurements
- More functional/operational details added in SMDs, as applicable
  - e.g., Power-supply sequencing
- Per manufacturers, there is a strong demand for space products

An Example of SMD Boiler Plate Update

TABLE IIA. Electrical test requirements.

Line Number	Test requirements	Subgroups (in accordance with MIL-PRF-38535, table III)	
		Device class Q	Device class V
1	Interim electrical parameters (see 4.2)	1,2,3,7,8A, 8B,9,10,11 1/	1,2,3,7,8A, 8B,9,10,11 1/
2	Static burn-in I and II (method 1015)	Not required	Required
3	Same as line 1	- - -	1, 7 Δ 1/ 2/
4	Dynamic burn-in (method 1015)	Required	Required
5	Same as line 1	1, 7 Δ 1/ 2/	1, 7 Δ 1/ 2/
6	Final electrical parameters	1,2,3,7,8A,8B,9, 10,11 1/	1,2,3,7,8A,8B,9, 10,11 1/
7	Group A test requirements 3/	1,2,3,4,7,8A,8B,9,10 ,11 4/	1,2,3,4,7,8A,8B,9, 10,11 4/
8	Group C end-point electrical parameters 3/	1,2,3,7,8A,8B, 9,10,11 Δ 2/	1,2,3,7,8A,8B, 9,10,11 Δ 2/
9	Group D end-point electrical parameters 5/	2,3,8A,8B	2,3,8A,8B
10	Group E end-point electrical parameters 3/	1,7,9	1,7,9
11	Column attach 6/	1,7,9	1,7,9

- **For Flip-chip column attach**
  - **Add room temperature electricals (subgroups 1, 7, 9) after column attach – step 11 above**

Electrical Characteristics

TABLE IA. Electrical performance characteristics.

Test	Symbol	Conditions $-55° \le T_C \le +125°C$ $1.7\ V \le V_{DD} \le 1.9\ V$ $1.4V \le V_{DDQ} \le V_{DD}$ Unless Otherwise Specified 1/ 2/ 3/	Group A Subgroups	Device Type	Limits		Units
					Min	Max	
Output HIGH Voltage 4/	V_{OH1}	I_{OH} = -0.1 mA, 50 ohm impedance	1, 2, 3	All	V_{DDQ} -0.20	V_{DDQ}	V
Output LOW Voltage 5/	V_{OL1}	I_{OL} = 0.1 mA, 50 ohm impedance	1, 2, 3	All	V_{SS}	0.20	V
Output HIGH Voltage	V_{OH2}	I_{OH} = -2.0 mA, 50 ohm impedance	1, 2, 3	All	$V_{DDQ}/2$ - 0.12	$V_{DDQ}/2$ + 0.12	V
Output LOW Voltage	V_{OL2}	I_{OL} = 2.0 mA, 50 ohm impedance	1, 2, 3	All	$V_{DDQ}/2$ - 0.12	$V_{DDQ}/2$ + 0.12	V
Input HIGH Voltage 6/	V_{IH}		1, 2, 3	All	V_{REF} +0.1	V_{DDQ} +0.3	V
Input LOW Voltage 6/	V_{IL}		1, 2, 3	All	-0.3	V_{REF} -0.1	V
Input Reference Voltage 6/ 7/	V_{REF}	Typical value = 0.75 V	1, 2, 3	All	0.68	0.95	V
Input Leakage Current	I_X	$GND \le V_I \le V_{DDQ}$	1, 2, 3	All	-20	20	uA
Output Leakage Current	I_{OZ}	$GND \le V_I \le V_{DDQ}$, output disabled	1, 2, 3	All	-20	20	uA

- **Encircled are the delta parameters**
- **The limits should be split into room-temperature limits and over-temperature limits**

New Technology Flip-chip Devices: Underfill Status Update

- **Use of Underfills**
  - **The use of underfill material enhances reliability of flip-chip packages.**
  - **MIL-PRF-38535K requires flip-chip devices to meet the underfill requirements specified in MIL-STD-883, Test Method 5011.**

- **Activities**
  - **NASA *EEE Parts Bulletin* on underfills.**
  - **Defense Logistics Agency (DLA) Engineering Practice (EP) study**
  - **Discussion in Underfill Task Group**

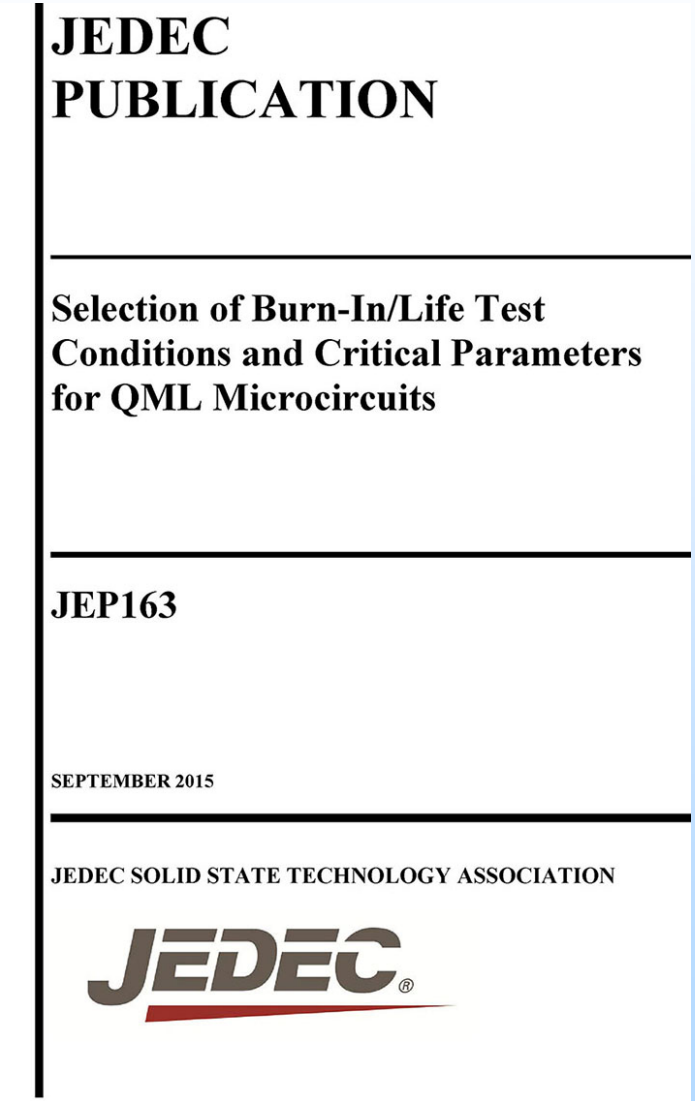
- **Status**
  - **The specification issue was resolved at the September 2016 meeting.**
  - **Task Group is now closed.**

Example of Updated Requirements, Microcircuits Burn-in (BI)

(NASA Inputs 12 September 2016)

- **Status**
  - **Task Group chaired by B. Rhoton**
  - **Published Guideline document JEP163.**
  - **Task Group is still open to address new concerns.**
  - **DLA's Engineering Practice (EP) study on BI is complete.**
  - **Task group is still open**

- ***A New Concern***
  - **BI of high-speed devices (frequencies approaching gigahertz range)**
    - **What about hot spots on the die? For example, SERDES in an FPGA may run much hotter than the rest of the die.**
      - **Practically no data on hot spots (no verification of models)**
    - **Ambient vs. case vs. junction temperature**


JEDEC PUBLICATION

Selection of Burn-In/Life Test Conditions and Critical Parameters for QML Microcircuits

JEP163

SEPTEMBER 2015

JEDEC SOLID STATE TECHNOLOGY ASSOCIATION

Dual-Use Technology

- ***Basically an infusion of commercial monolithic microcircuits into DoD system.***
  - ***Rad hard by design 45nm CMOS microelectronics technology (BAE Systems, built at IBM foundry)***
  - ***Adding their unique processing steps to the existing processes, e.g. MRAMs being offered by Aeroflex and Honeywell (done in collaboration with Everspin)***
  - ***Upscreening selected products from commercial portfolio (Analog Devices)***

- ***This has resulted in paradigm changes. An example follows:***
  - ***Not all parts are specified over the full military temperature range, –55°C to +125°C. Many of them call out –40°C to +110°C operating temperature range. These differences are now clearly shown in the standard microcircuit drawings (SMDs). However, there are no guidelines for BI of these devices. (Per notes 3/ and 4/ of the regression table, doing BI at temperatures lower than TA=125°C is not allowed for monolithics.)***
  - ***It is unclear what assumptions went into generating the numbers.***

MIL-STD-883J
w/CHANGE 1

TABLE I. Burn-in time-temperature regression. 1/ 2/ 3/ 4/

Minimum temperature T_A (°C)	Minimum time (hours)			Test condition (see 3.1)	Minimum reburn-in time (hours)
	Class level S	Class level B	Class level S hybrids (Class K)		
100	---	352	700	Hybrids only	24
105	---	300	600	"	24
110	---	260	520	"	24
115	---	220	440	"	24
120	---	190	380	"	24
125	240	160	320	A - E	24
130	208	138	---	"	21
135	180	120	---	"	18
140	160	105	---	"	16
145	140	92	---	"	14
150	120	80	---	"	12
175	---	48	---	F	12
200	---	28	---	"	12
225	---	16	---	"	12
250	---	12	---	"	12

1/ Test condition F shall be authorized prior to use and consists of temperatures 175°C and higher.
2/ For condition F the maximum junction temperature is unlimited and care shall be taken to ensure the device(s) does not go into thermal runaway.
3/ The only allowed conditions are as stated above.
4/ Test temperatures below 125°C may be used for hybrid circuits only.

METHOD 1015.10
26 February 2010

MIL-STD-883, Test Method 1005

MIL-STD-883J
w/CHANGE 1

TABLE I. Steady-state time temperature regression. 1/ 2/ 3/ 4/

Minimum temperature T_A (°C)	Minimum time (hours)			Test condition (see 3.5)
	Class level S	Class level B	Class level S hybrids (Class K)	
100		7500	7500	Hybrid only
105		4500	4500	"
110		3000	3000	"
115		2000	2000	"
120		1500	1500	"
125	1000	1000	1000	A -E
130	900	704	---	"
135	800	496	---	"
140	700	352	---	"
145	600	256	---	"
150	500	184	---	"
175		40	---	F
180		32	---	"
185		31	---	"
190		30	---	"

1/ Test condition F shall be authorized prior to use and consists of temperatures 175°C and higher.
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4/ Test temperatures below 125°C may be used for hybrid circuits only.

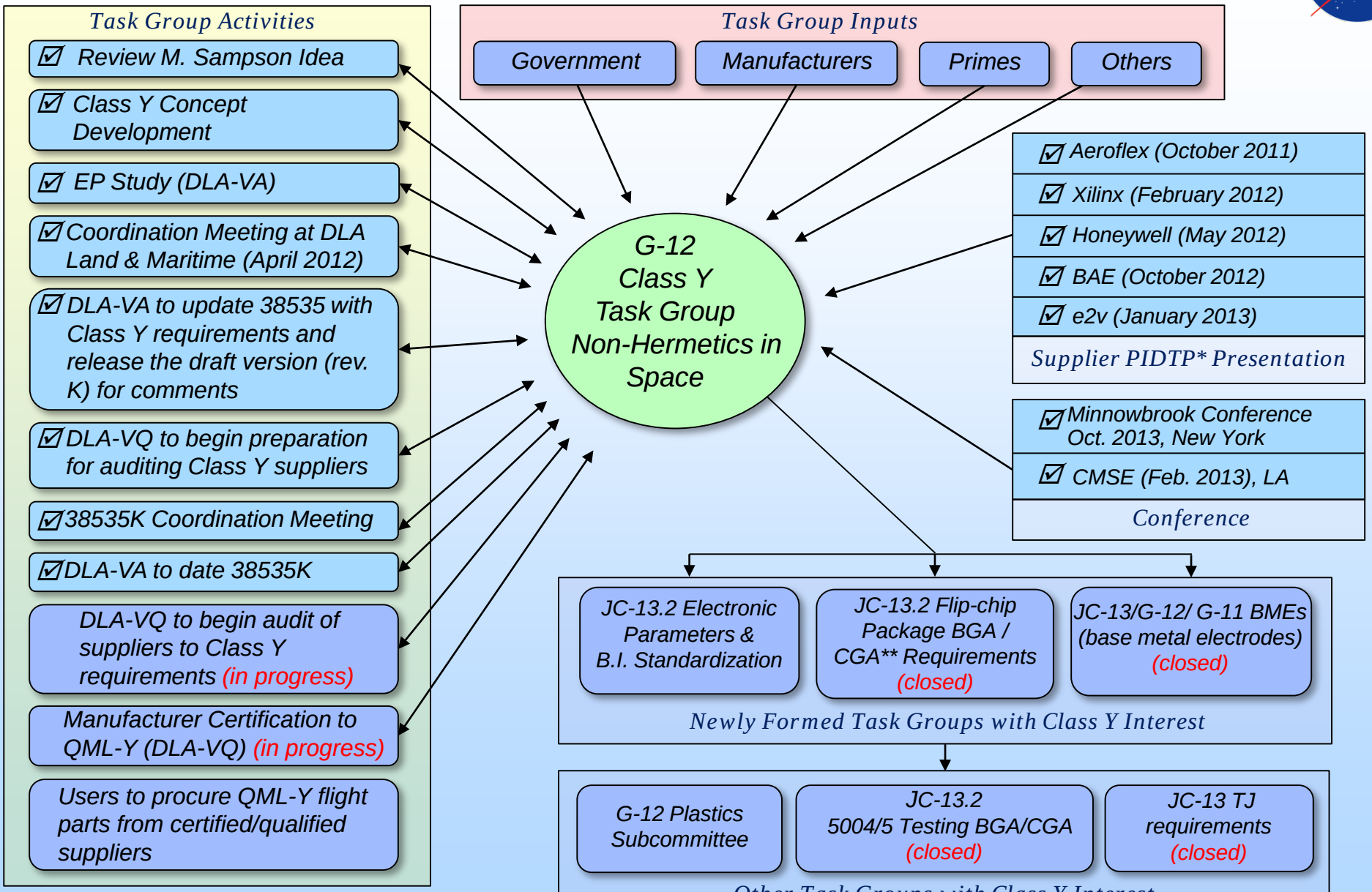
METHOD 1005.9
26 February 2010

- ***Life test below TA = 125°C not allowed for monolithic microcircuits.***

What if the Product Didn't Fit Any of the Existing Classifications? The "Class Y" Initiative

- Advances in packaging and device technology are happening rapidly.
- How do we enable space flight projects to benefit from the newly developed devices?
- For Xilinx Virtex-4 and -5 FPGAs (which are ceramic-based flip-chip nonhermetic parts), a new class was needed.
- NASA led a G-12 initiative, called Class Y, for infusing Xilinx Virtex-4 and -5 FPGAs and other similar devices into military/space standards.
- Such an effort must be coordinated with the suppliers and users.
- Need to address all aspects of packaging configuration.
- New test methods must be created and the existing standards updated as necessary.

Infusion of the New Class (Y) Technology into the QML System for Space



* PIDTP = Package Integrity Demonstration Test Plan
** BGA / CGA = ball-grid array / column-grid array

Class Y Certifications Activity

- **Column attach service providers**
  - **Six Sigma, Milpitas, CA**
  - **Micross, Crewe, UK**
  - **BAE Systems, Manassas, VA**
  -
- **Manufacturers**
  - **Cobham, Colorado Springs, CO**
  - **Honeywell, Plymouth, MN**
- **Planned**
  - **Xilinx, San Jose, CA**
  - **e2V, Grenoble, France**
  - **Cypress, San Jose, CA**

Artist's conception of the OSIRIS-REx spacecraft at Bennu asteroid

The OSIRIS-REx spacecraft was launched September 8 this year and is scheduled to arrive at asteroid Bennu in 2018. Once there it is to make observations and return a small sample by 2023. In this image, the solar arrays are raised into a "Y-wing" configuration prior to arm contact.

Signal Integrity Capacitors

- New technology high-speed devices require signal integrity capacitors
  - Commercial capacitors of base metal electrode (BME) construction were designed into the products
    - Tiny, low voltage
- A task group comprised of the manufacturers and the users developed a screening specification
- Status
  - The general specification MIL-PRF-32535 and a set of 10 slash sheets were released.
  - The slash sheets for the interdigitated capacitors (IDCs), used in Xilinx Virtex 5 FPGAs and other new devices, are being worked.

ESD - A New Concern from NASA

- ***Electro Static Discharge (ESD)***
  - ***MIL-STD-883, Test Method 3015***
    - ***Too old, long test times***
    - ***Needs to be revisited for new technology***
      - ***Smaller feature sizes, large number of contacts/pins, advancements in packaging (2D, 3D)***
    - ***883 vs JEDEC (3 zaps/pin vs 1 zap/pin, for HBM test)***
    - ***Equipment used to assemble /process parts/wafers need closer look – special talk at Space subcommittee meeting***
    - ***Generic issue; applies to all parts military/space (and COTS)***
  - ***MIL-PRF-38535***
    - ***Clarify requirements***
      - ***No specific ESD requirements for wafer foundries***
    - ***DLA is conducting their engineering practice (EP) study***
  - ***NASA EEE Parts Bulletin***
    - ***Special edition on ESD***
  - ***NASA ESD Surveys***
    - ***Conducted to bring awareness***

NASA *EEE Parts Bulletin*
Special Edition on Electrostatic Discharge (ESD)

- **Show 2-3 pages of the recently released Bulletin**

National Aeronautics and Space Administration

EEE Parts Bulletin

Electrical, Electronic, and Electromechanical

A periodic newsletter of the JPL/GSMS Assurance Technology Program Office (ATPO), NASA EEE Parts Assurance Group (NEPAG), and Section 514, of the Jet Propulsion Laboratory.

January–July, 2016 • Volume 8, Issue 1 (Published since 2009)

Special Edition on Electrostatic Discharge (ESD)

Damage from ESD is a major cost to the microcircuit industry in terms of time, money, and mission risk. We plan to release two issues. This first special issue deals with the need to upgrade specifications related to ESD and suggestions for better ESD practices wherever parts are manufactured, stored, or prepared for shipment. This issue also includes an article about partnering in radiation and reliability testing. The second special issue will describe examples of ESD-related problems.

Figure 1 is an example of subtle damage that may be caused by ESD.

EAG 5.0kV 10.5mm x15.0k SE(M) 3/16/2016 3.00um

Figure 1. An investigation into excessive current draw on an electronic component successfully isolated a short location using a relatively new infrared imaging technique called pulse sample thermography (PST). Deprocessing and subsequent layer-by-layer scanning electron microscopy (SEM) inspections identified a likely ESD silicon melt site at the active layer on a unique horizontal structure. Follow-up review with the manufacture noted this device to be very sensitive to ESD. The issue was attributed to mishandling, and a follow-up activity was initiated to review the ESD control rigor. (Figure courtesy of JPL Analysis and Test Laboratory.)

Upgrading ESD Control: Its Importance and Possible Strategies

A. Why Improved ESD Control Practices Are Crucial

Microcircuit pin counts have increased significantly in the last decade, particularly for communication and computing products. NASA and the space community are using 1752-pin counts, and higher counts are growing more common in the general market.

Current qualification standards were developed with typical pin counts in the twenties. Applying these old device testing standards to modern high-pin count products can cause severe problems. Testing times increase dramatically. Worse, wear caused by repeatedly stressing the same path and the increasing influence of tester parasitic losses (parasitics) can lead to false-positive failures.

1

urthermore, the landscape of microcircuit part production, handling, and shipping has changed radically. Because of the increased complexity of parts, the paradigm of a manufacturer shipping directly to a customer has largely given way to a highly dispersed production environment. Table 1 shows the most extreme possible result of such an environment. (Such extreme dispersion is more likely with new products such as flip chips.)

Table 1. An Extreme Example of possible dispersion of production and use for a microcircuit product.

Company	Operation/Use
Component Level	
A	Die design
B	Wafer fabrication
C	Wafer bumping
D	Package Design
E	Assembly
F	Column attach
G	Testing and screening
H	Radiation testing
I	Transport by a franchised distributor
J	User Inventory Operations
K	Kitting of upper-level assembly operations
Board Level and Above	
L	Board-level test and verification
M	Intermediate board-level assembly
N	Final box-level assembly
O	Placement of the box level assembly containing the part in a system (e.g., aircraft, spacecraft, or appliance)

Note: At board level and above (L-O), reduced ESD failures can be realized through upper-level design mitigation (usually EMI compliance and spacecraft charging mitigation) and also box-level handling processes. System level handling processes can also reduce occurrences (for example, shorting plugs and connector covers) for the integration and test phase of the electronics system.

It is important to recognize and fully address all the risk points to which ESD sensitive parts are subjected: from when they are fabricated and delivered from the original component manufacture's (OCM) site; through supply chain avenues to user inventories; then on to kitting and upper-level printed circuit board (PCB) level assembly, test and verification; and eventually to final box level assembly, test and final system level test. This is particularly important for handling, packing, and shipping of ESD Class 0 devices.

This article describes challenges of high pin-count ESD device testing, solutions, and possible future trends in the standardization of device testing. Some issues to consider include:

- What are the differences and the advantages vs. disadvantages of the MIL standards, the JEDEC standards, and other standards for potential use and/or which might influence the MIL standards?
- Do we want a standard for reducing the number of pin combinations required for testing?
- Would statistical pin testing be a good approach?
- How can the testing time be reduced without losing useful information (and significantly impacting the test data)?
- Should the MIL standards be expanded to include charged device model (CDM) testing?
- How do the new 2.5D and 3D configurations affect ESD testing?
- Are all three models (human body model, charged device model, and machine model) still valid?

We need to consider future trends when revising test standards. This issue is growing more important because the unit cost of contemporary devices are very high (and are growing costlier as more functionality is added), on the order of several tens of thousands of dollars per unit. Poor ESD environment for such products creates possibility of damage/ latent damage to them, both of which could be very expensive. Costs for implementing an ESD-prevention program are miniscule compared to the overall cost incurred in dealing with ESD damage.

The above concerns were presented by NASA representative Michael Sampson at the June 2016 G12 Space Subcommittee meeting. We proposed that the military documents that control the ESD requirements be reviewed and updated as a first step. As part of this update process, we suggest that DLA perform an engineering practice (EP) study on ESD as quickly as possible.

Eventually, these document changes will require review and coordination with associated reference documents from other organizations to bring consistency.

B. Existing ESD Control Requirements and Suggested Changes to Them

The Department of Defense has an extensive set of ESD requirements and related documents. In addition, several other standards organizations have existing ESD-control requirements documents. The listing below includes

2

what we might have individually accomplished. Examples of this effort are seen in several references [1–3].

Figure 3 illustrates a sample of this test campaign performed at the Texas A&M University (TAMU) Cyclotron Facility. This test was for simulation of effects from the galactic cosmic ray (GCR) environment: highly energetic particles of danger to electronics in many space missions. Both NASA and Navy Crane team members participated in this test.

Figure. 3. Testing of Intel Broadwell Processor at TAMU.

Building upon the success of these joint efforts has both teams enthusiastically looking forward to further collaborations, and discussions are well underway to extend this teaming even further.

References

[1] C. Szabo, A. R. Duncan, K. A. LaBel, M. J. Kay, P. Bruner, M. Krzesniak, and L. Dong, "Preliminary Radiation Testing of a State-of-the-Art Commercial 14nm CMOS Processor / System-on-a-Chip," in *Proc. 2015 IEEE Radiation Effects Data Workshop*, July 2015, pp. 1–8.

[2] K. A. LaBel, R. A. Gigliuto, C. M. Szabo, M. A. Carts, M. J. Kay, T. Sinclair, M. J. Gadlage, A. R. Duncan, and J. D. Ingalls, "Hardness Assurance for Total Dose and Dose Rate Testing of a State-of-the-Art Off-Shore 32 nm CMOS Processor," in *Proc. 2013 IEEE Radiation Effects Data Workshop*, July 2013, pp. 1–6.

[3] A. R. Duncan, C. M. Szabo, D. P. Bossev, K. A. LaBel, A. M. Williams, M. J. Gadlage, J. D. Ingalls, C. H. Hedge, A. H. Roach, and M. J. Kay, "Single Event Effects in 14-nm Intel Microprocessors," Presented at *2016 IEEE Radiation Effects Data Workshop*, July 2016.

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5

Evaluating Automotive Parts for Potential NASA Applications

- **The main drivers are size, weight, and price of electronic components**
  - **Commercial electronic parts usually offer varied functions**
  - **How do automotive parts compare to catalog commercial?**
- **Commercial Parts Options**
  - **Manufacturers make parts to meet the needs of their chosen market(s)**
  - **Automotive parts are designed to meet the needs of subsystem suppliers to automobile manufacturers**
- **Space**
  - **Parts from manufacturers that are qualified to the Automotive Electronics Council (AEC) Q specifications seem to offer advantages for the smallsat users**
  - **NASA is doing a limited evaluation of automotive electronic parts**

Evaluating Automotive Parts for Potential NASA Applications

AEC Q specifications are Qualification Requirements Only, Focused on:

- **A One-Time INITIAL QUALIFICATION of a Device Family**
  - **"Device Family" is Common Materials, Processes, Designs, Manufacturing Location, etc.**
  - **"Generic Data" may be used provided relevance of data can be demonstrated**
- **Requirements for REQUALIFICATION**
  - **Provides recommendations as needed**
- **Requirements for process change notification (PCN) to automotive customers**
- **THEY DO NOT PROHIBIT PURE TIN**

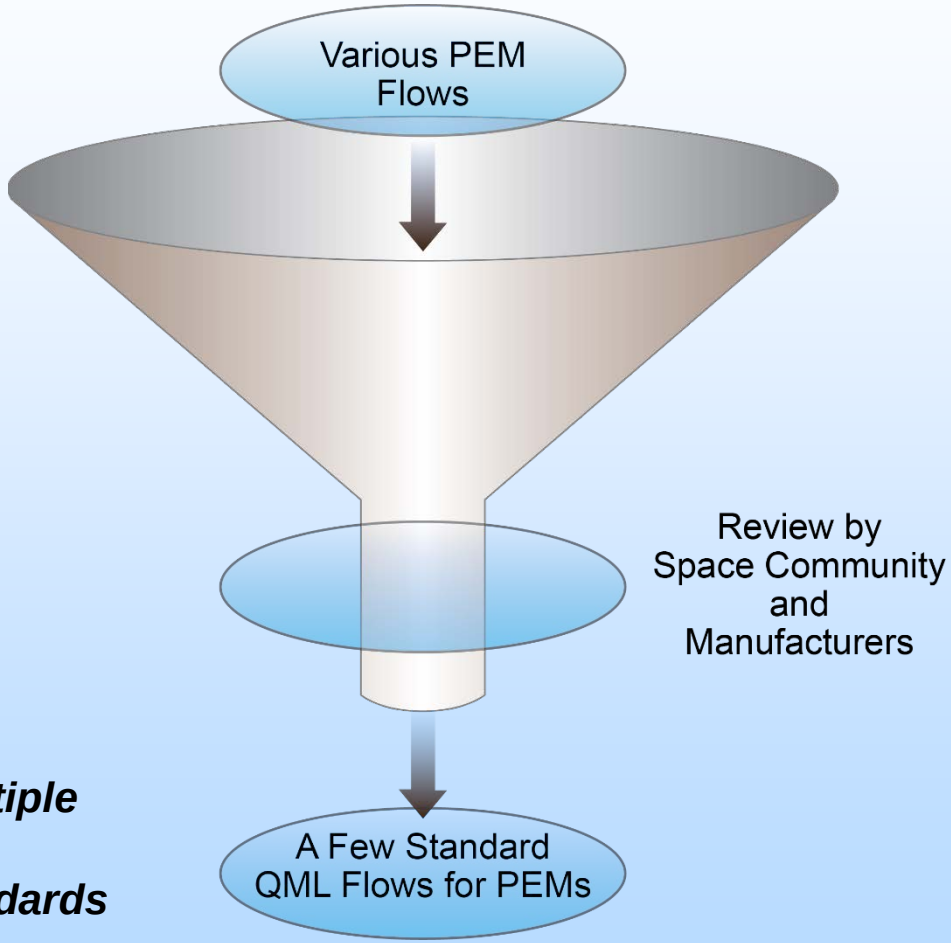
– Whisker mitigation is recommended!

Counterfeit Parts

- Refers to counterfeit parts awareness and mitigation.
- GIDEPs (Government Industry Data Exchange Program [reports]) on counterfeit parts are reviewed on NEPAG telecons.
- During the DLA audits, the manufacturers are asked for their counterfeit mitigation plans. Most of them have some form of mitigation.
- NASA provides counterfeit training.
- NASA supports the SAE (Society of Automotive Engineers) effort.
- Procure parts, particularly new technology devices, from the authorized sources.

Standard PEMs (Plastic Encapsulated Microcircuits) for Potential NASA Applications

- ***NASA Applications***
  - ***Cubesats***
  - ***Smallsats***
  - ***Others***



Standardizing on a few well-defined flows rather than multiple flows defined by each manufacturer or by each standards group.

NASA Workshop

- **Workshop**
  - **NASA Small Missions Workshop combined with Electronic Technology Workshop (ETW) is held in June every year**
    - **Next ETW will be June 19–22, 2017**
  - **Venue: Goddard Space Flight Center, Greenbelt, MD**
  - **Past papers posted on NEPP Website:**
    nepp.nasa.gov
  - **See above website for other details**

Conclusion

- **Adapting new technology is an on-going challenge.**
- **NASA has responded to an ever changing environment over the years**
  - **NASA supports a very wide spectrum of space missions/programs ranging from smallsats/cubesats to flagship missions such as Juno and the planned Europa mission. The success of each mission is important.**
  - **NASA has adopted next-generation devices over the years through our own evaluations and jointly working with other space entities.**
  - **We have adopted progressively smaller and more capable parts as technology advanced.**
- **The JAXA Microelectronics Workshop (MEWS) is an extremely useful resource**

Thank you!

JUNO @ Jupiter

- ***On July 4, 2016, the Juno spacecraft arrived at Jupiter.***
- ***Please watch the video for Juno (courtesy of NASA/JPL-CalTech).***

http://nepp.nasa.gov

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