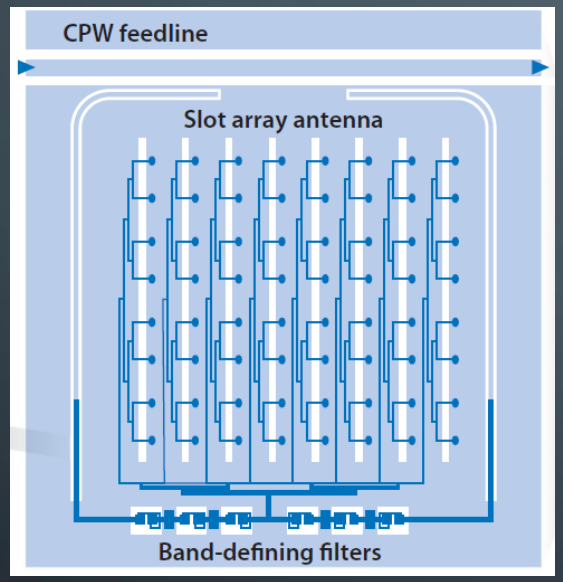
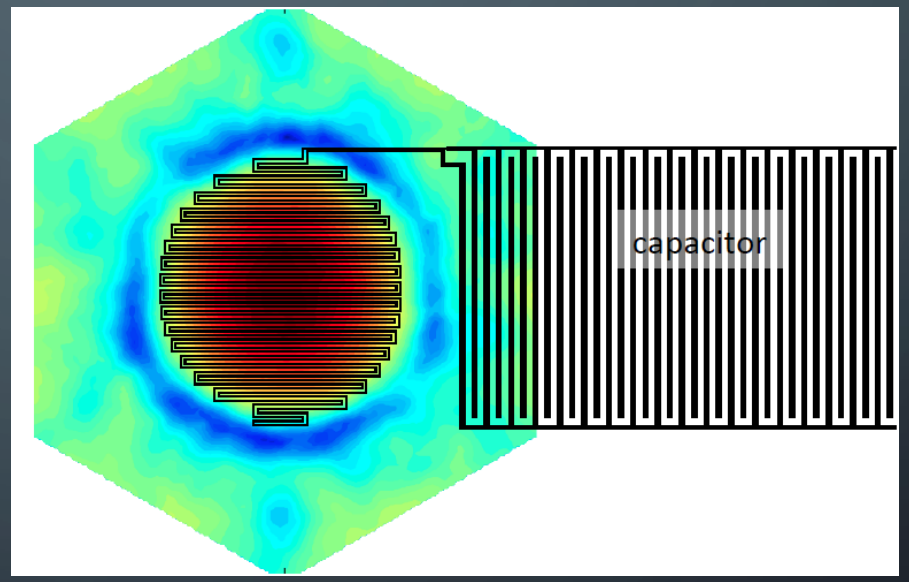
RTD INTRO: LOW-LOSS, LOW-NOISE, CRYSTALLINE SILICON DIELECTRIC FOR SUPERCONDUCTING DETECTORS





.ANDREW D. BEYER[1], M.I. HOLLISTER[2], J. SAYERS[2], C.F. FREZ[1], AND S.R. GOLWALA[2].

[1]JET PROPULSION LABORATORY, CALIFORNIA INSTITUTE OF TECHNOLOGY, PASADENA, CA.

[2] CALIFORNIA INSTITUTE OF TECHNOLOGY, PASADENA, CA.

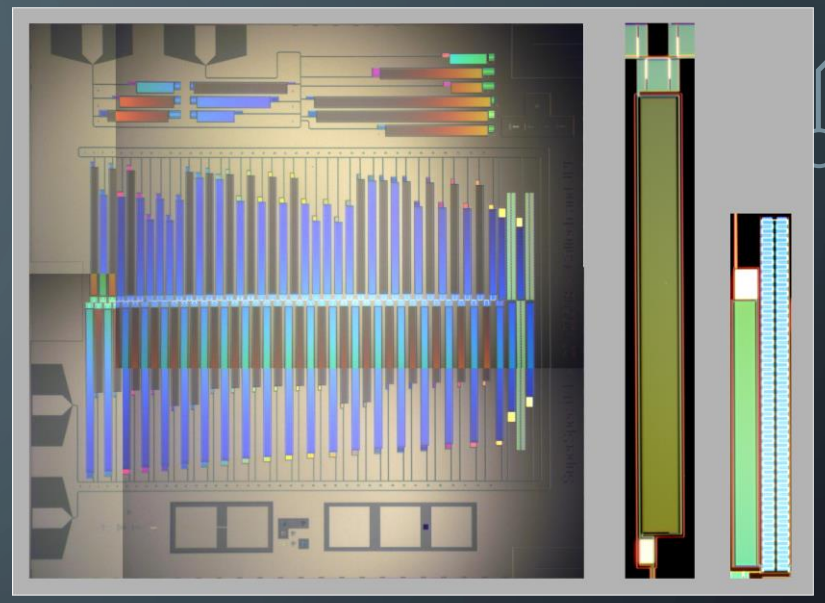
Images from J. Zmuidzinas' talk: https://sofia.usra.edu/Science/SCF/pdf/02-19-14_Zmuidzinas.pdf

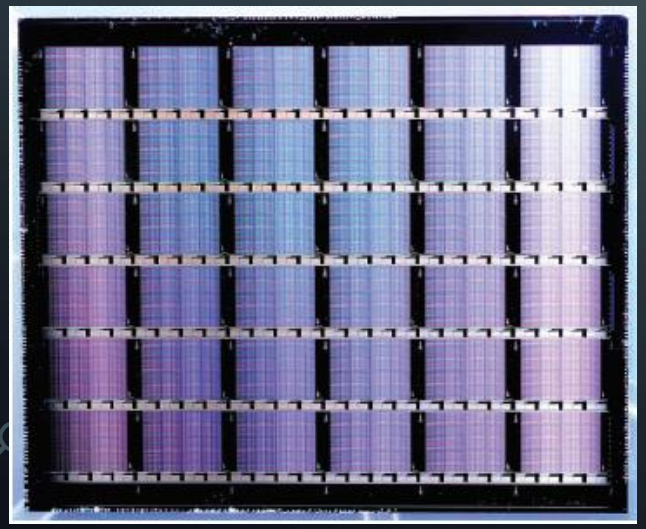
Superconducting detector architectures relying upon dielectrics

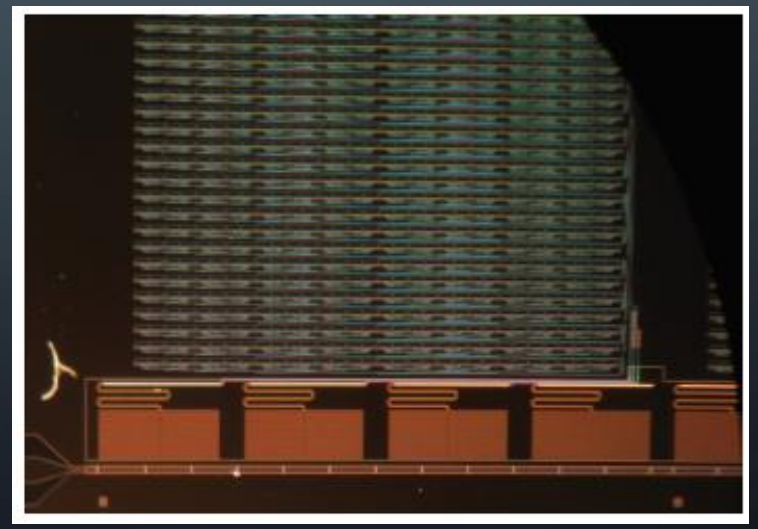
Future Physics of the Cosmos and Cosmic Origins missions require large arrays of highly sensitive millimeter-wave and submillimeter detectors, including spectroscopic detectors:

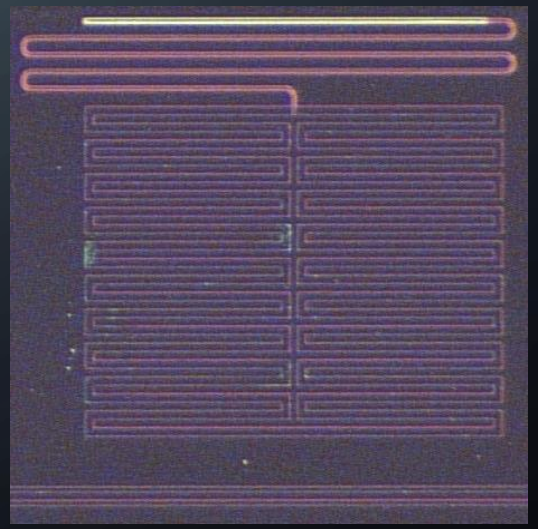
- **superconducting phased-array antennas**
- **superconducting spectrometers**
- **kinetic inductance detectors (KIDs).**

SuperSpec (below)





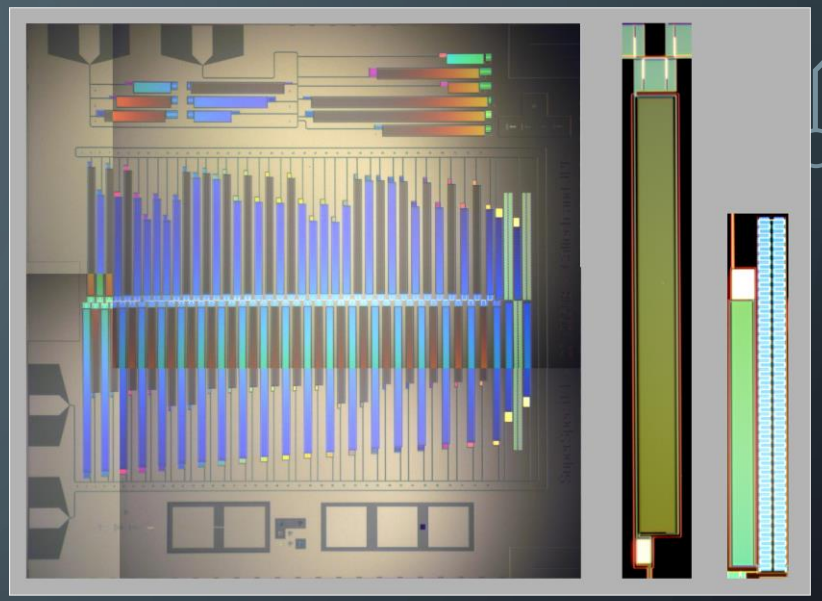




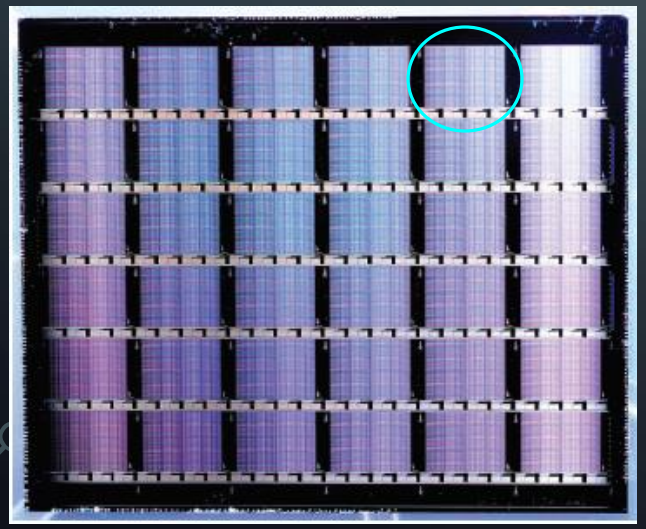
Superconducting detector architectures relying upon dielectrics

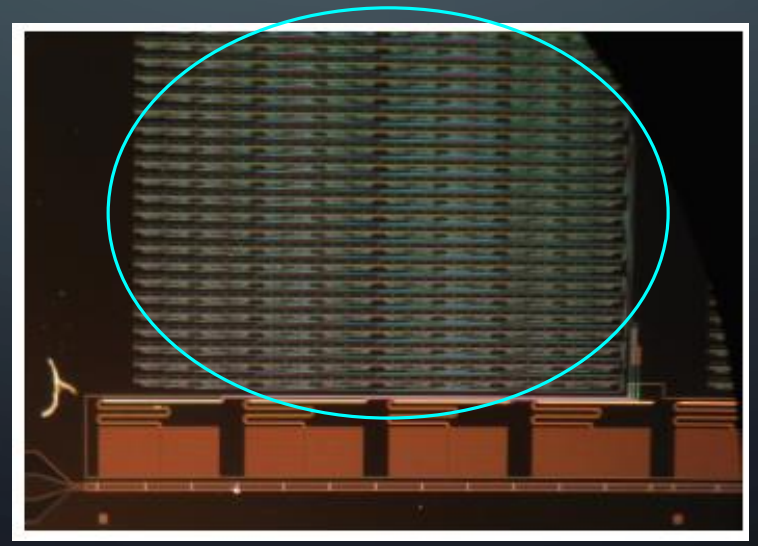
- **superconducting phased-array antennas:** E.g. BICEP2, Keck Array, BICEP3, and SPIDER suborbital CMB polarization receivers and the Caltech Submillimeter Observatory's MUSIC multiband camera;
- **superconducting spectrometers:** E.g. SuperSpec
- **kinetic inductance detectors (KIDs)**: E.g. MAKO, MUSIC.

SuperSpec (below)

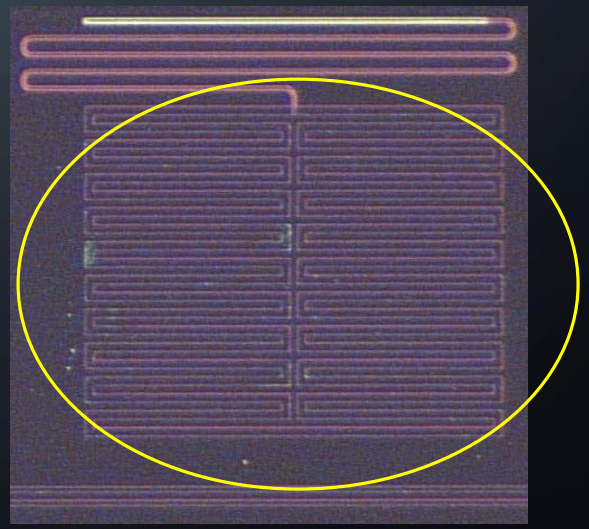


MUSIC phased array antenna





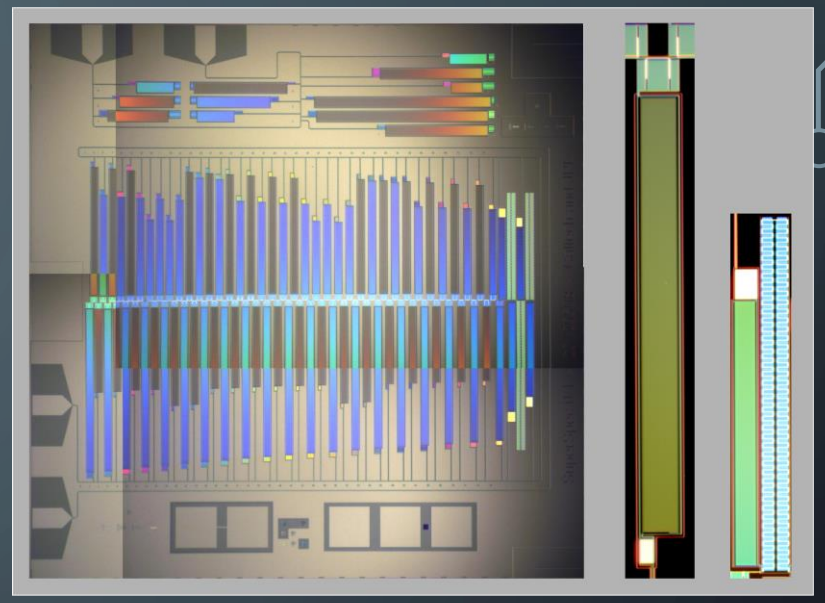
KID interdigitated capacitor



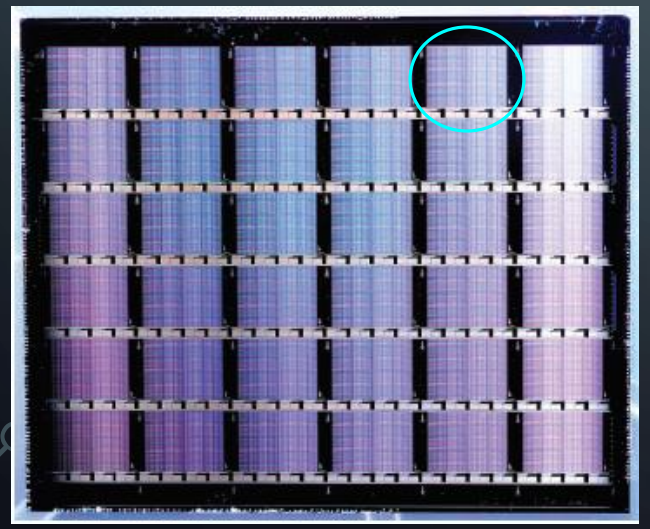
Superconducting detector architectures relying upon dielectrics

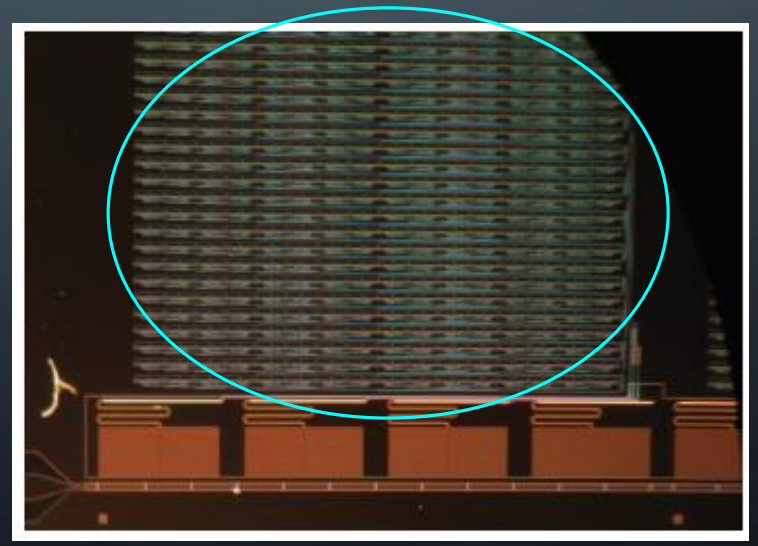
- **superconducting phased-array antennas:** rely on superconductor-dielectric-superconductor microstrip transmission line to coherently sum radiation received by arrays of slot dipole antennas and to define spectral bandpasses;
- **superconducting spectrometers:** uses superconducting microstrip to route optical power to detectors and to define spectral channels;
- **kinetic inductance detectors (KIDs)**: use capacitors.

SuperSpec (below)

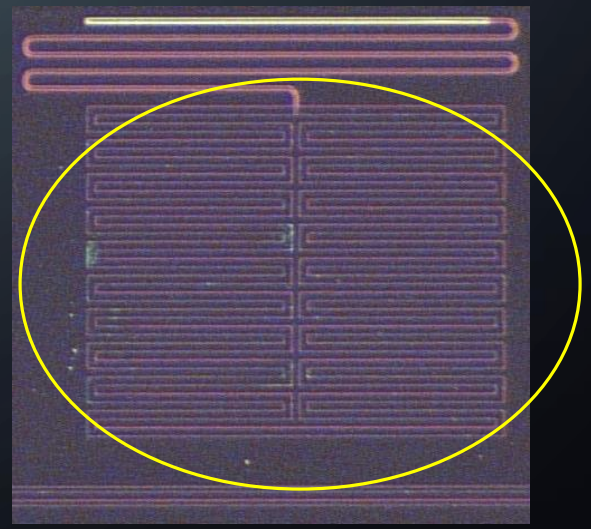


MUSIC phased array antenna

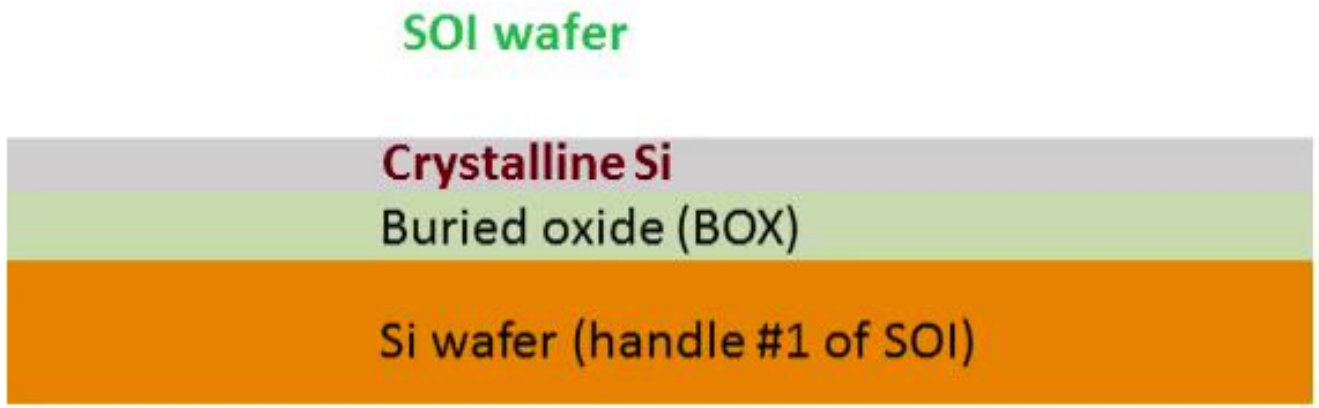




KID interdigitated capacitor

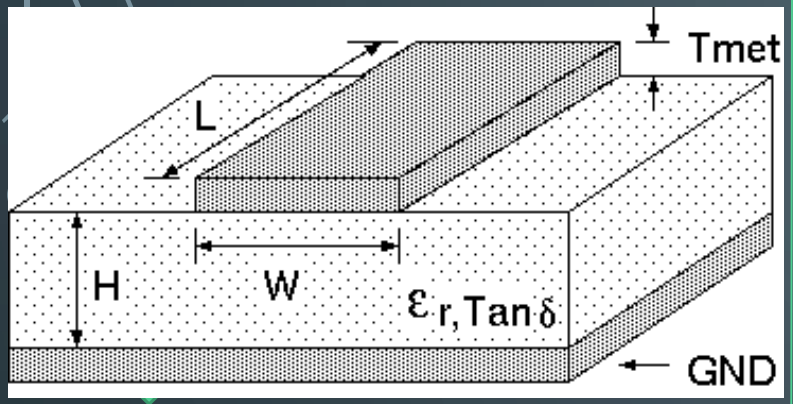


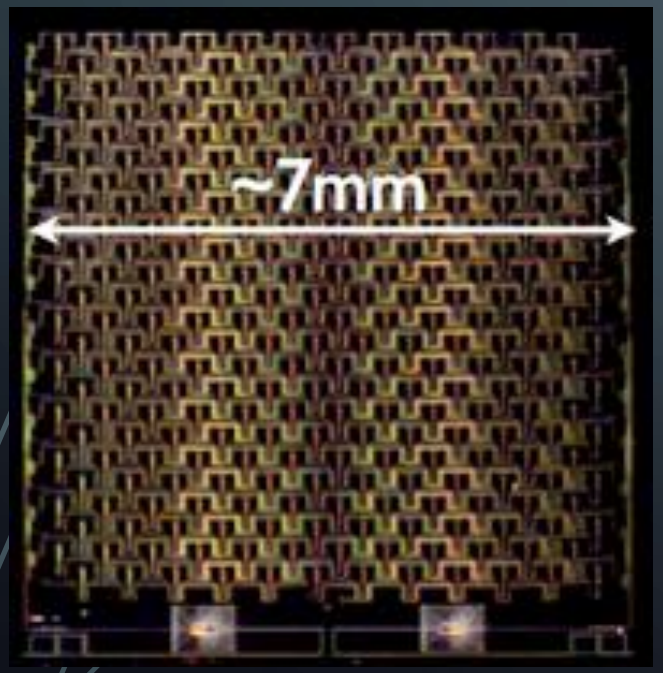
Fabrication idea



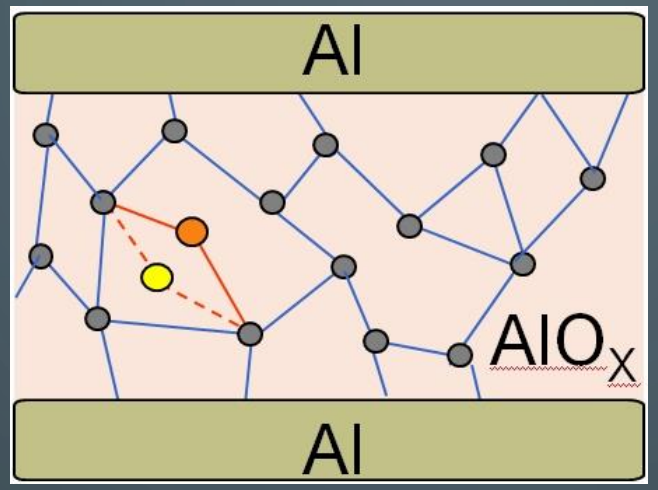
Amorphous vs. crystalline materials

Microstrip loss

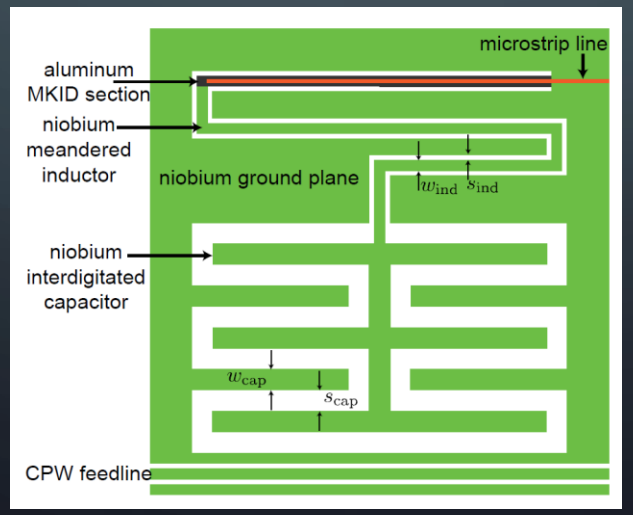




Two-level systems (TLS): excess noise in KIDs



Use large, interdigitated C

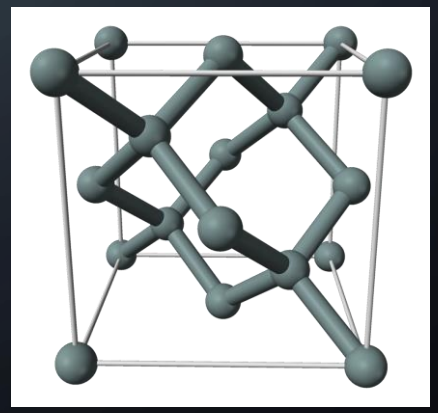


From O. Noroozian thesis (Caltech 2012).

- Dielectric loss, quantified by loss tangent: tan δ.

Superconducting detectors w/ dielectrics:

- Currently, amorphous dielectrics (SiO_2, SiN_x, amorphous hydrogenated silicon (a-Si:H)) are used because they are most convenient for fabrication. →They have tan $\delta \sim 10^{-3}$.
- Crystalline Si: tan $\delta < 5\times10^{-6}$.



Amorphous vs. crystalline materials

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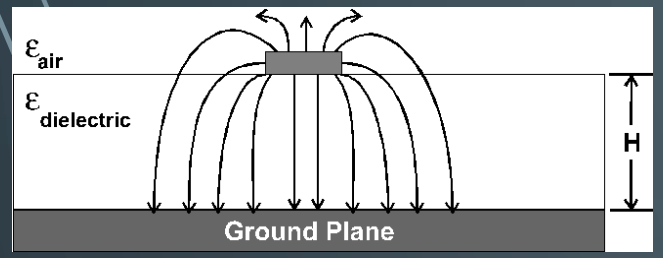
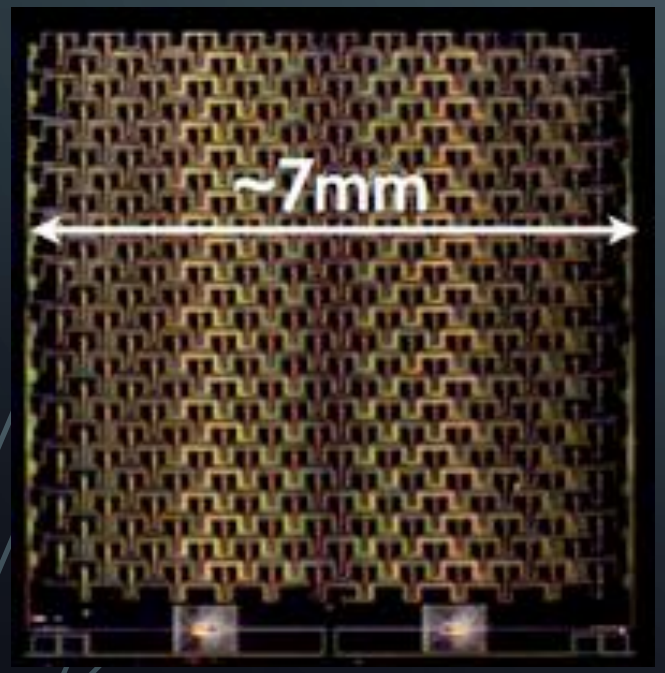


Significant loss in clever antennas



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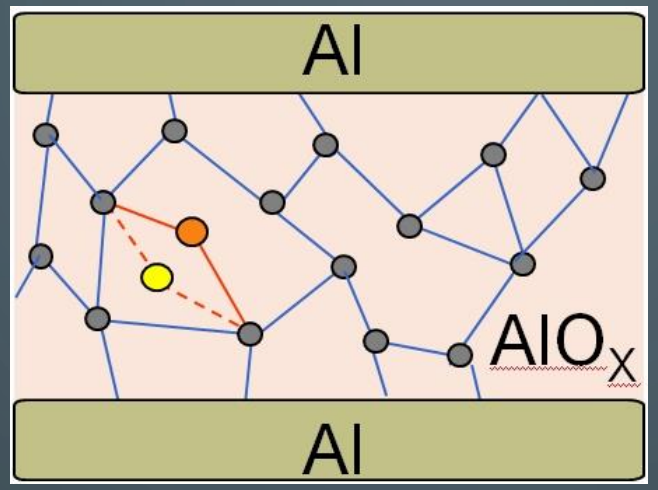

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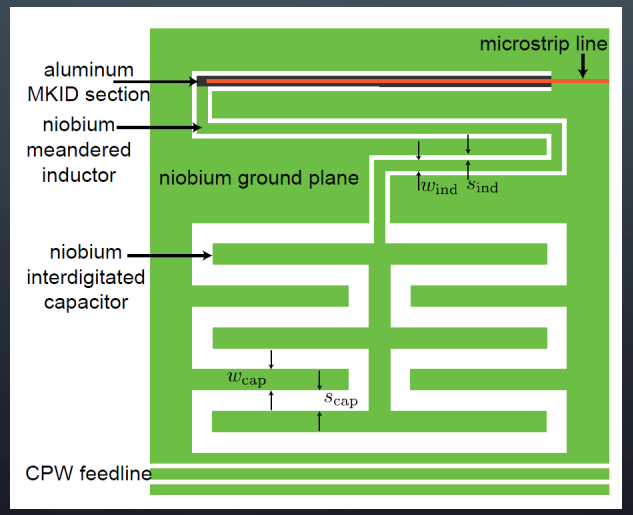

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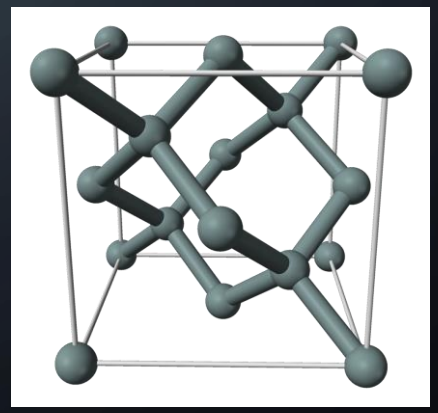
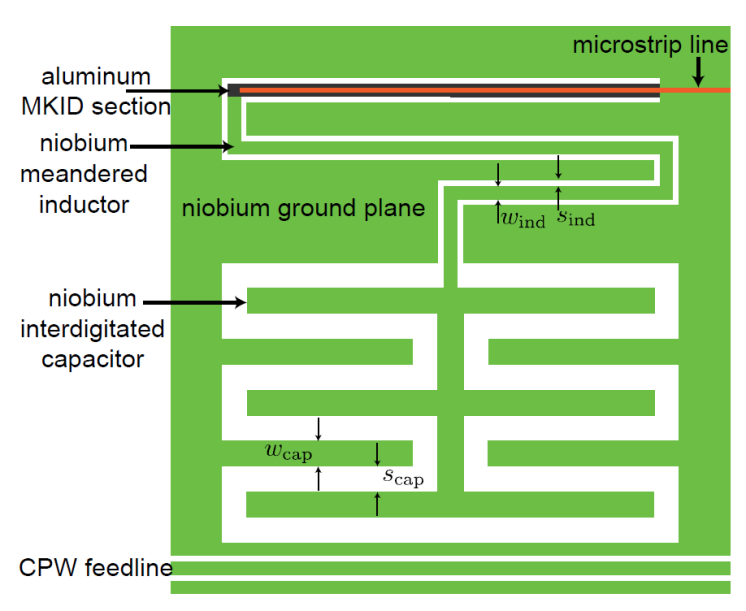
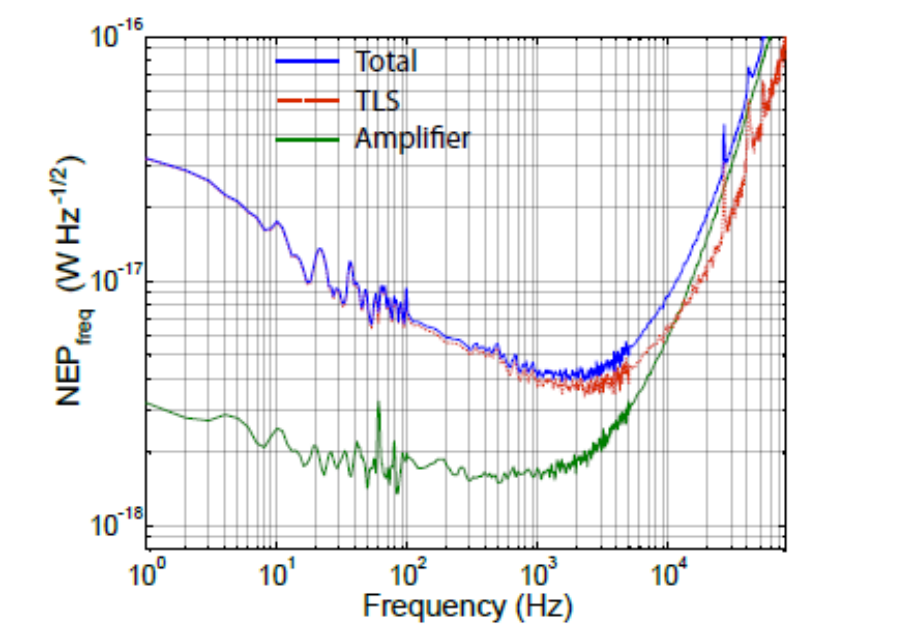
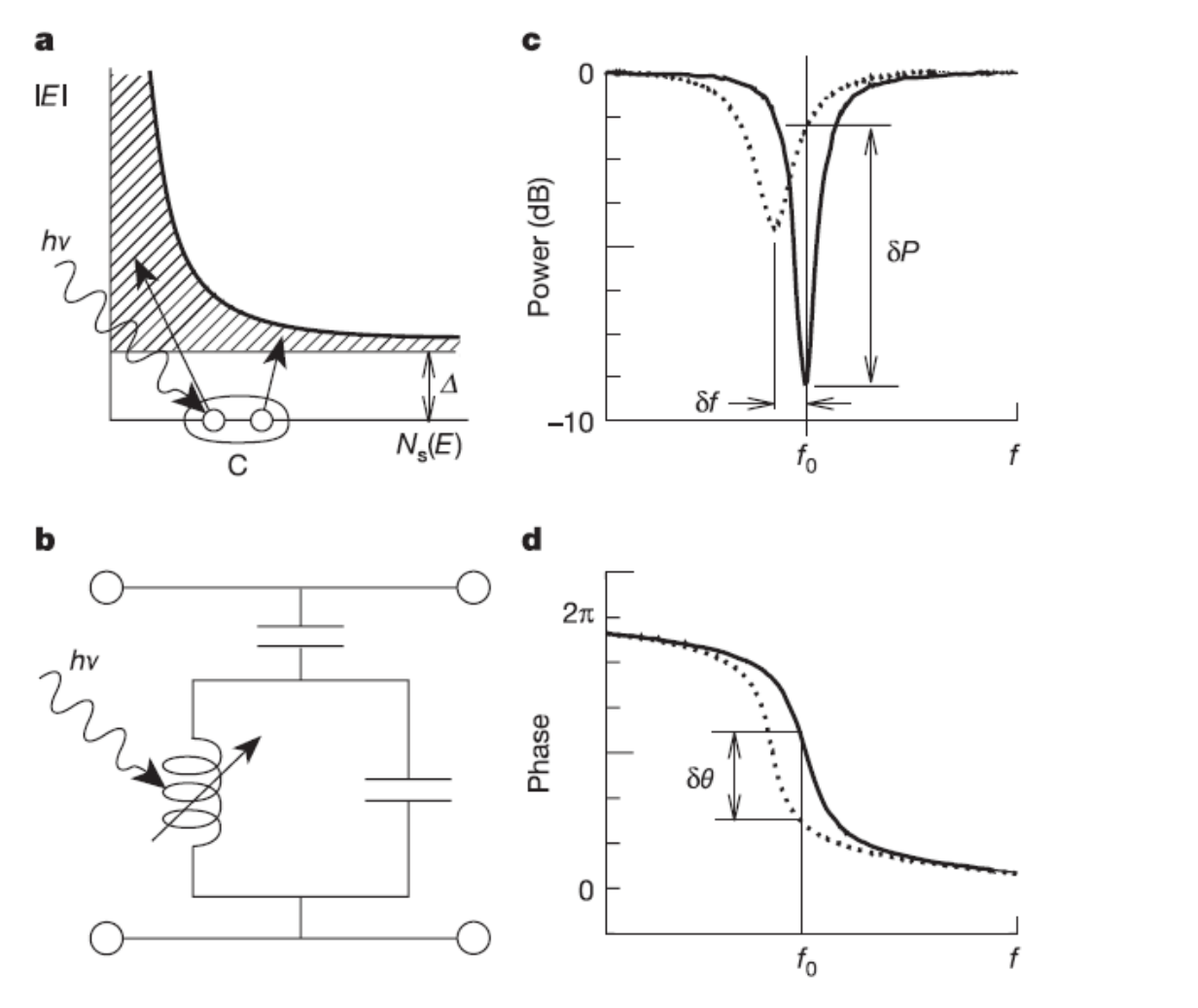


Kinetic inductance detectors (KIDs)



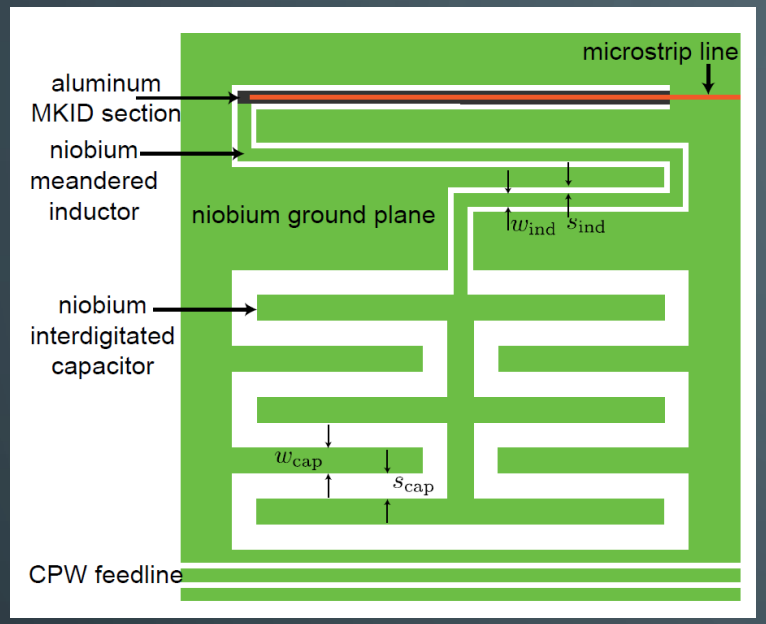


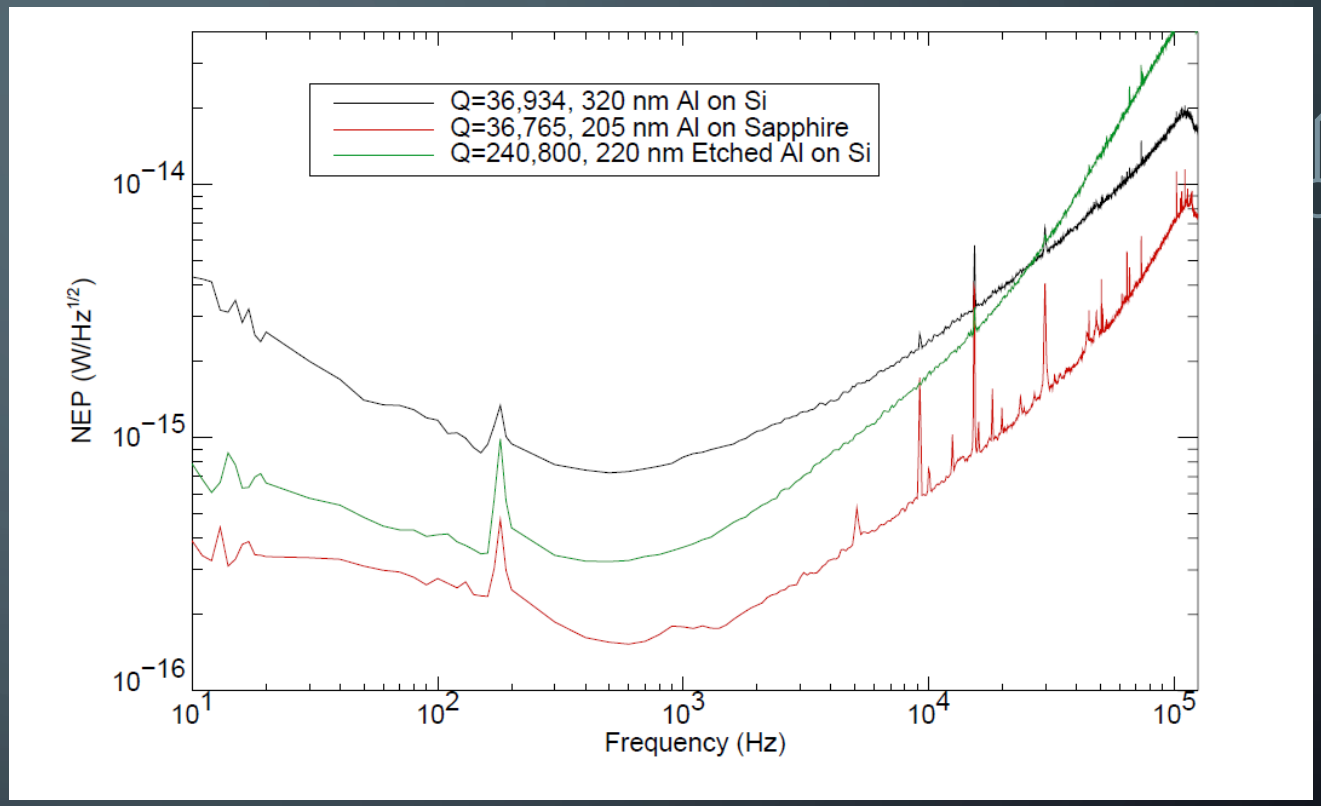
NEP: Noise equivalent power

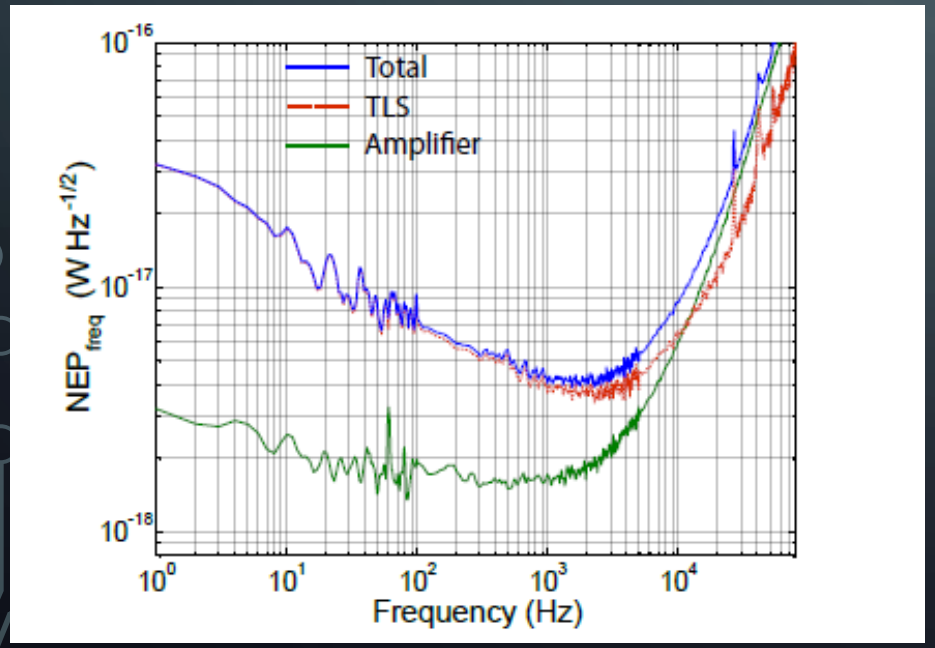


Left images: O. Noroozian thesis, Caltech 2012.
Right image: B. Mazin thesis, Caltech 2004.

Kinetic inductance detectors (KIDs)



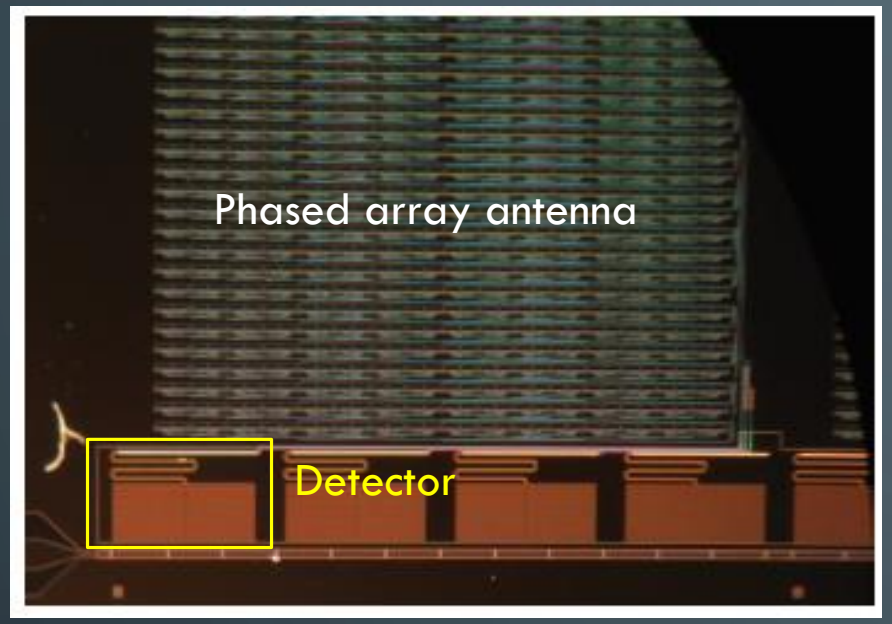


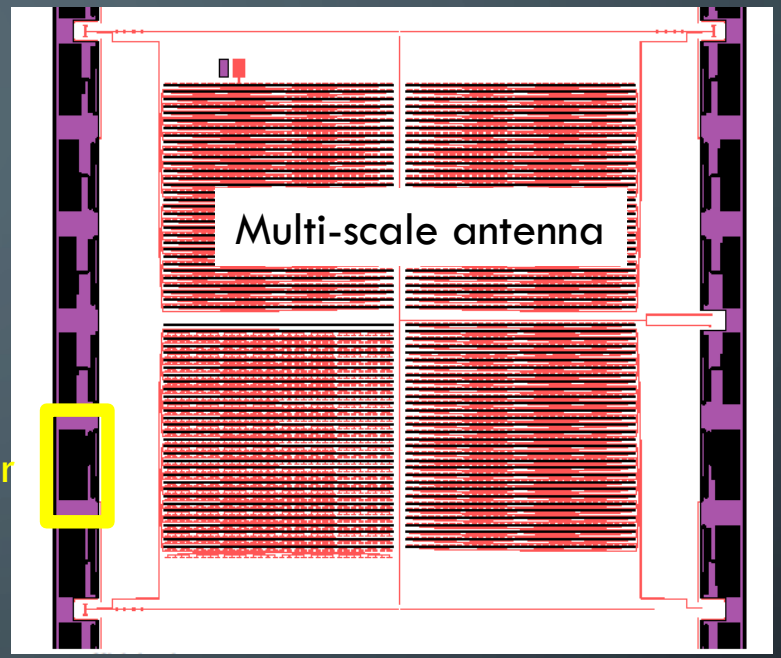


- Substrate dielectric affects noise performance.

Left images: O. Noroozian thesis, Caltech 2012.
Right image: B. Mazin thesis, Caltech 2004.

Advantages of reducing loss tangent in detectors





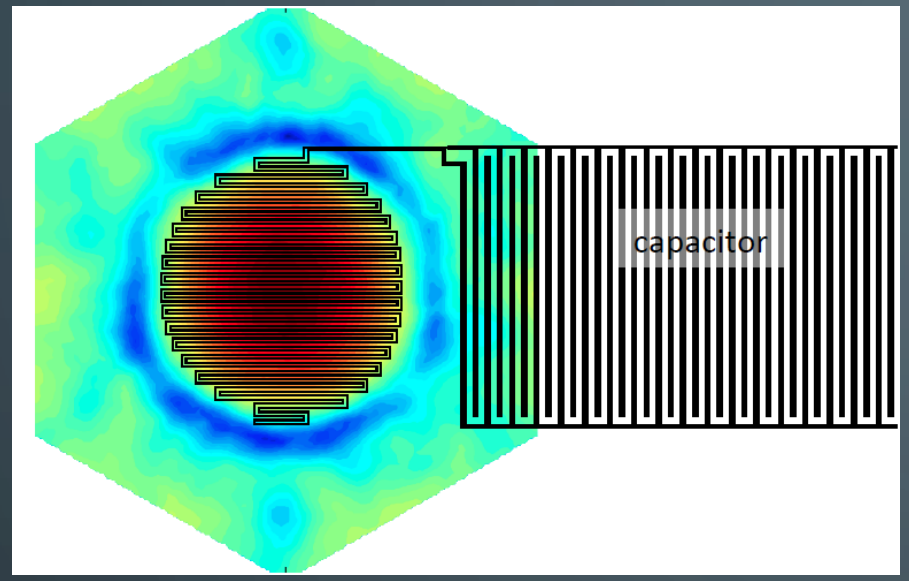
- **Phased-array antennas:** move detectors away from antenna and shield from absorption of unfiltered (spatial or spectral) light. Allow to simplify detector wiring → X long wiring busses. Multiscale antennas covering a decade of spectral bandwidth possible.

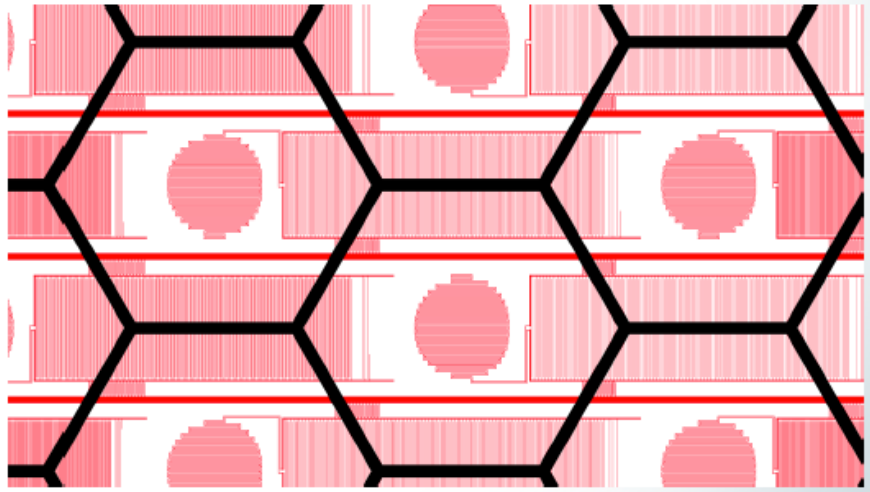
- **Superconducting spectrometers:** improve spectral resolution limit, $R_{max} \approx (1/\tan \delta)$, from 10^3 to 2×10^5→resolved extragalactic mm/submm spectroscopy (intrinsic line widths $\Delta\nu/\nu \sim 10^{-4}$ to 10^{-3}).

- **KIDs:** interdigitated capacitors (IDC) replaced by parallel-plate capacitors 40 times smaller in area. Currently, IDCs can be an appreciable fraction of focal plane area. E.g. In KIDs for imaging at 350 μm (MAKO), it has been necessary to introduce the complexity of a microlens arrays to focus incoming light on the small active region of the detectors.

Advantages of reducing loss tangent in detectors

Images from J. Zmuidzinas' talk: https://sofia.usra.edu/Science/SCF/pdf/02-19-14_Zmuidzinas.pdf





Layout showing inductor, capacitor and coupling (red) + lens positions (black)

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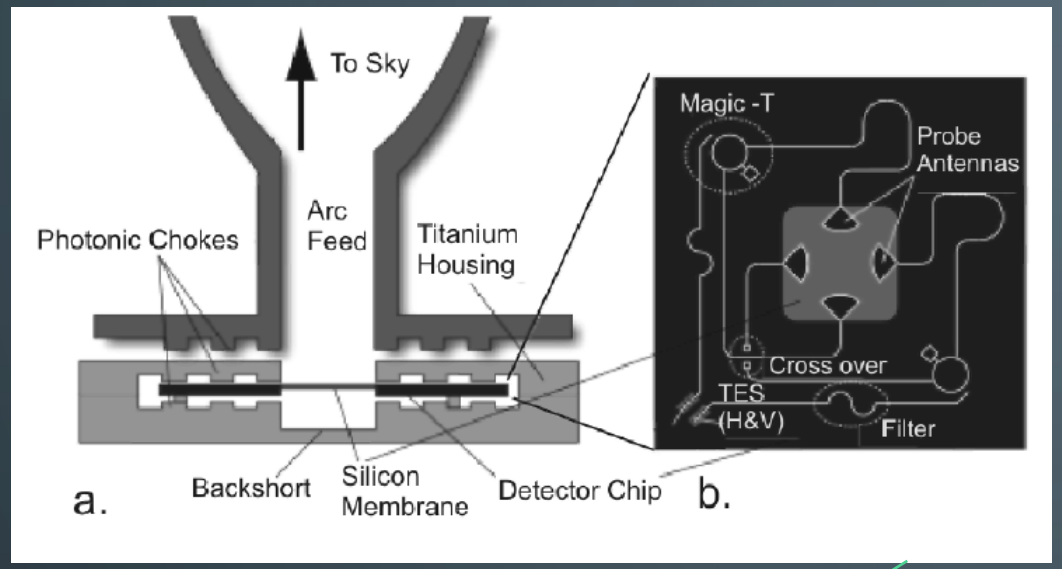
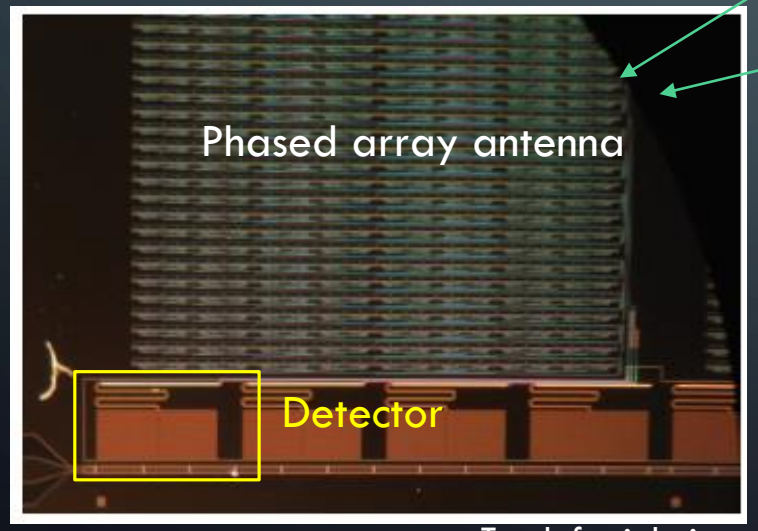
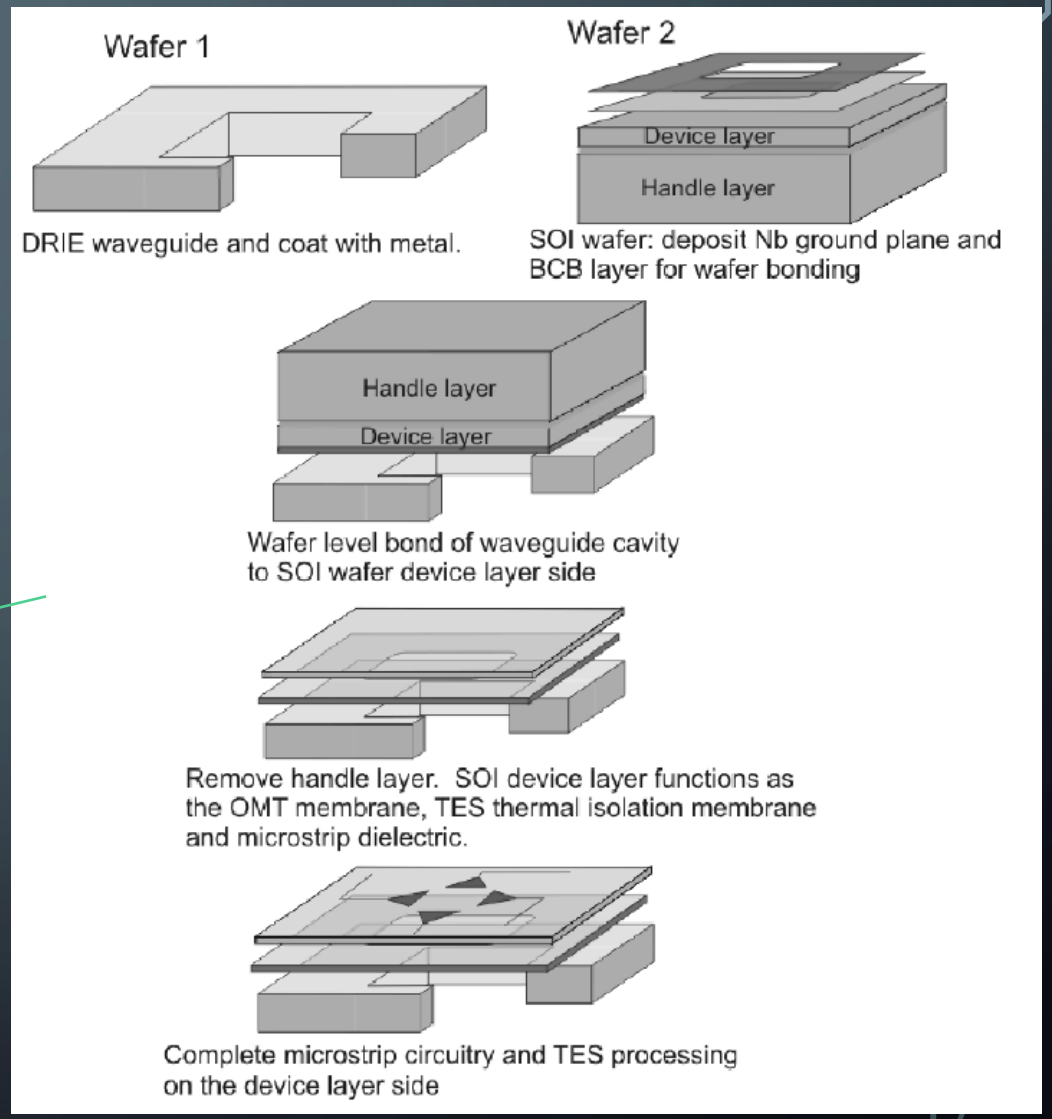
Fabrication inspiration



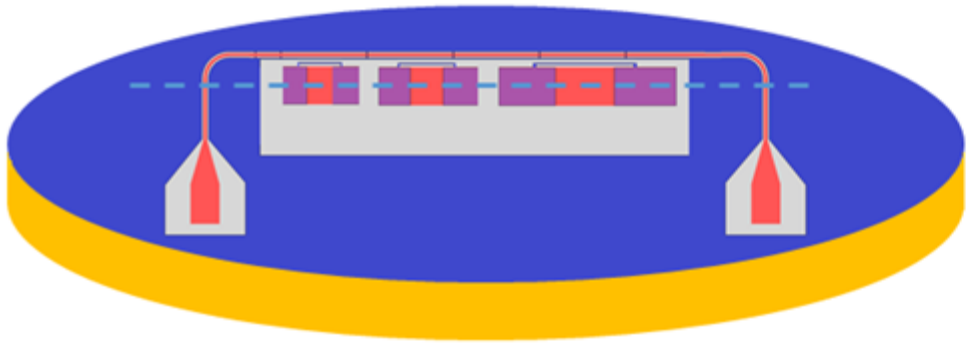


Employ ideas here



Top left, right images from Denis et. al. AIP Conference Proceedings **1185**, 371 (2009); doi: 10.1063/1.3292355

Goals



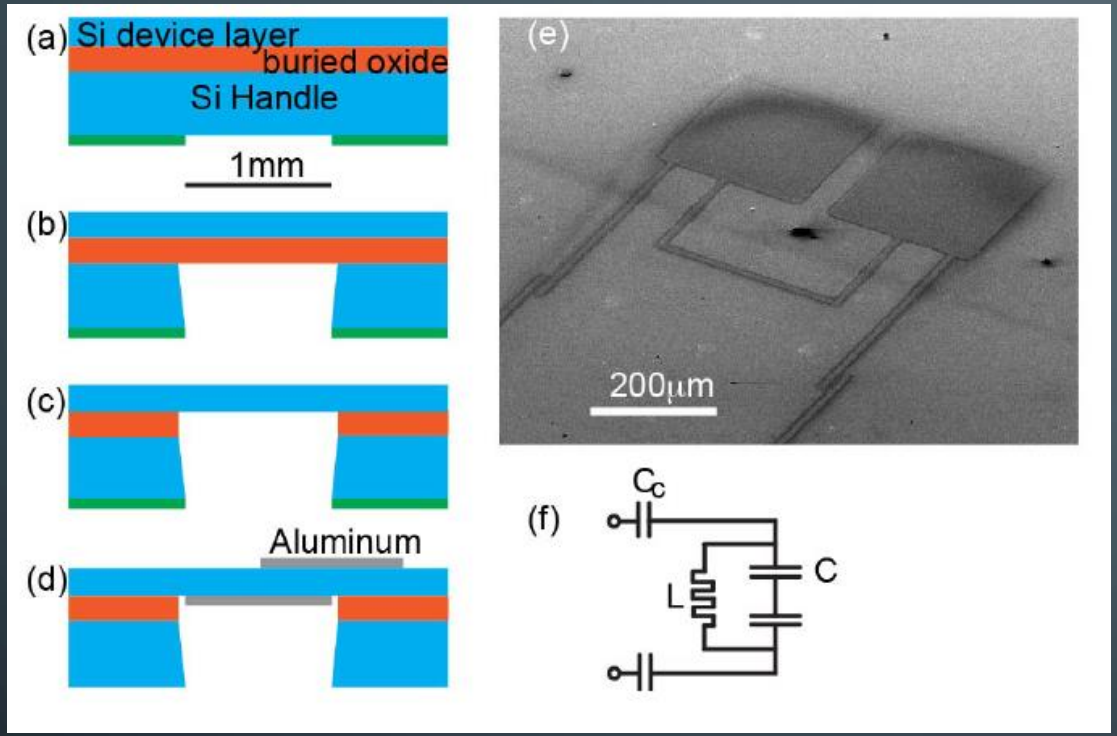
Control experiment

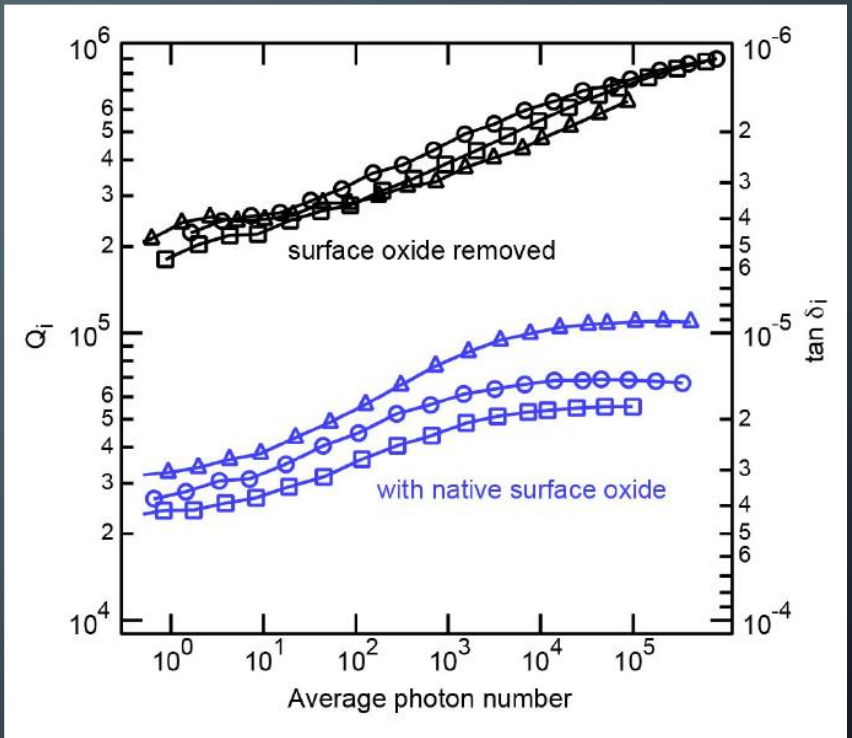
Wafer bond experiment

Year 1: Develop control experiment to evaluate dielectric without wafer bonding.
Develop RF loss test device with device thickness of 5um then 1um using wafer bonding.

Year 2: Develop mm-wave loss test device with device thickness of 5um then 1um with wafer bonding.

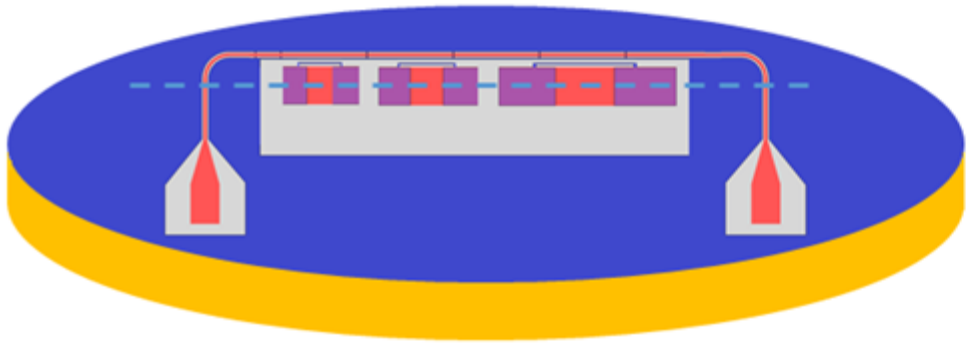
Control experiment: SOI loss before wafer bonding





Images from: Weber *et. al.*, Appl. Phys. Lett. **98**, 172510 (2011); http://dx.doi.org/10.1063/1.3583449

Goals



Control experiment

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Goal 1: Develop control experiment to evaluate dielectric without wafer bonding.
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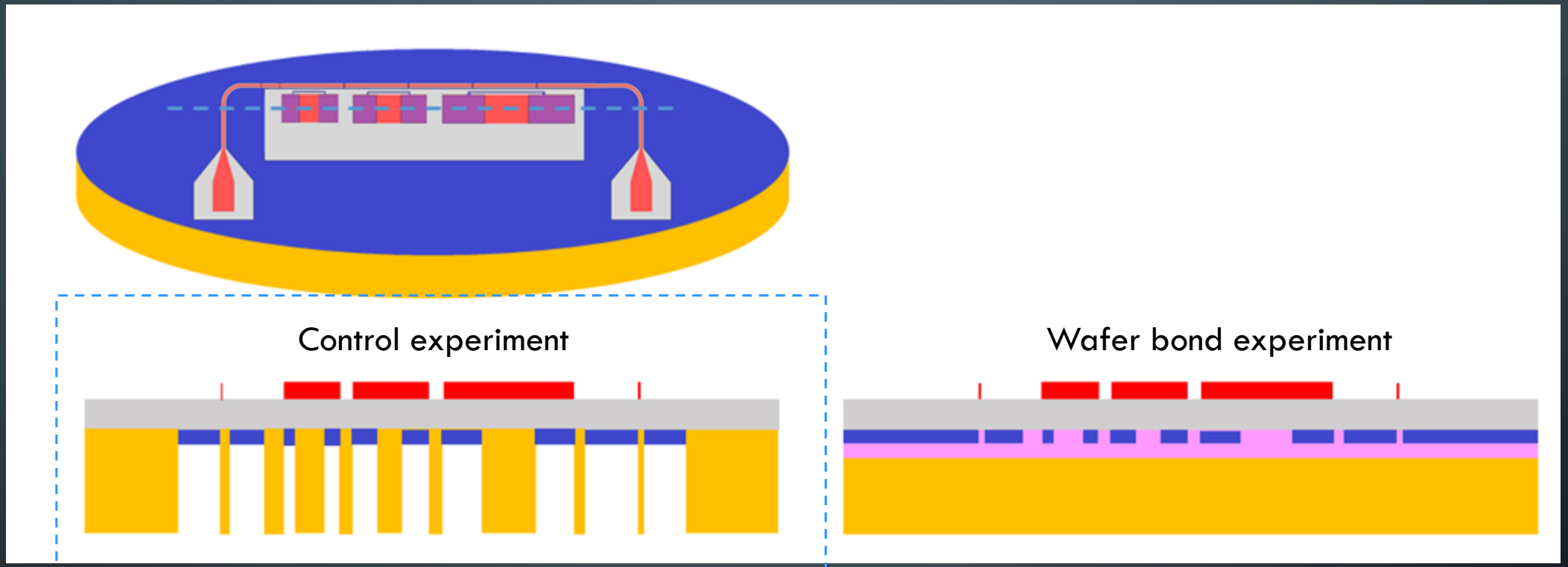
Goals



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Control Experiment analysis

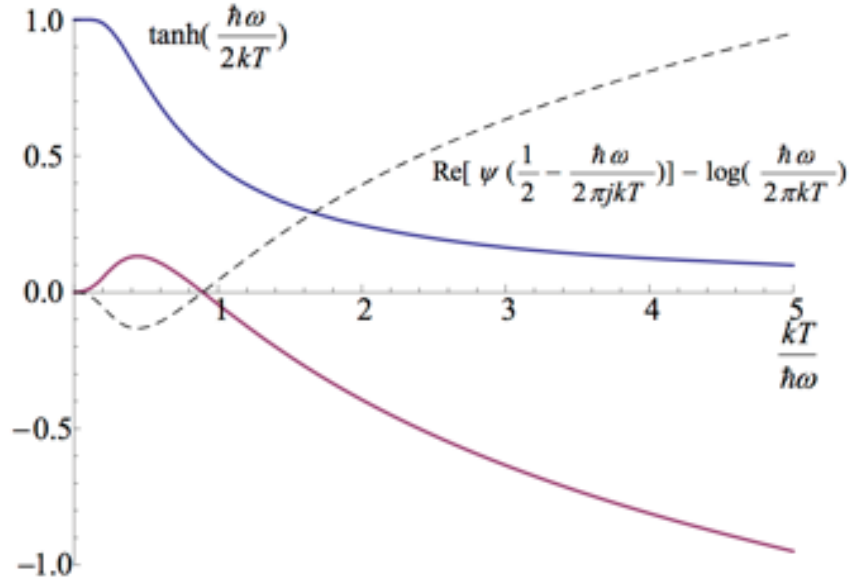
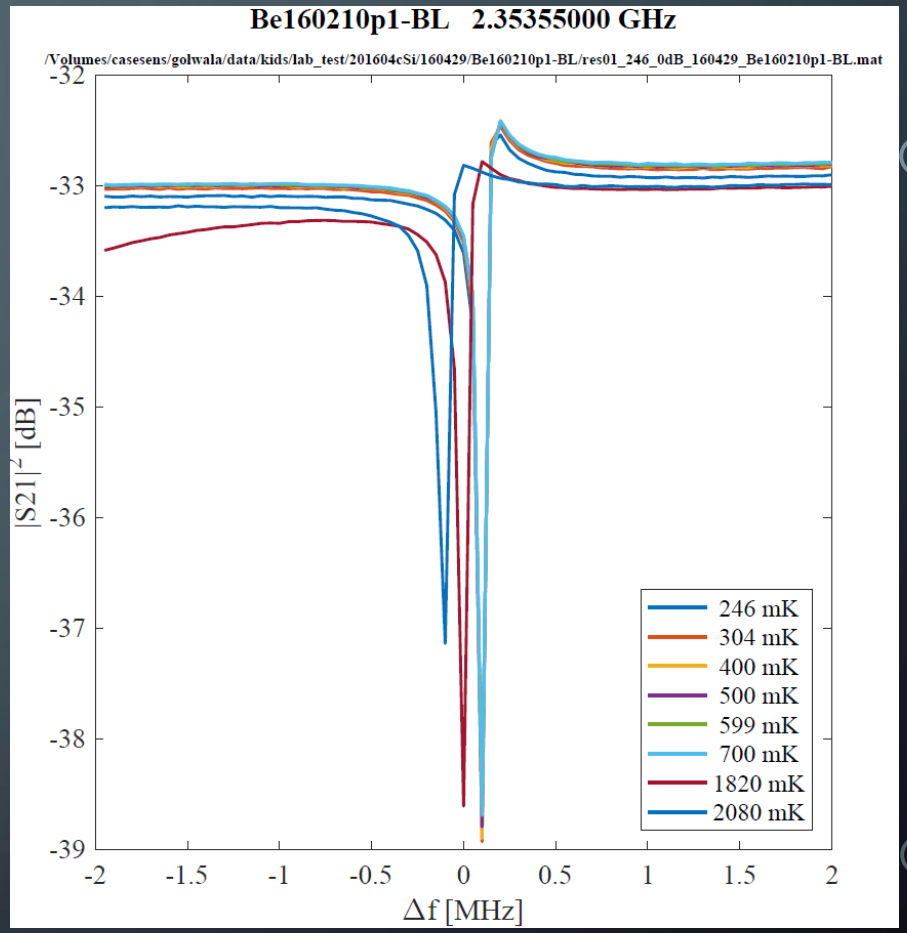
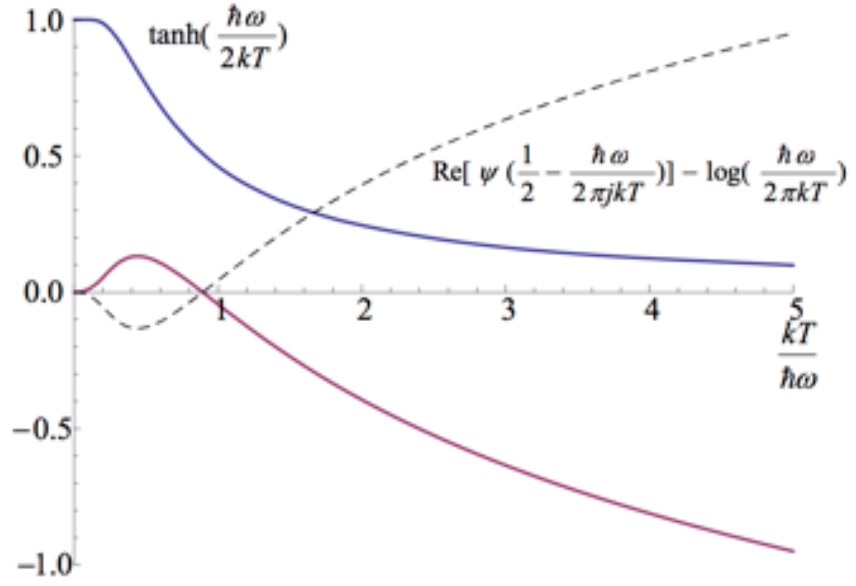


Figure 5.13: Temperature dependence of δ_{TLS} (blue curve) and ϵ'_{TLS} (red curve)



$$\frac{f_r(T) - f_r(0)}{f_r} = \frac{F\delta^0_{\mathrm{TLS}}}{\pi}\left[\mathrm{Re}\Psi\left(\frac{1}{2} - \frac{\hbar\omega}{2j\pi k_B T}\right) - \log\frac{\hbar\omega}{2\pi k_B T}\right]. \tag{5.74}$$

Control Experiment analysis



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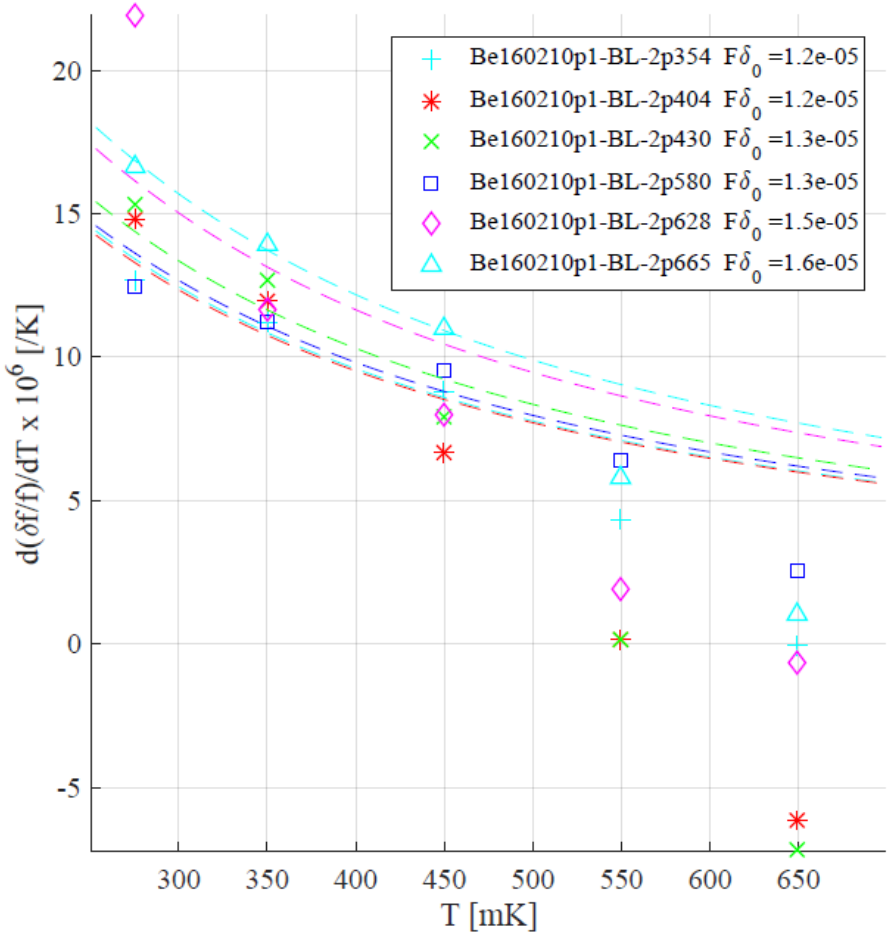


Control Experiment analysis

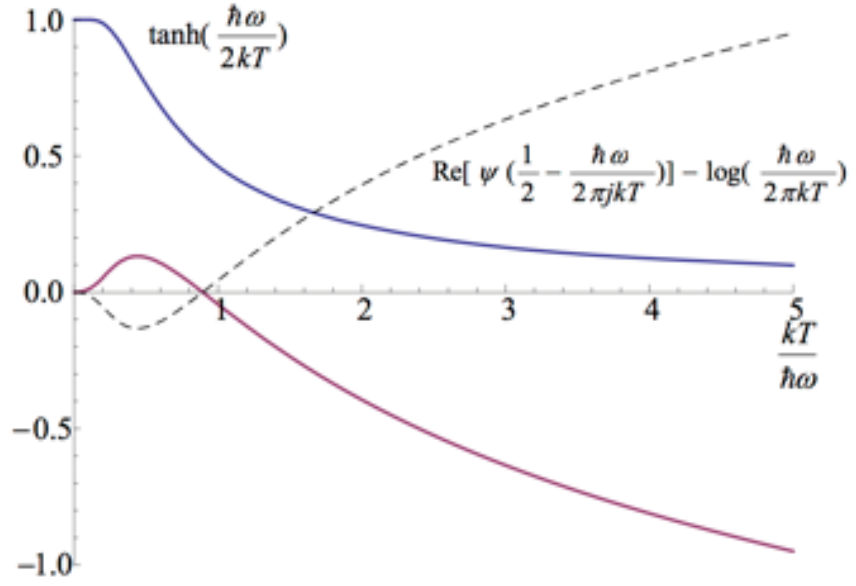
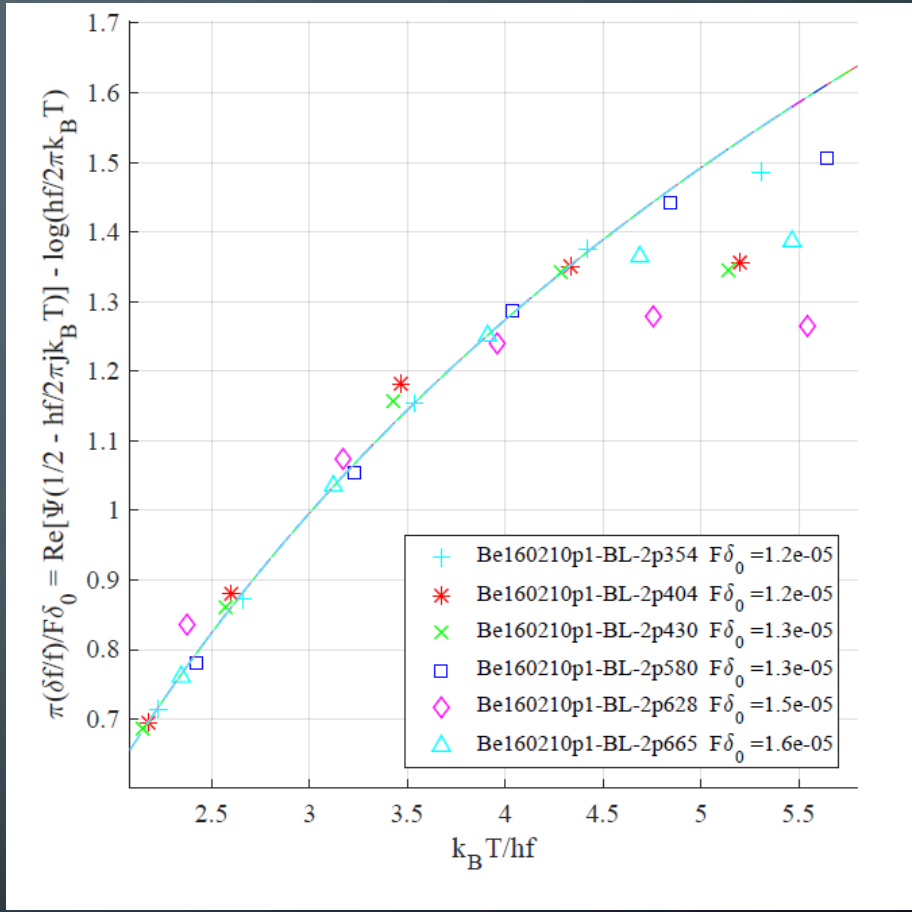


Figure 5.13: Temperature dependence of δ_{TLS} (blue curve) and ϵ'_{TLS} (red curve)



$$\frac{f_r(T)-f_r(0)}{f_r} = \frac{F\delta^0_{\mathrm{TLS}}}{\pi}\left[\mathrm{Re}\Psi\left(\frac{1}{2}-\frac{\hbar\omega}{2j\pi k_B T}\right)-\log\frac{\hbar\omega}{2\pi k_B T}\right]. \tag{5.74}$$

Control Experiment analysis

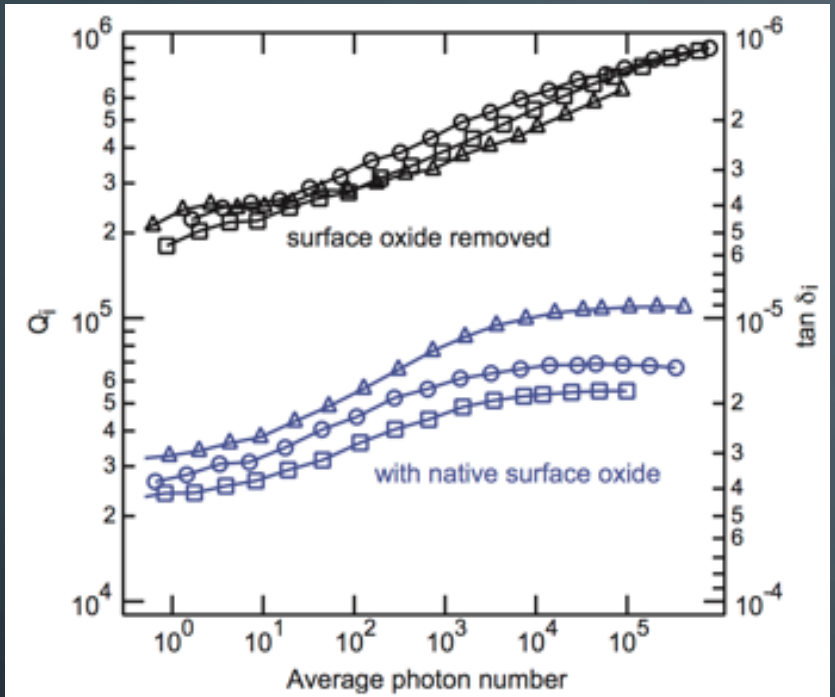
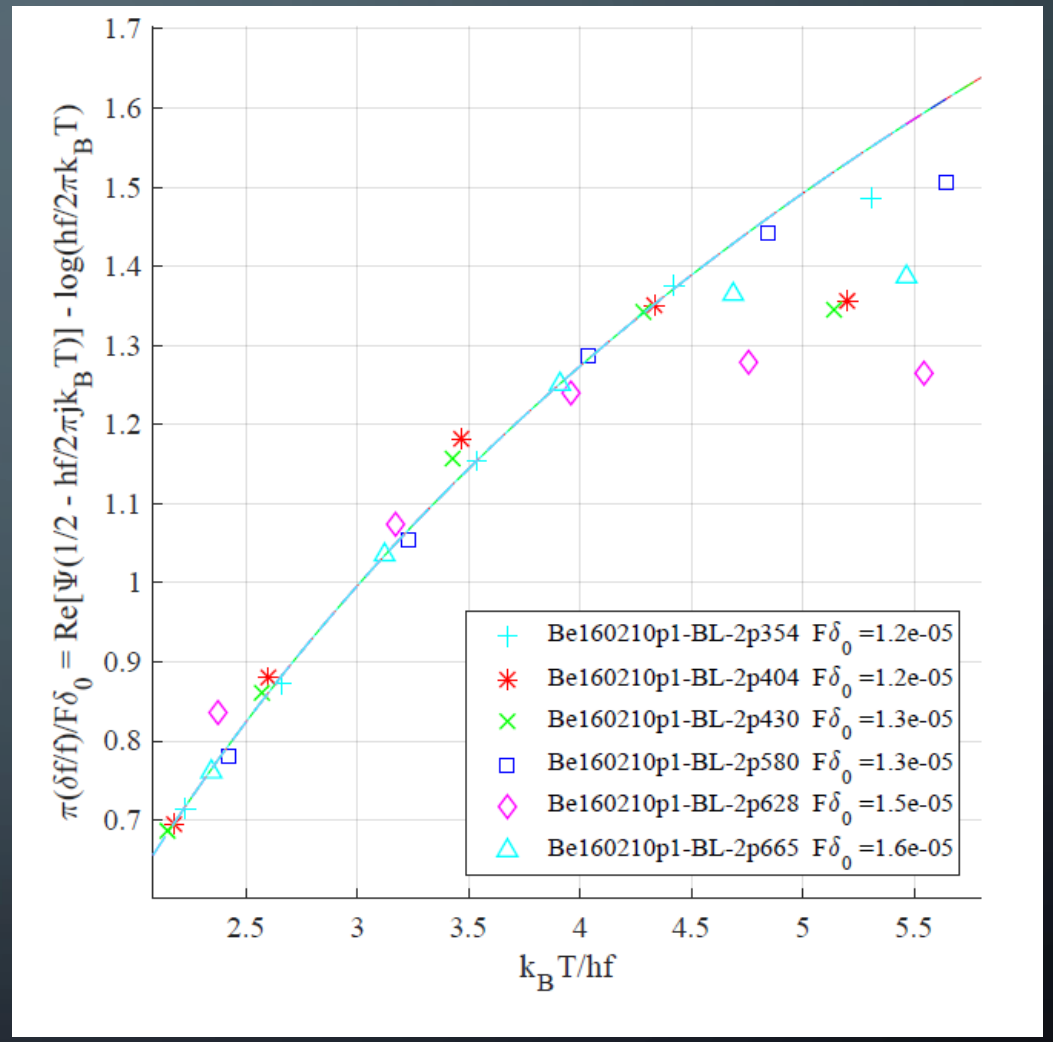


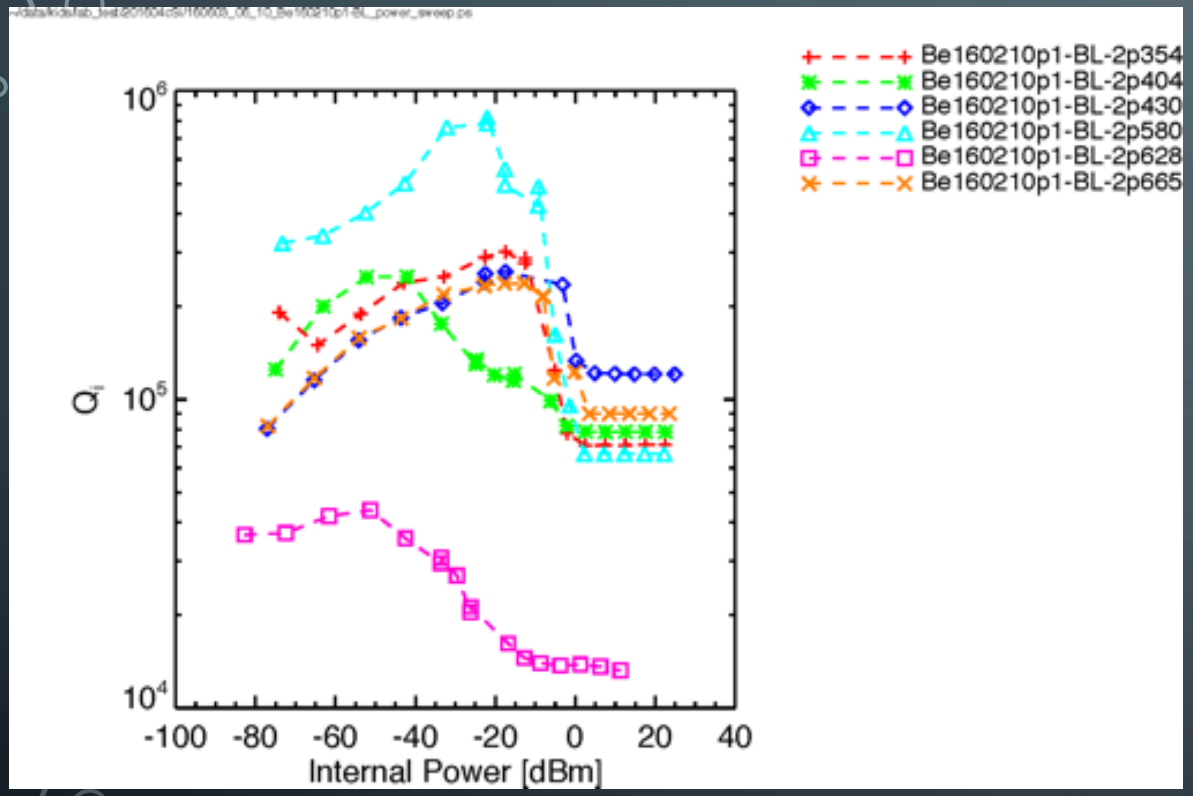
FIG. 3. (Color) Internal quality factor of aluminum resonators between 4 and 5 GHz. Devices which had the native oxide stripped from the top of the device layer (black) exhibited lower losses than devices with the native surface oxide present (blue). Black symbols {△,○,□}, correspond to $\omega_0/(2\pi)=\{4.99223, 4.05102, 4.91246\}$ GHz resonators, respectively. Blue symbols correspond to $\omega_0/(2\pi)=\{4.96406, 5.02214, 4.47342\}$ GHz resonators.

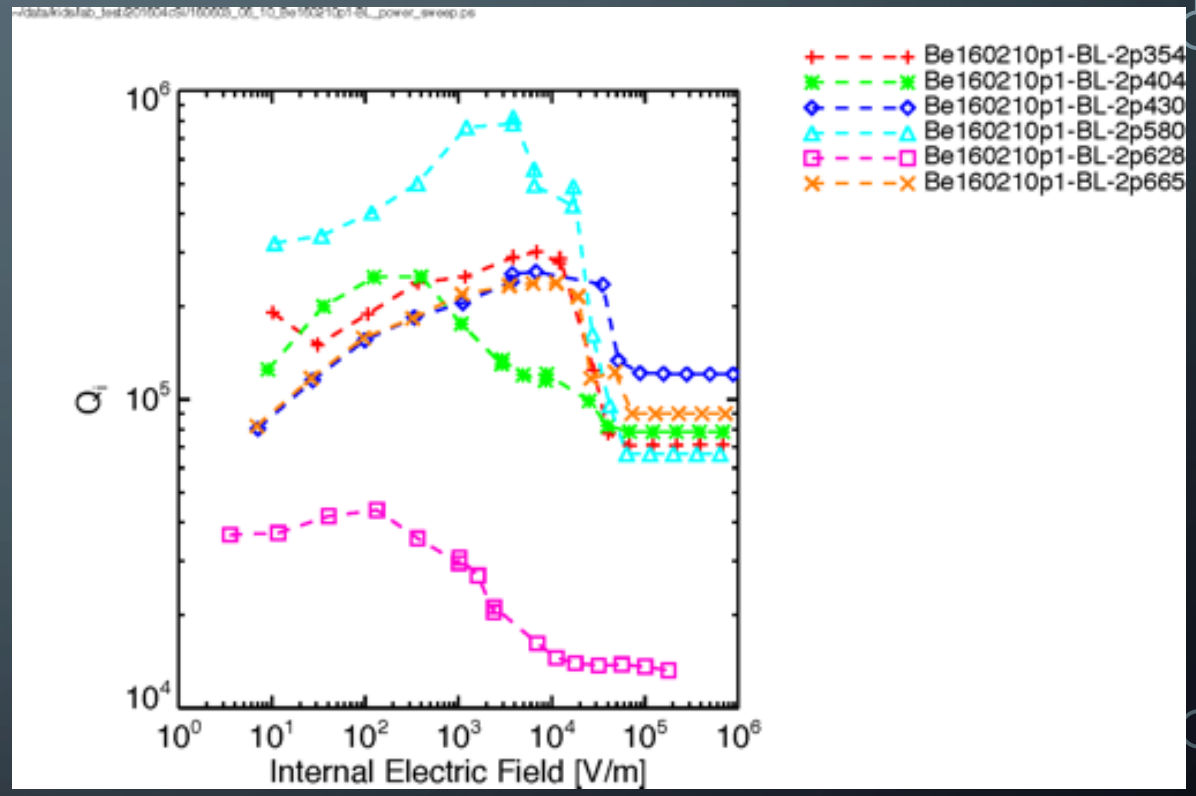
Weber *et. al.*, Appl. Phys. Lett. **98,** 172510 (2011); http://dx.doi.org/10.1063/1.3583449



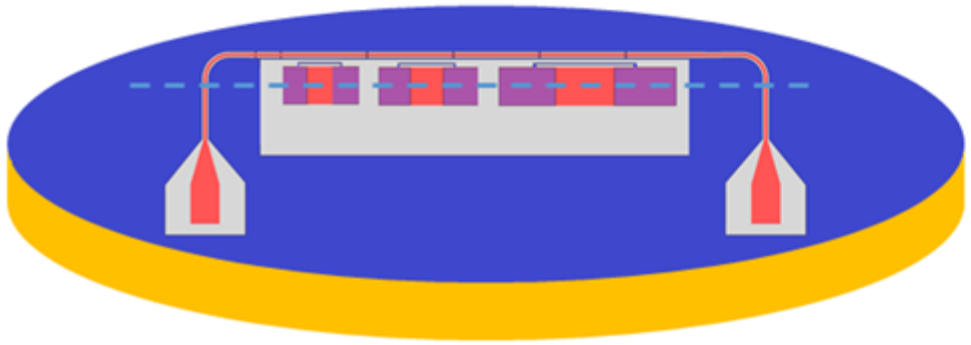
We get $F\delta_0$ =1-2 x 10^{-5}.

Control Experiment analysis





Goals



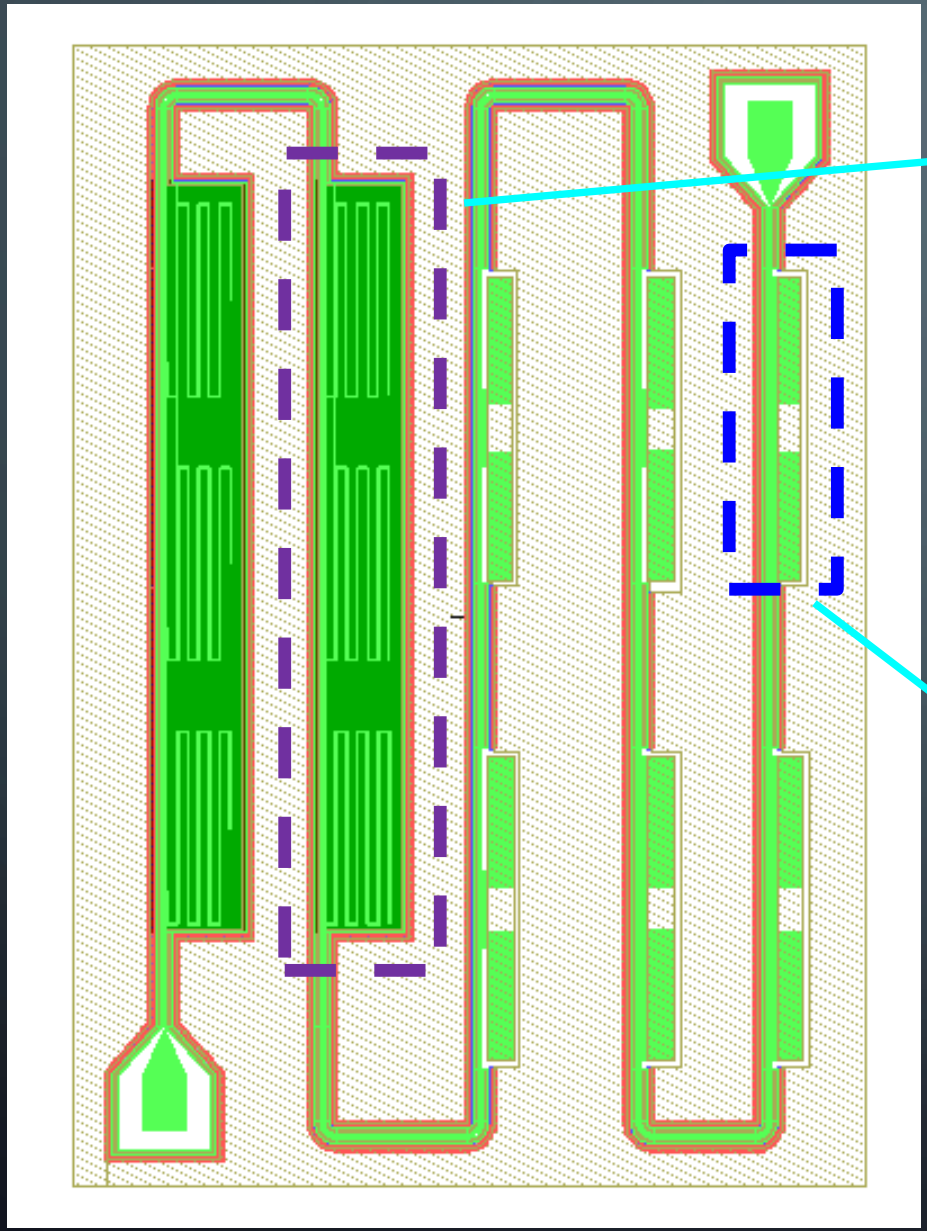
Control experiment

Wafer bond experiment

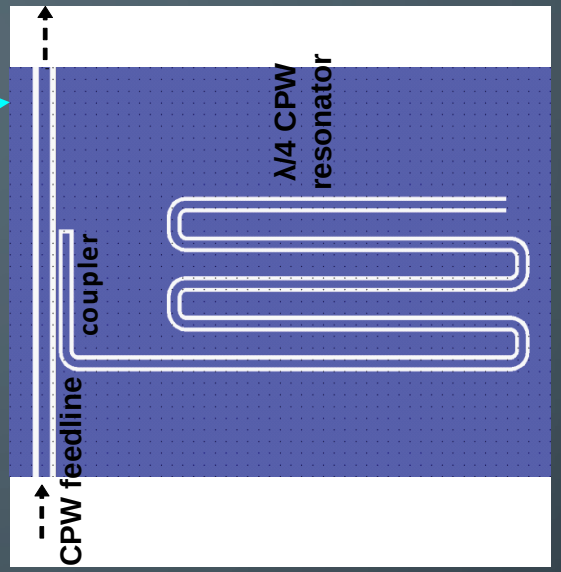
Goal 1: Develop control experiment to evaluate dielectric without wafer bonding.
Develop RF loss test device with device thickness of 5um then 1um using wafer bonding.

Goal 2: Develop mm-wave loss test device with device thickness of 5um then 1um with wafer bonding.

Goal 1 RF test structure



Alpha test structures:

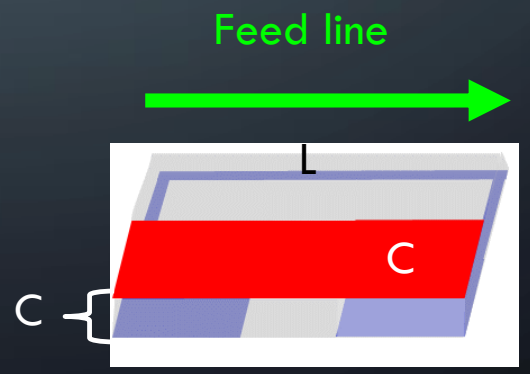


Direct determination of α from f_0.

α is the kinetic inductance fraction: $\alpha = L_{ki}/(L_{ki}+L_m)$.

Multiple CPW geometries allow one to determine α.

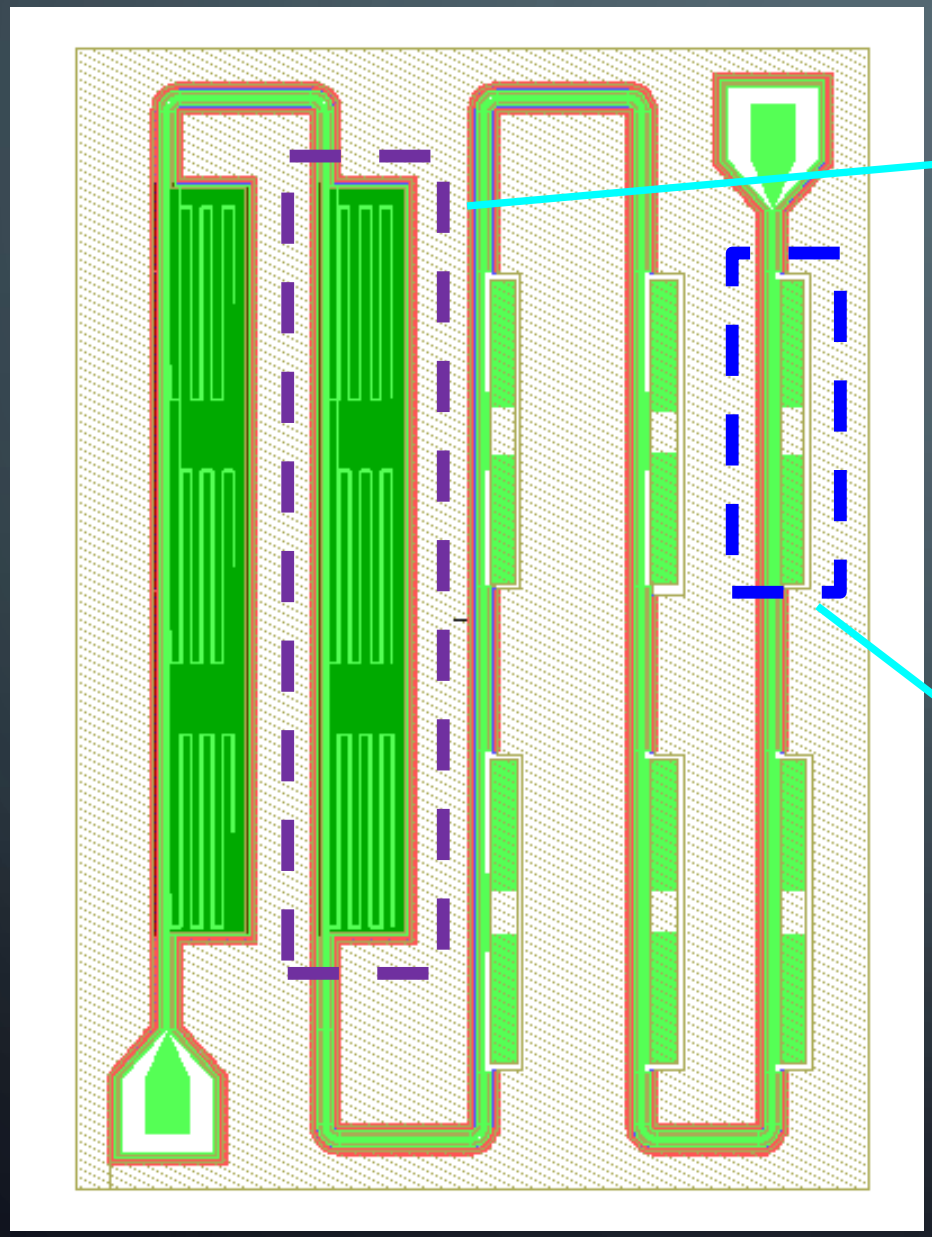
Dielectric test structures:



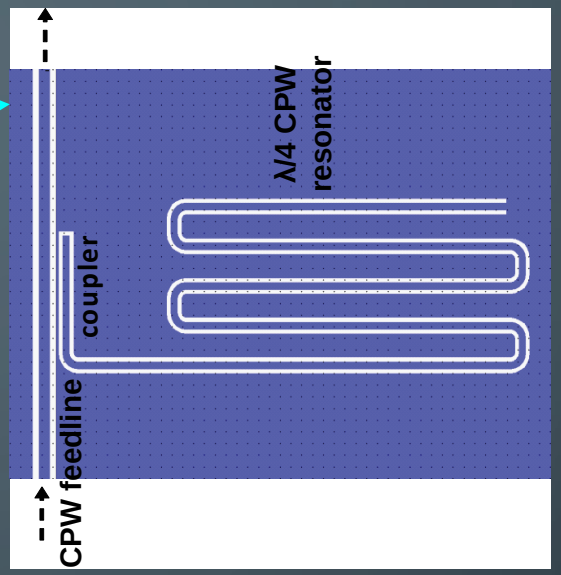
LC resonator test structure

Allows for determination of RF loss and measure of ε/d (ε: dielectric constant, d: thickness).

Goal 1 RF test structure



Metal loss test structures:

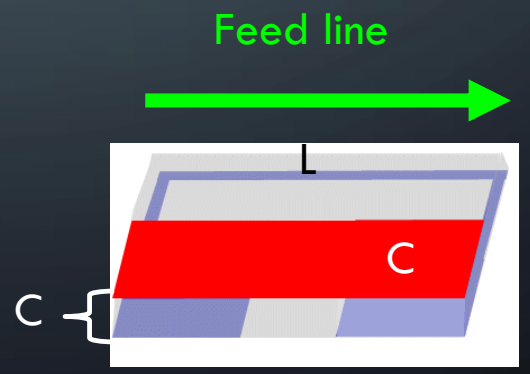


~~Direct determination of α from f_0.~~

~~α is the kinetic inductance fraction: α $=L_{ki}/(L_{ki}+L_m)$.~~

~~Multiple CPW geometries allow one to determine α.~~

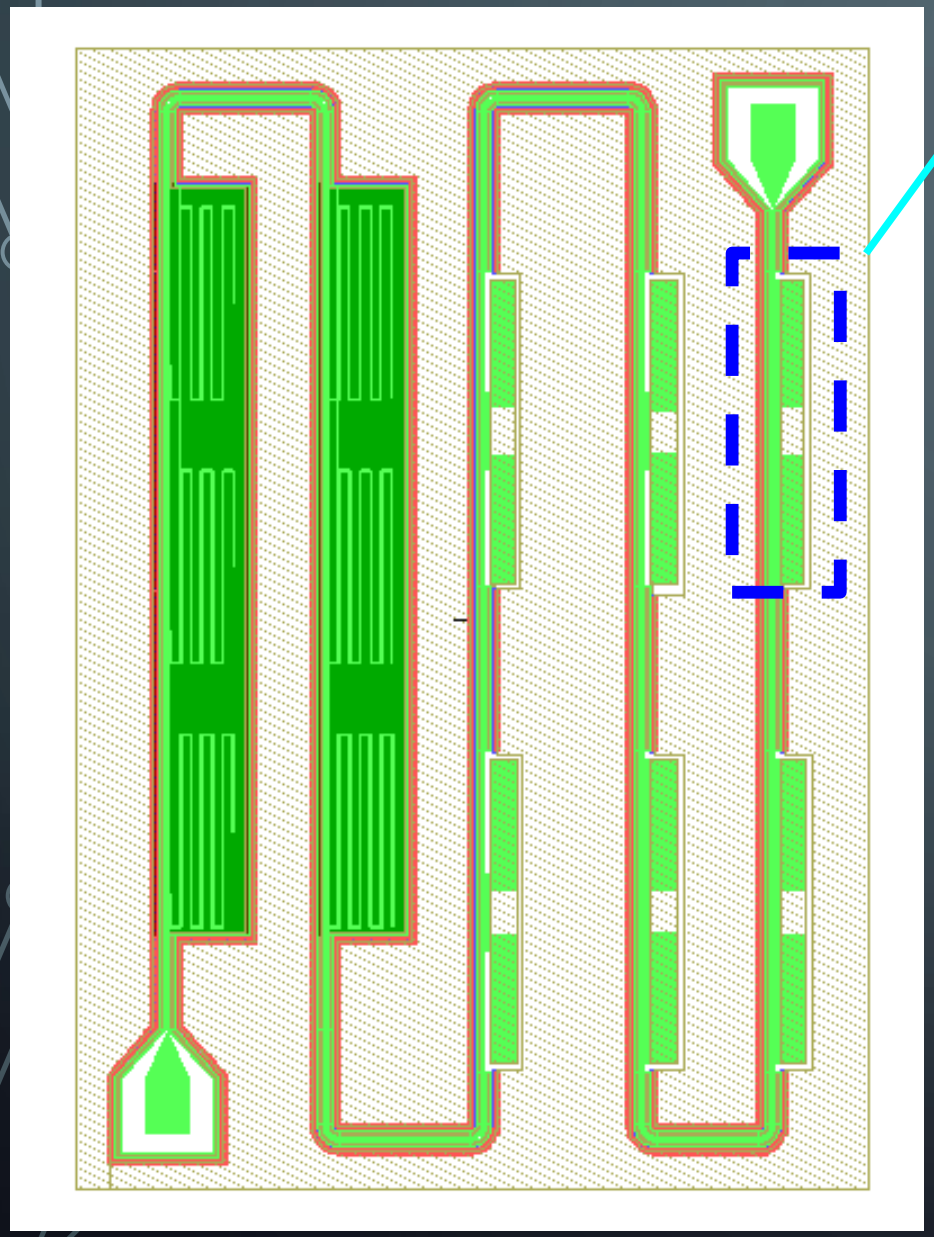
Dielectric test structures:



LC resonator test structure

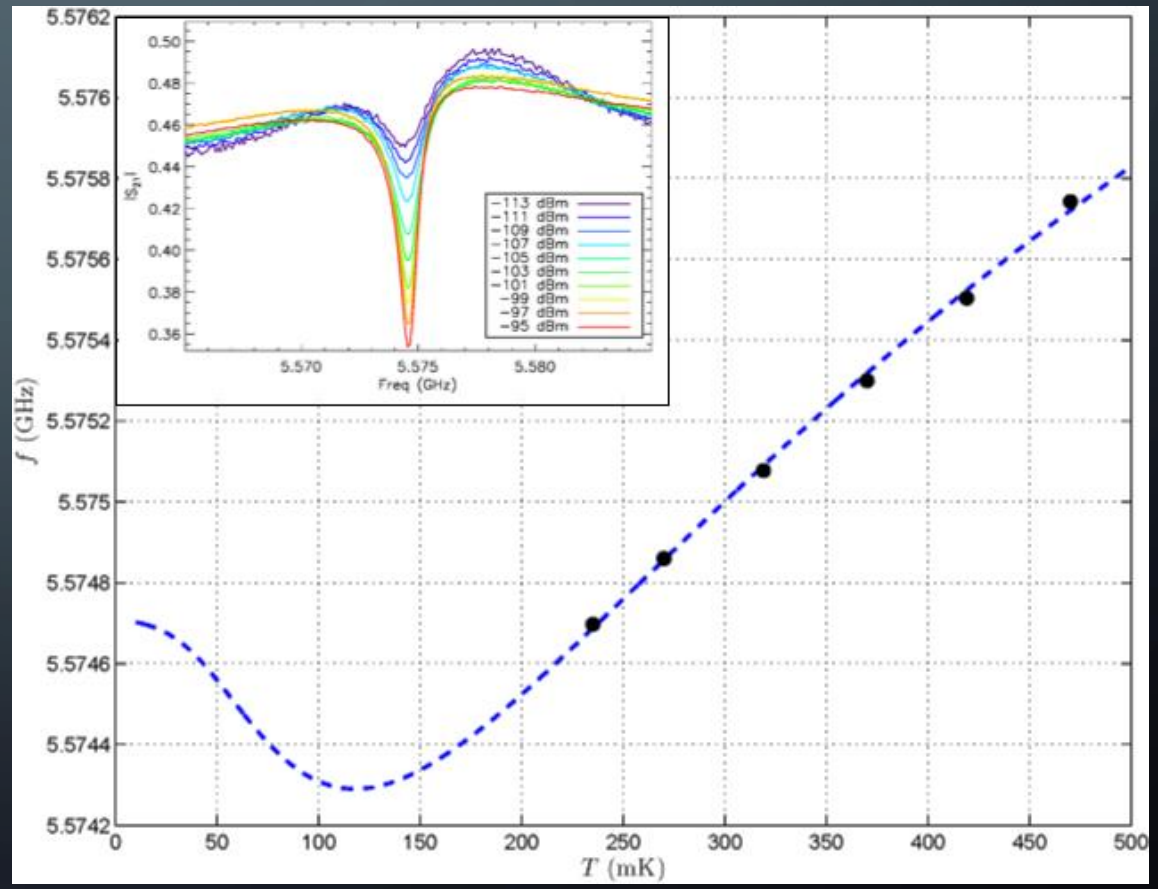
Allows for determination of RF loss and measure of ε/d (ε: dielectric constant, d: thickness).

Goal 1 RF test structure

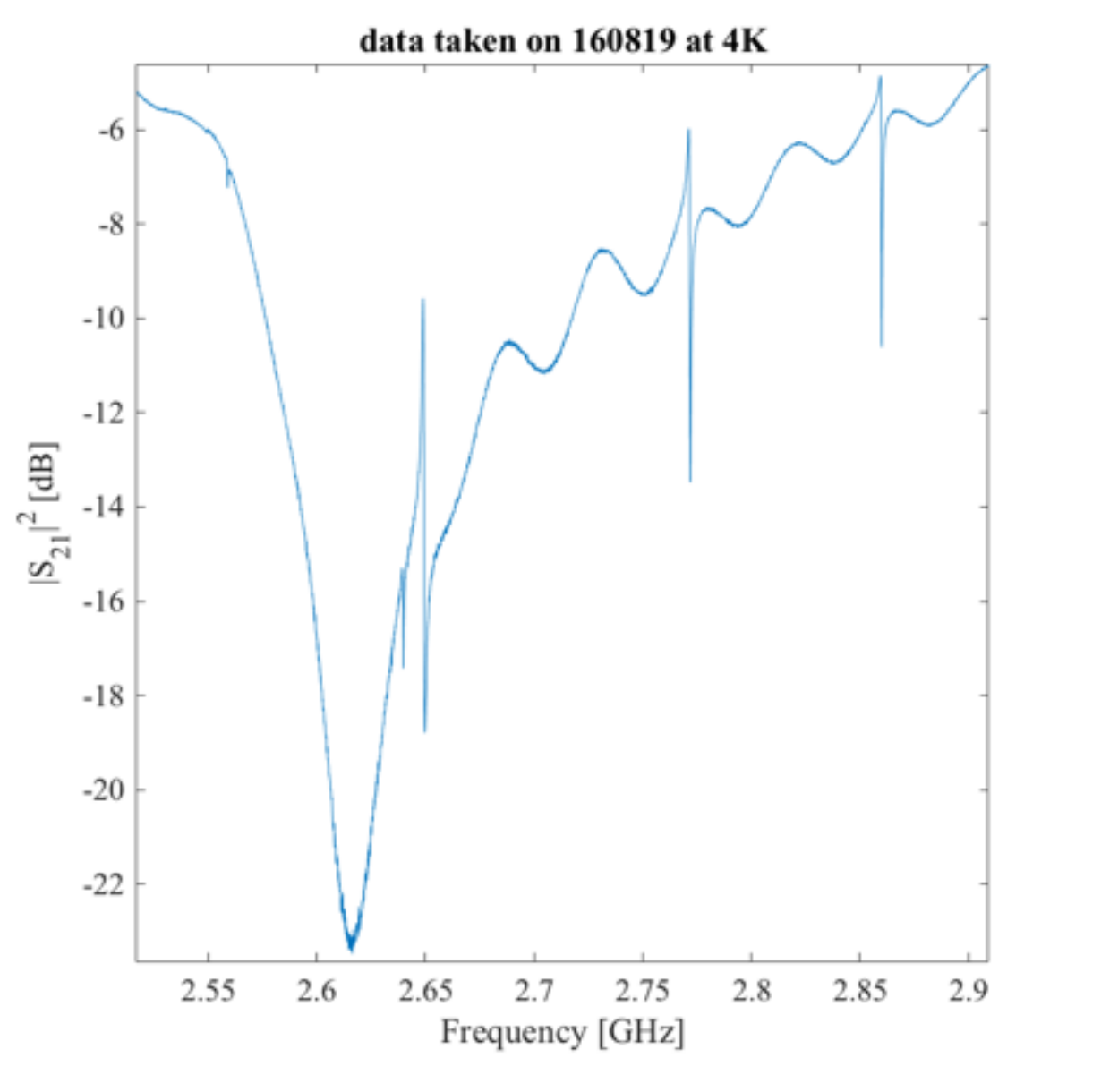


Dielectric test structures:

TLS noise at high readout power → KIDs typical operation. Resonator frequency shift is less sensitive to readout power → best measure of the zero-power loss tangent. Reflects the intrinsic properties of the dielectric and also best predicts the mm-wave loss tangent.

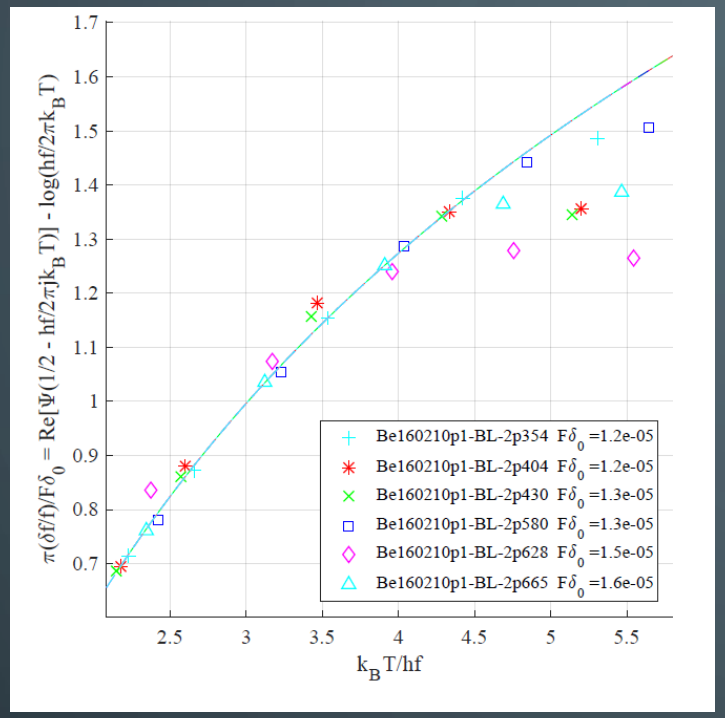


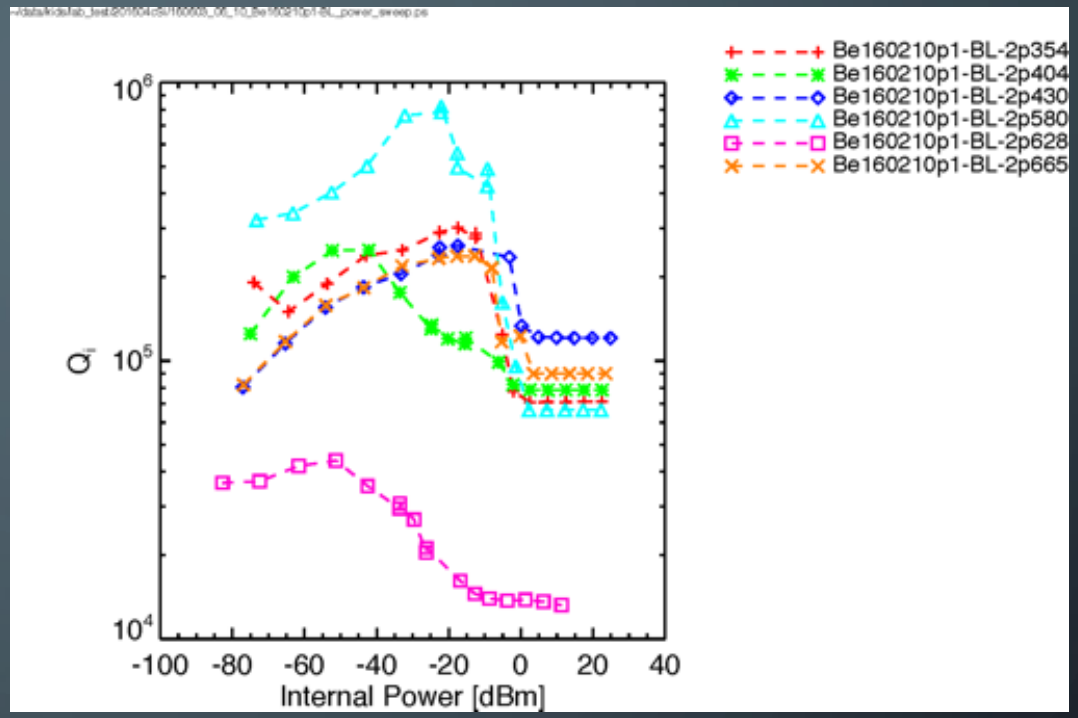
RF Wafer Bonded Device Experiment analysis



Device alive, and undergoing testing.

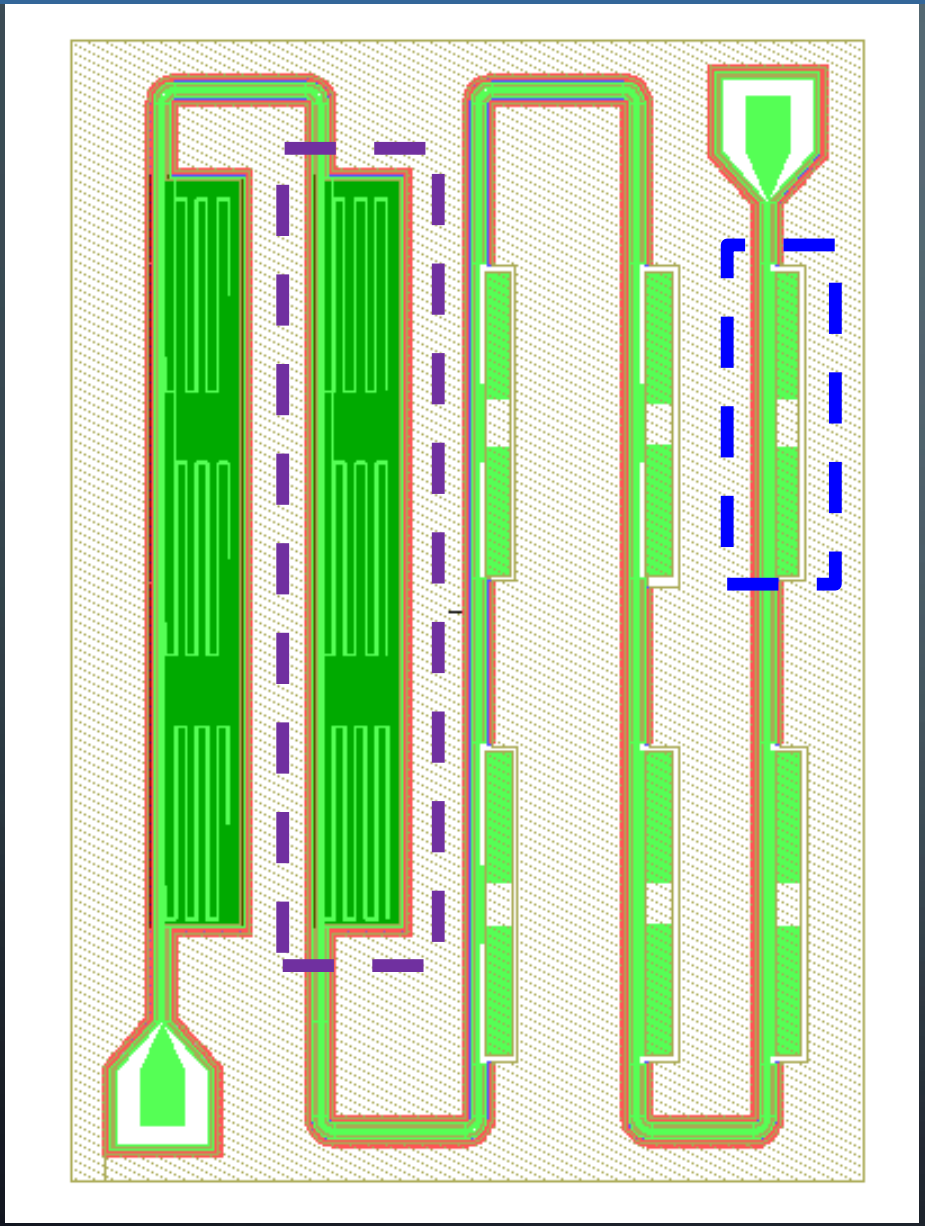
Conclusions

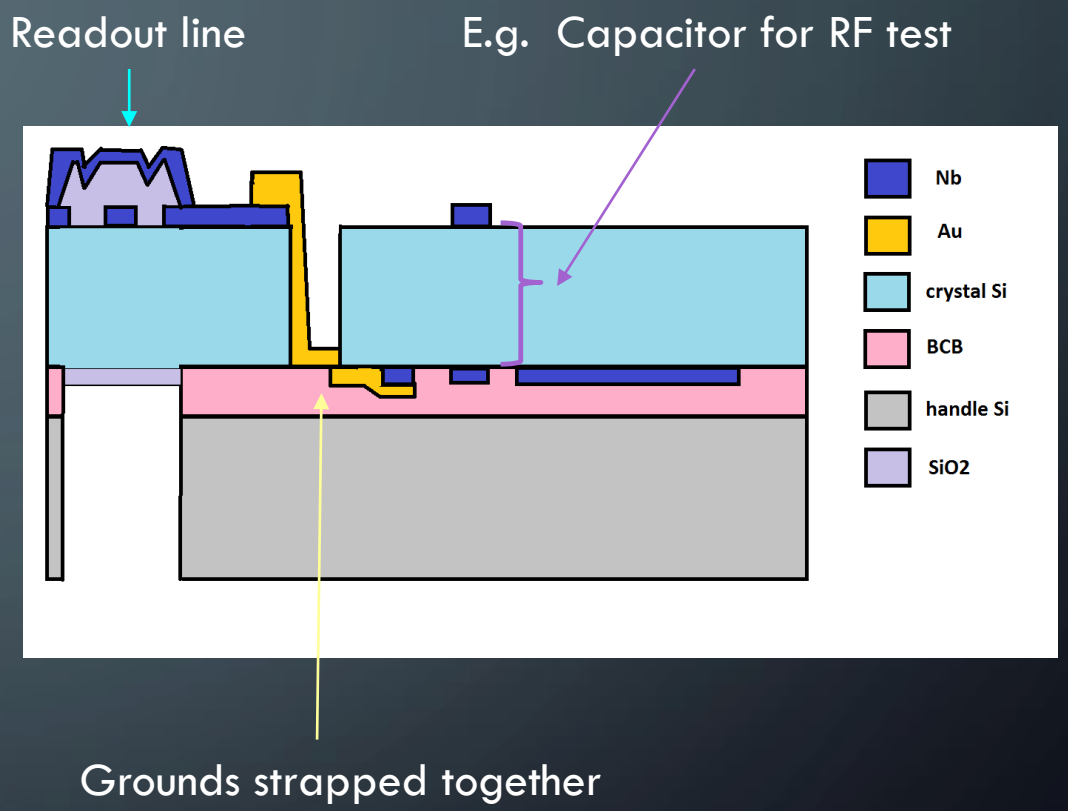


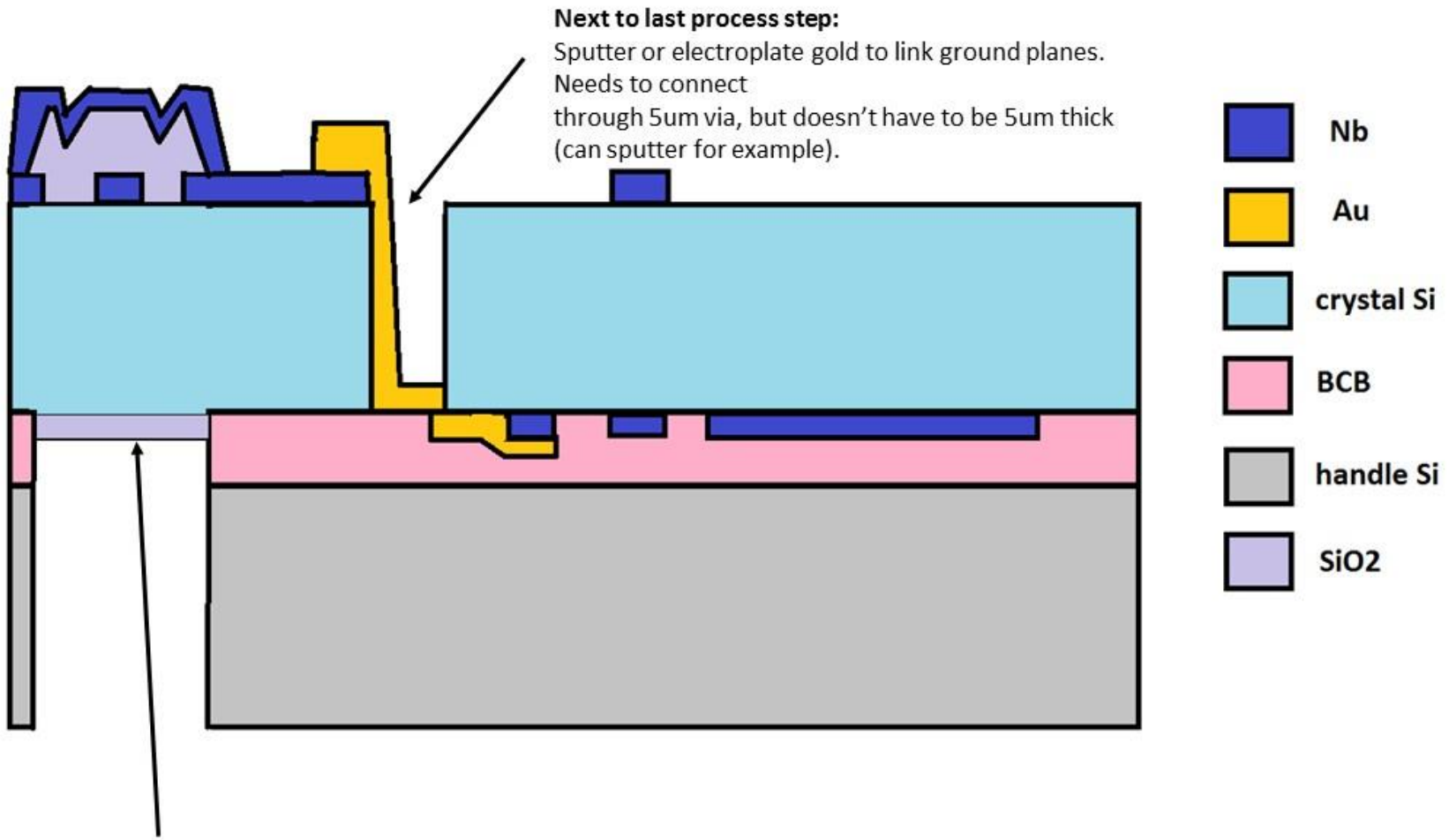


- Low loss confirmed in control test experiments, although factor of 3-6x best in literature.
- Successfully fabricated RF test structure using wafer bonding. More robust fab. process. Undergoing testing.

Year 1 RF test structure







DRIE last. SiO2 (or Au) used as a stop to keep from going through crystalline Si under CPWs.

DRIE last processing step. With DRIE photoresist still in place, etch away the SiO2 or Au stop before removing DRIE photoresist mask.

Adhesive bonding	Room temperature up to 400 °C Low to moderate bond pressure	+ high bond strength + low bond temperature + works practically with any substrate material including electronic wafers − no hermetic bonds − limited temperatures stability	MEMS, Sensor packaging, 3D-ICs, temporary bonds

TABLE I. Commonly used wafer bonding techniques (Refs. 1–15).

Wafer bonding technique	Typical bonding conditions	Advantages and disadvantages	Application areas
Direct bonding	600–1200 °C Room-temperature schemes have been reported Small or no bond pressure	+ high bond strength + hermetic + resistant to high temperatures − high surface flatness required − high bond temperatures not always compatible with electronic wafers	SOI wafer fabrication
Anodic bonding	150–500 °C 200–1500 V No bond pressure	+ high bond strength + hermetic + resistant to high temperature − bond temperatures in combination with voltage not always compatible with electronic wafers	Sensor packaging
Solder bonding	150–450 °C Low bond pressure	+ high bond strength + hermetic + compatible with electronic wafers − solder flux	Bump and flip-chip bonding
Eutectic bonding	200–400 °C Low to moderate bond pressure	+ high bond strength + hermetic + compatible with electronic wafers − sensitive to native oxides at surfaces	Hermetic packaging Bump and flip-chip bonding
Thermocompression bonding and direct metal-to-metal bonding	350–600 °C 100–800 MPa (high bond pressure)	+ hermetic + compatible with electronic wafers − very high net forces for full wafer bonding required − high surface flatness required	Wire bonding Bump and flip-chip bonding, e.g., 3D-ICs
Ultrasonic bonding	Room temperature up to 250 °C High bond pressure	+ compatible with electronic wafers − only demonstrated for small bond areas	Wire bonding
Low-temperature melting glass bonding	400–1100 °C Low to moderate bond pressure	+ high bond strength + hermetic − bond temperatures not always compatible with electronic wafers	Sensor packaging
Adhesive bonding	Room temperature up to 400 °C Low to moderate bond pressure	+ high bond strength + low bond temperature + works practically with any substrate material including electronic wafers − no hermetic bonds − limited temperatures stability	MEMS, Sensor packaging, 3D-ICs, temporary bonds