MIL/JEDEC Standards Update

2016 Electronics Technology Workshop (ETW)

NASA Electronic Parts and Packaging Program (NEPP)

GSFC, Greenbelt, Maryland
June 13-16, 2016

S. Agarwal
NASA - Jet Propulsion Laboratory, California Institute of Technology
Pasadena, California, USA
Shri.g.agarwal@jpl.nasa.gov

The Rover Environmental Monitoring Station (REMS) on NASA's Curiosity Mars rover includes temperature and humidity sensors mounted on the rover's mast. One of the REMS booms extends to the left from the mast in this view.
Image credit: NASA/JPL-Caltech/MSSS

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Abstract

MIL/JEDEC standards play a vital role in electronic parts procurement and usage on all NASA missions. Through the NASA Electronic Parts Assurance Group (NEPAG) Program, NASA is an active participant in work related to the standards as they apply to electronic parts. This paper will provide an update on those activities.

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NEPAG Partnering with Industry Groups

- **JEDEC JC13 (Manufacturers), and**
- **SAE SSTC G11/G12 (Users)**

JEDEC JC13

JC-13	Solid State Devices for Government Products
JC-13.1	Discrete Semiconductors for Government Products
JC-13.2	Microelectronics for Government Products
JC-13.4	Radiation Hardness
JC-13.5	Hybrids and MCMs for Government Products
JC-13.7	New Electronic Device Insertion for Government Products

SSTC G11/G12

SAE SSTC G-11	Users of Passive Components
SAE SSTC G-12	Users of Solid State Devices

G12 Management:

Chair – A. Touw

Vice Chair – S. Agarwal

Joint JEDEC and G12 meetings are held 3 time a year. NEPAG is an active participant in those meetings. NEPAG's Shri Agarwal was recently appointed as the vice chair of G12.

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JEDEC/G11/G12 Meetings

- **JC13.x/G11/G12 Meetings**
  - The JEDEC/G11/G12 meetings are held three times a year. The first meeting of FY16 was held in Jan 2016.
  - NASA participation:
    - Organize NEPAG meetings
    - Active involvement in Task Group meetings
      - JC13.1, 13.2, 13.4, 13.5, 13.7, and G11/G12
    - G-12 Management
      - Participate in Executive Council meetings
      - Take notes of G12 meetings
      - Help with Task Group meetings

*JEDEC (Joint Electron Device Engineering Council) is a standardization body composed of semiconductor device manufacturers and their supply chains. SAE (Society of Automotive Engineers) coordinates development of technical standards by aerospace, automotive, and other users. Held three times a year, these meetings are key to parts standardization including the infusion of new technology.

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Grid for JEDEC/G11/G12 meetings (Example: Jan2016)

San Antonio, Texas — PRELIMINARY Meeting Schedule — January 2015

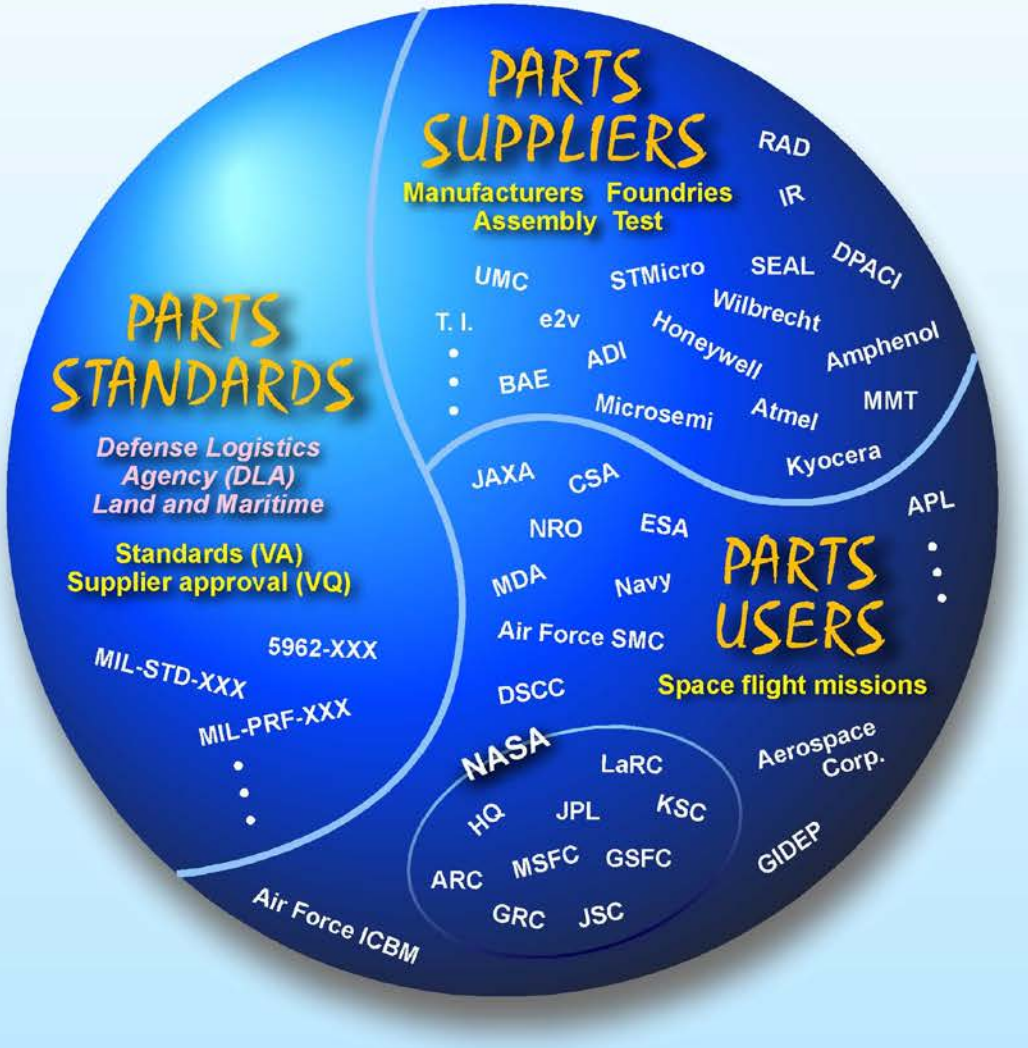
Day	Room	7:30 AM	8:00 AM	9:00 AM	10:00 AM	11:00 AM	12:00 PM	1:00 PM	2:00 PM	3:00 PM	4:00 PM	5:00 PM	6 PM	7PM
Mon 1/12	A					JC-13 Digital vs. Film Xray TM & Req		G-12 PEM Qual and Screening Flow	G-12 Plastics Sub- Committee	Joint JC-13.7 Copper Wirebonds	Joint JC-13.7/G-12 New Electronic Device			
	B							JC-13.1 Technical 750 Test Method Review						
	C						JC-13 ExCo Mtg (by invitation)	JC-13.5 PI / QML Discussion and Other General Issues				NEPAG Meeting (25 Attendees)		
Day	Room	7:30 AM	8:00 AM	9:00 AM	10:00 AM	11:00 AM	12:00 PM	1:00 PM	2:00 PM	3:00 PM	4:00 PM	5:00 PM	6 PM	7PM
Tues 1/13	A	New Member Orientation	JC-13 J-STD-002 (Solderability) Use in 750 and 883	G-12 Wear-out	JC-13.2 Electronic Parameters & B/I Standardization	JC-13 TJ Req		JC-13 / G-12 Joint Meeting	G-12 General Session	G-12 / JC-13 Trusted Sources	G-12 & G-11 Counterfeit Mitigation Subcommittee			
	B				JC-13.1 MIL-PRF-19500P Appendix J				JC-13.1 MIL-PRF-19500R			JC-13.1 Industry Feedback to DLA: 750 Test Methods and Slash Sheets		
	C			JC-13.5 Review Element Eval. Req. 38534					JC-13.5 Package Element Eval	JC-13.5 TG172 QML Requirements				
	D		JC-13.4 Subcommittee Meeting											
Day	Room	7:30 AM	8:00 AM	9:00 AM	10:00 AM	11:00 AM	12:00 PM	1:00 PM	2:00 PM	3:00 PM	4:00 PM	5:00 PM	6PM	7PM
Wed 1/14	A		JC-13.2 JEP-121 (8:30)	Joint JC-13.2/G-12 Meeting (9:30)				Joint JC-13.5/G-12 Meeting		Joint JC-13.1/G-12 Meeting		G-12 & G-11 Space Subcommittee		
	B			JC-13.1/13.7/G-12 New Technology in 19500				Standardization of SMD Carrier Packages						
	C		JC-13.5 Subcommittee Meeting							JC-13.5 Subcommittee Meeting				
	D		JC-13 / G-12 / G-11 BMEs	G-11 Committee Meeting				G-11 Committee Meeting						
	E		G-12 Radiation RHA Subcommittee					ASTM Meeting						
Day	Room	7:30 AM	8:00 AM	9:00 AM	10:00 AM	11:00 AM	12:00 PM	1:00 PM	2:00 PM	3:00 PM	4:00 PM	5:00 PM	6PM	7PM
Thurs 1/15	A		JC-13 Leak Rate Issues (883 and 750)		G-12 Tech Talk: NASA Hermeticity Study	JC-13 RGA		JC-13 General Session		JC-13 ExCo Meeting (by invitation)				
	B		G-11 Committee Meeting											

- **NEPAG@JEDEC (circled above) is held to decide on member participation in JEDEC/G11/G12 meetings.**

NEPAG

Space Parts World

Develop/Maintain Standards for Space Electronic Parts



The parts users and standards organizations work with suppliers to ensure availability of standard parts for NASA, DoD and others. **For Space microcircuits, DLA, NASA/JPL (S. Agarwal) and the U.S. Air Force / Aerospace Corp. (L. Harzstark) form the Qualifying Activity (QA).**

Specific Activities
JC13.5 – Class Y

- **Class Y**
  - Created for complex ceramic based non-hermetic microcircuits.
  - Introduced PIDTP
    - Package integrity demonstration test plan
    - Also applies to Class V, reference: MIL-PRF-38535, Revision K
  - QML Certification Status
    - Column Attach Service Providers with Class Y (and V) certification
      - Six Sigma, Milpitas, California
      - Astrium (Airbus), Paris, France (columns similar to Six Sigma)
      - Micross Components, Crewe, U. K. (columns similar to IBM)
    - Manufacturers
      - Aeroflex Cobham (Has certification)
      - Honeywell (Actively pursuing certification)
      - Xilinx (Planned)
      - E2v (Planned)

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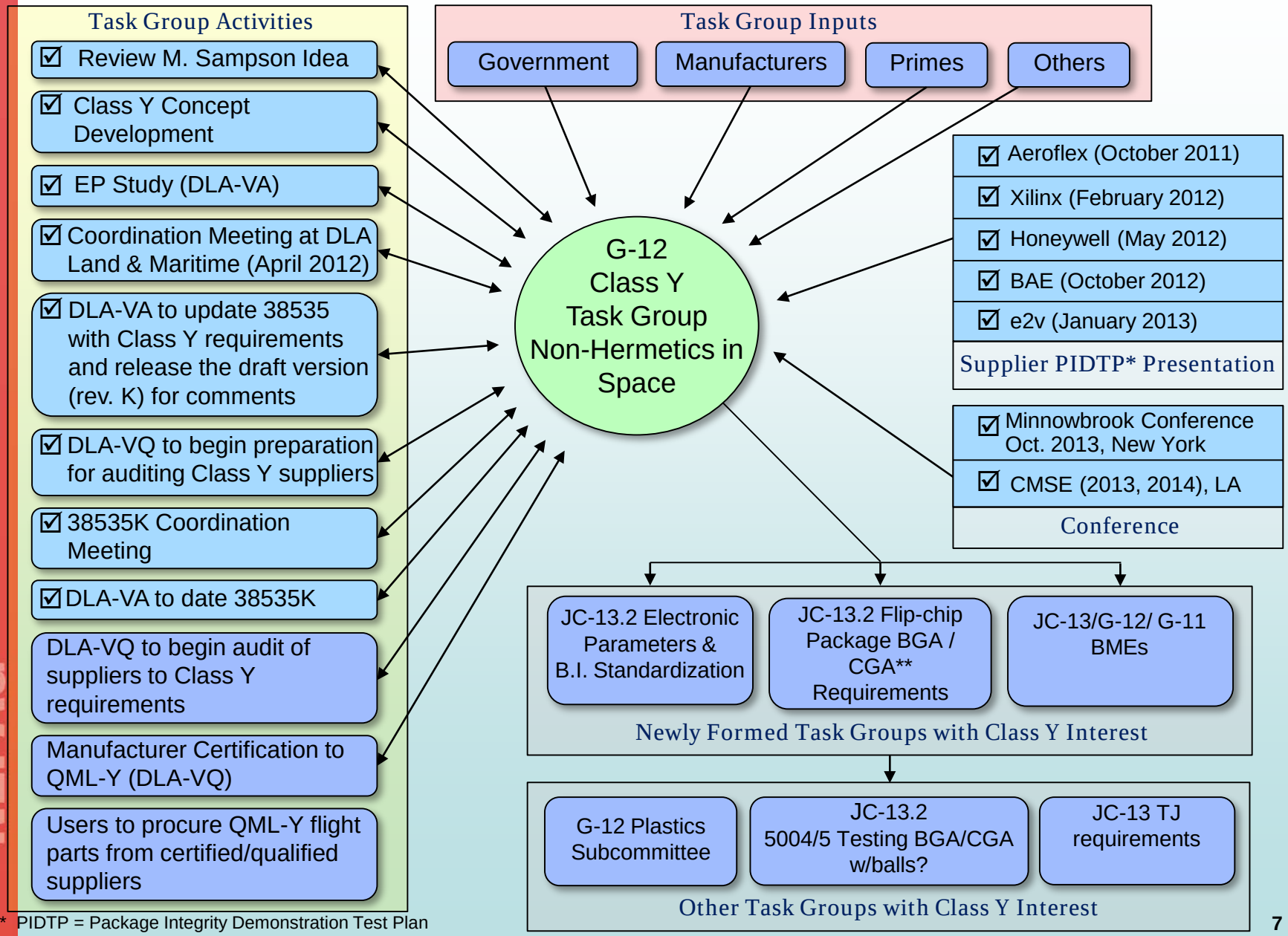
Infusion of New Technology into Military Standards
NASA Led the Class Y Effort for Xilinx V4/V5 FPGAs and other similar Devices
Shows the Extent of Effort/Coordination



* PIDTP = Package Integrity Demonstration Test Plan
** BGA / CGA = ball-grid array / column-grid array

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Specific Activities
JC13.4 – Radiation Test Standard JESD57

- **JESD57 Test Standard**
  - Contains procedures for the measurement of single-event effects in semiconductor devices from heavy-ion irradiation.
  - Only U. S. test standard covering many of the heavy-ion induced single-event effects.
  - Last updated 20 years ago (in 1996)
    - Does not reflect advanced electronics and complex technologies
  - A new revision will soon be submitted for a vote.
    - NASA NEPP-led effort
    - Point of contact: Jean-Marie Lauenstein

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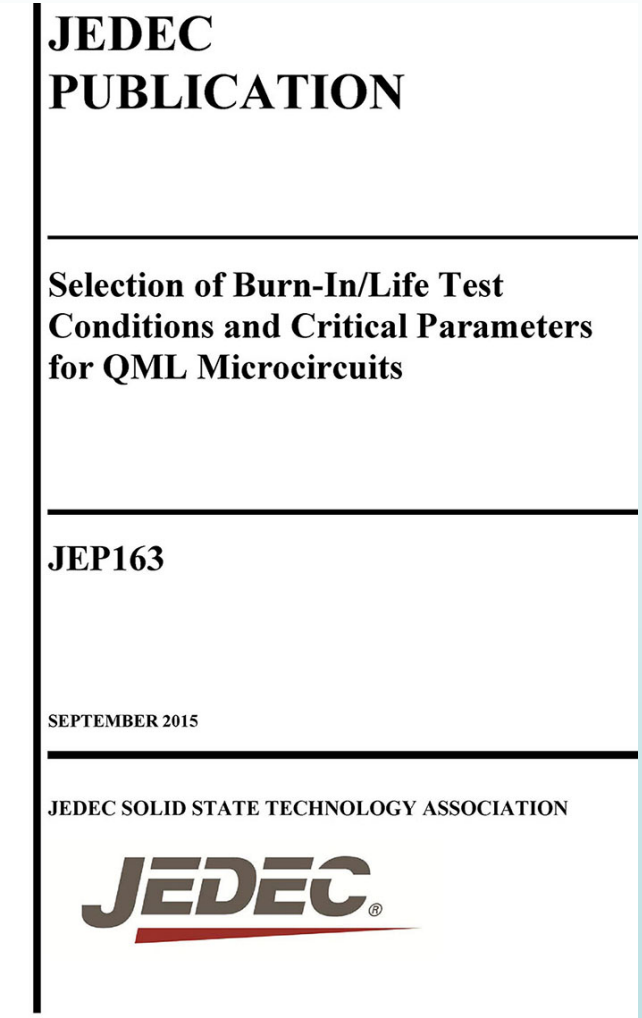
Updating MIL-STD-883, an Example
Burn-in of Monolithic Microcircuits

- The requirements in MIL-STD-883
  - Last update was 25 years ago
  - Now, outdated. Does not reflect the current technology.
- A JEDEC task group was formed to look at
  - Burn-in, electrical test and delta requirements
    - Different technologies and devices
- Status
  - Published Guideline document JEP163.
  - Task Group is still open to address new concerns.
  - DLA's Engineering Practice (EP) study on burn-in is in progress


JEDEC
PUBLICATION

Selection of Burn-In/Life Test Conditions and Critical Parameters for QML Microcircuits

JEP163

SEPTEMBER 2015

JEDEC SOLID STATE TECHNOLOGY ASSOCIATION

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Updating Requirements, an Example
Burn-in of Monolithic Microcircuits

- A New Concern
  - Burn-in of high-speed devices
    - What about hot spots on the die?
- **Frequencies**
  - 500 MHz for digital functions
  - A few giga-samples per second (Gsps) for data converters
  - Several tens of gigahertz (GHz) for analog functions
- Status
  - To be addressed in the Task Group

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Dual Use Technology

- Basically an infusion of commercial monolithic microcircuits into DoD system.
  - Rad hard by design 45nm CMOS microelectronics technology (BAE Systems, built at IBM foundry)
  - Adding their unique processing steps to the existing processes, e.g. MRAMs being offered by Aeroflex and Honeywell (done in collaboration with Everspin)
  - Upscreening selected products from commercial portfolio (Analog Devices)

- This has resulted in paradigm changes. An example follows:
  - Not all parts are specified over the full military temperature range, –55°C to +125°C. Many of them call out –40°C to +110°C operating temperature range. These differences are now clearly shown in the standard microcircuit drawings (SMDs). However, there are **no** guidelines for BI of these devices. (Per notes 3/ and 4/ of the regression table, doing BI at temperatures lower than 125°C is not allowed for monolithic microcircuits.)
  - It is unclear what assumptions went into generating the numbers.

MIL-STD-883J
w/CHANGE 1

TABLE I. Burn-in time-temperature regression. 1/ 2/ 3/ 4/

Minimum temperature T_A (°C)	Minimum time (hours)			Test condition (see 3.1)	Minimum reburn-in time (hours)
	Class level S	Class level B	Class level S hybrids (Class K)		
100	---	352	700	Hybrids only	24
105	---	300	600	"	24
110	---	260	520	"	24
115	---	220	440	"	24
120	---	190	380	"	24
125	240	160	320	A - E	24
130	208	138	---	"	21
135	180	120	---	"	18
140	160	105	---	"	16
145	140	92	---	"	14
150	120	80	---	"	12
175	---	48	---	F	12
200	---	28	---	"	12
225	---	16	---	"	12
250	---	12	---	"	12

1/ Test condition F shall be authorized prior to use and consists of temperatures 175°C and higher.
2/ For condition F the maximum junction temperature is unlimited and care shall be taken to ensure the device(s) does not go into thermal runaway.
3/ The only allowed conditions are as stated above.
4/ Test temperatures below 125°C may be used for hybrid circuits only.

METHOD 1015.10
26 February 2010

NEPAG

MIL-STD-883, Test Method 1005

MIL-STD-883J
w/CHANGE 1

TABLE I. Steady-state time temperature regression. 1/ 2/ 3/ 4/

Minimum temperature T_A (°C)	Minimum time (hours)			Test condition (see 3.5)
	Class level S	Class level B	Class level S hybrids (Class K)	
100		7500	7500	Hybrid only
105		4500	4500	"
110		3000	3000	"
115		2000	2000	"
120		1500	1500	"
125	1000	1000	1000	A -E
130	900	704	---	"
135	800	496	---	"
140	700	352	---	"
145	600	256	---	"
150	500	184	---	"
175		40	---	F
180		32	---	"
185		31	---	"
190		30	---	"

1/ Test condition F shall be authorized prior to use and consists of temperatures 175°C and higher.
2/ For condition F the maximum junction temperature is unlimited and care shall be taken to ensure the device(s) does not go into thermal runaway.
3/ The only allowed conditions are as stated above.
4/ Test temperatures below 125°C may be used for hybrid circuits only.

METHOD 1005.9
26 February 2010

- Life test below 125°C not allowed for monolithic microcircuits.

New Technology Flip-chip Devices

- **Use of Underfills**
  - The use of underfill material enhances reliability of flip-chip packages.
  - MIL-PRF-38535K requires flip-chip devices to meet the underfill requirements specified in MIL-STD-883, Test Method 5011.
  - Several manufacturers are developing flip-chip products (Classes V and Y). It was reported that there were problems in meeting the requirements in 5011. A JEDEC Task Group was formed to address this issue.

- **Activities**
  - In order to bring the subject matter awareness, NASA published a special edition of EEE Parts Bulletin on **underfills**.
  - Defense Logistics Agency (DLA) conducted an **Engineering Practice (EP) study**
  - Considerable discussion held in Jacksonville, Florida. Actions in progress are:
    - Space community and DLA to come up with set of requirements
    - Review those requirements with manufacturers of flip-chip devices

- **Status (monitored by S. Agarwal)**
  - A tentative plan developed to continue audits until the requirements in 5011 and/or 38535 are updated.
  - The discussion will continue in New Orleans
    - 1 hour allotted at the June JEDEC

Special Edition of NASA Parts Bulletin on Flip-chip Underfills

- NASA EEE Parts Bulletin (June–July 2015)

National Aeronautics and Space Administration

EEE Parts Bulletin

Electrical, Electronic, and Electromechanical

A periodic newsletter of the JPL/OSMS Assurance Technology Program Office (ATPO), NASA EEE Parts Assurance Group (NEPAG), and Section 514, of the Jet Propulsion Laboratory.

June–July, 2015 • Volume 7 • Issue 2 (Published since 2009)

Special Issue

Flip-Chip Underfills

This is a special edition of the NASA *EEE Parts Bulletin* that brings awareness of the issues currently being worked as part of the new technologies for space applications, in this case, flip-chip underfills. The following articles were written by NASA specialists. The first introduces the subject matter, and the second describes the results of evaluations conducted for the NASA Electronic Parts and Packaging (NEPP) program. Also included is a third article noting the parallel effort by the Defense Logistics Agency (DLA) to elicit input from the manufacturing and user communities regarding development of test requirements for flip-chip underfills.

Cross section of a flip-chip die (top) with underfill fillet keyed to two diagrams (middle) showing the location and general arrangement of underfill around the chip components. Right diagram shows relationship to enlarged view of fillet (bottom) at 20 µm. (Photographs and micrographs were generated by R. Ruiz.)

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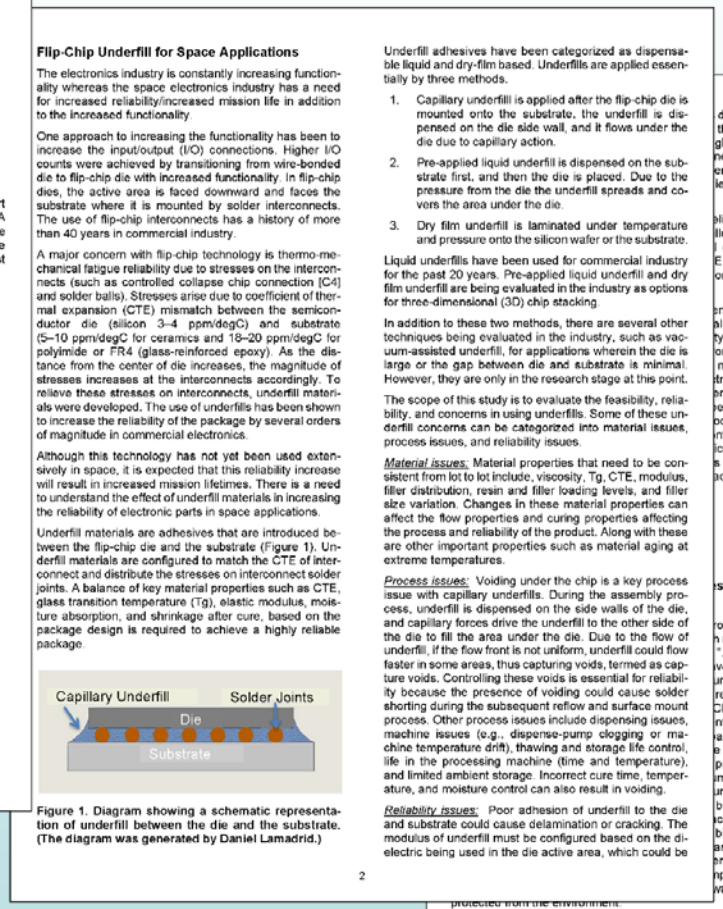


Flip-Chip Underfill for Space Applications

The electronics industry is constantly increasing functionality whereas the space electronics industry has a need for increased reliability/increased mission life in addition to the increased functionality.

One approach to increasing the functionality has been to increase the input/output (I/O) connections. Higher I/O counts were achieved by transitioning from wire-bonded die to flip-chip die with increased functionality. In flip-chip dies, the active area is faced downward and faces the substrate where it is mounted by solder interconnects. The use of flip-chip interconnects has a history of more than 40 years in commercial industry.

A major concern with flip-chip technology is thermo-mechanical fatigue reliability due to stresses on the interconnects (such as controlled collapse chip connection [C4] and solder balls). Stresses arise due to coefficient of thermal expansion (CTE) mismatch between the semiconductor die (silicon 3–4 ppm/degC) and substrate (5–10 ppm/degC for ceramics and 18–20 ppm/degC for polyimide or FR4 (glass-reinforced epoxy). As the distance from the center of die increases, the magnitude of stresses increases at the interconnects accordingly. To relieve these stresses on interconnects, underfill materials were developed. The use of underfills has been shown to increase the reliability of the package by several orders of magnitude in commercial electronics.

Although this technology has not yet been used extensively in space, it is expected that this reliability increase will result in increased mission lifetimes. There is a need to understand the effect of underfill materials in increasing the reliability of electronic parts in space applications.

Underfill materials are adhesives that are introduced between the flip-chip die and the substrate (Figure 1). Underfill materials are configured to match the CTE of interconnect and distribute the stresses on interconnect solder joints. A balance of key material properties such as CTE, glass transition temperature (Tg), elastic modulus, moisture absorption, and shrinkage after cure, based on the package design is required to achieve a highly reliable package.

Figure 1. Diagram showing a schematic representation of underfill between the die and the substrate. (The diagram was generated by Daniel Lamadrid.)

Underfill adhesives have been categorized as dispensable liquid and dry-film based. Underfills are applied essentially by three methods.

1. Capillary underfill is applied after the flip-chip die is mounted onto the substrate, the underfill is dispensed on the die side wall, and it flows under the die due to capillary action.
2. Pre-applied liquid underfill is dispensed on the substrate first, and then the die is placed. Due to the pressure from the die the underfill spreads and covers the area under the die.
3. Dry film underfill is laminated under temperature and pressure onto the silicon wafer or the substrate.

Liquid underfills have been used for commercial industry for the past 20 years. Pre-applied liquid underfill and dry film underfill are being evaluated in the industry as options for three-dimensional (3D) chip stacking.

In addition to these two methods, there are several other techniques being evaluated in the industry, such as vacuum-assisted underfill, for applications wherein the die is large or the gap between die and substrate is minimal. However, they are only in the research stage at this point.

The scope of this study is to evaluate the feasibility, reliability, and concerns in using underfills. Some of these underfill concerns can be categorized into material issues, process issues, and reliability issues.

Material issues: Material properties that need to be consistent from lot to lot include, viscosity, Tg, CTE, modulus, filler distribution, resin and filler loading levels, and filler size variation. Changes in these material properties can affect the flow properties and curing properties affecting the process and reliability of the product. Along with these are other important properties such as material aging at extreme temperatures.

Process issues: Voiding under the chip is a key process issue with capillary underfills. During the assembly process, underfill is dispensed on the side walls of the die, and capillary forces drive the underfill to the other side of the die to fill the area under the die. Due to the flow of underfill, if the flow front is not uniform, underfill could flow faster in some areas, thus capturing voids, termed as capture voids. Controlling these voids is essential for reliability because the presence of voiding could cause solder shorting during the subsequent reflow and surface mount process. Other process issues include dispensing issues, machine issues (e.g., dispense-pump clogging or machine temperature drift), thawing and storage life control, life in the processing machine (time and temperature), and limited ambient storage. Incorrect cure time, temperature, and moisture control can also result in voiding.

Reliability issues: Poor adhesion of underfill to the die and substrate could cause delamination or cracking. The modulus of underfill must be configured based on the dielectric being used in the die active area, which could be

2

There were concerns that the exposure of the underfill to the space environment would cause underfill degradation and ultimately lead to decreased package reliability. To address these concerns, NASA, under the NEPP program, has investigated the effect of low Earth orbit (LEO) environment and humidity on underfill properties. Prior to conducting the actual experiments, the potential risks of various constituents of the LEO environment were assessed. Since electronics within a spacecraft are exposed to less harsh conditions than outside of the spacecraft, the long-term vacuum exposure was rated as the most realistic environmental concern for the underfill material among all the negative constituents of the LEO environment. A raw underfill material used in an actual class-Y product was procured and exposed to long term vacuum, heat, oxygen plasma, and humidity. The underfill did not show any signs of degradation after the long term vacuum and heat exposure; instead, it showed signs of improvement. Conversely, humidity exposure resulted in decreased adhesive strength and lowered glass transition temperature of the underfill. The oxygen plasma exposure, conducted to simulate the exposure to the atomic oxygen environment, did not result in generation of any potential contaminants.

Since an underfill material exhibited property changes after the exposure to various environments, the impact of the underfill property change on the package reliability was of interest; NASA has collaborated with a part manufacturer and procured the manufacturer's research and development (R&D) samples to study this issue. The samples were underfilled daisy-chained flip-chip dies assembled on ceramic substrates. The samples were preconditioned and temperature cycled. The pre-conditioning conditions included vacuum thermal aging, humidity exposure, multiple reflow, and current stressing.

After temperature cycling, all the samples failed by an underfill breakdown mechanism, regardless of the preconditioning condition. A crack initiated at the longest fillet of the underfill and propagated to the flip chip solder bumps, causing the solder bump failure. This result was in agreement with the conventional wisdom among flip-chip engineers that flip-chip solder bumps generally do not fail before the underfill is compromised. After the current stressing, half of the flip-chip bumps suffered a minimum of 20% drop in the joint shear strength. However, the temperature cycling life of the current stressed samples did not exhibit changes, which indicates that underfill plays a far greater role than the flip chip solder joint strength in temperature cycling life of flip chip packages. The vacuum thermal aged and multiple reflowed samples exhibited 50% increase in temperature cycling life, while the humidity exposed samples showed a 30% decrease.

The strong correlation between the results of the two different studies, the study with the raw underfill material and the study with industry R&D samples, suggests that underfills' capability to withstand degradation by

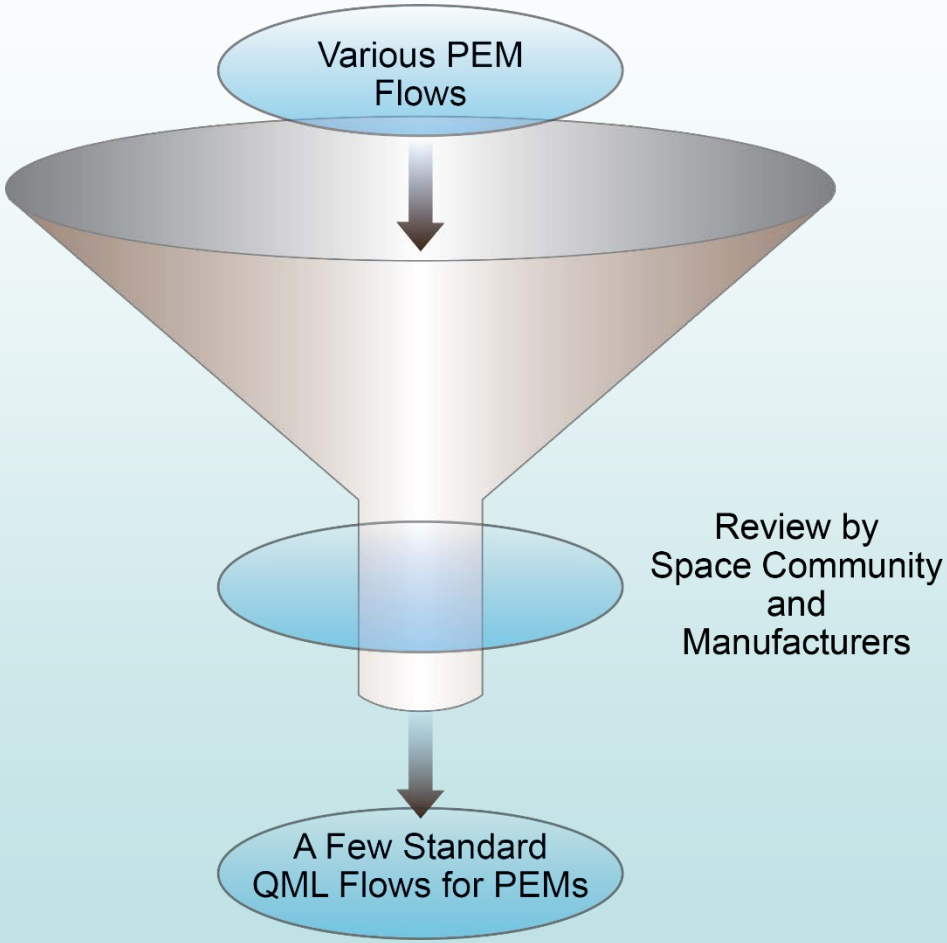
3

http://trs-new.jpl.nasa.gov/dspace/handle/2014/41402

NEPAG

G12 COTS (Commercial-Off-the-Shelf) Effort Standard PEMs (Plastic Encapsulated Microcircuits)

- **NASA Applications**
  - ❖ **Cubesats**
  - ❖ **Smallsats**



NEPAG

Signal Integrity Capacitors

- **New technology high-speed devices require signal integrity capacitors**
  - Commercial capacitors of base metal electrode (BME) construction were designed into the products
    - Tiny, low voltage
- **A task group comprised of the manufacturers and the users developed a screening specification**
- **Status**
  - The general specification MIL-PRF-32535 (formerly known as MIL-PRF-THIN) and a set of 10 slash sheets were released few months back. MIL-PRF-38535 will be updated to include the PRF-32535.
  - The slash sheets for the interdigitated capacitors (IDCs), used in Xilinx Virtex 5 FPGAs and other new devices, are being worked.

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New Issues

- **Electro Static Discharge (ESD)**
  - MIL-STD-883, Test Method 3015
    - Too old
      - Was written over 20 years ago
      - Long test times (could be up to 5-6 hours per unit)
    - Needs to be revisited for new technology
      - Smaller feature sizes, large number of pins, advancements in packaging (2D, 3D)
    - Compare with latest JEDEC test methods
  - MIL-PRF-38535
    - Clarify requirements
      - No specific ESD requirements for wafer foundries
  - NASA EEE Parts Bulletin
    - Special edition on ESD being worked

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A Changing Landscape (Shipping/Handling/ESD Challenge)

A New Trend – Supply Chain Management
Ensuring gap-free alignment for each qualified product
(All entities in the supply chain must be certified/approved)

Die design and fabrication	Company A
Fabrication	Company B
Wafer Bumping	Company C
Package design and package manufacturing	Company D
Assembly	Company E
Column attach and solderability	Company F
Screening, electrical and package tests	Company G
Radiation testing	Company H

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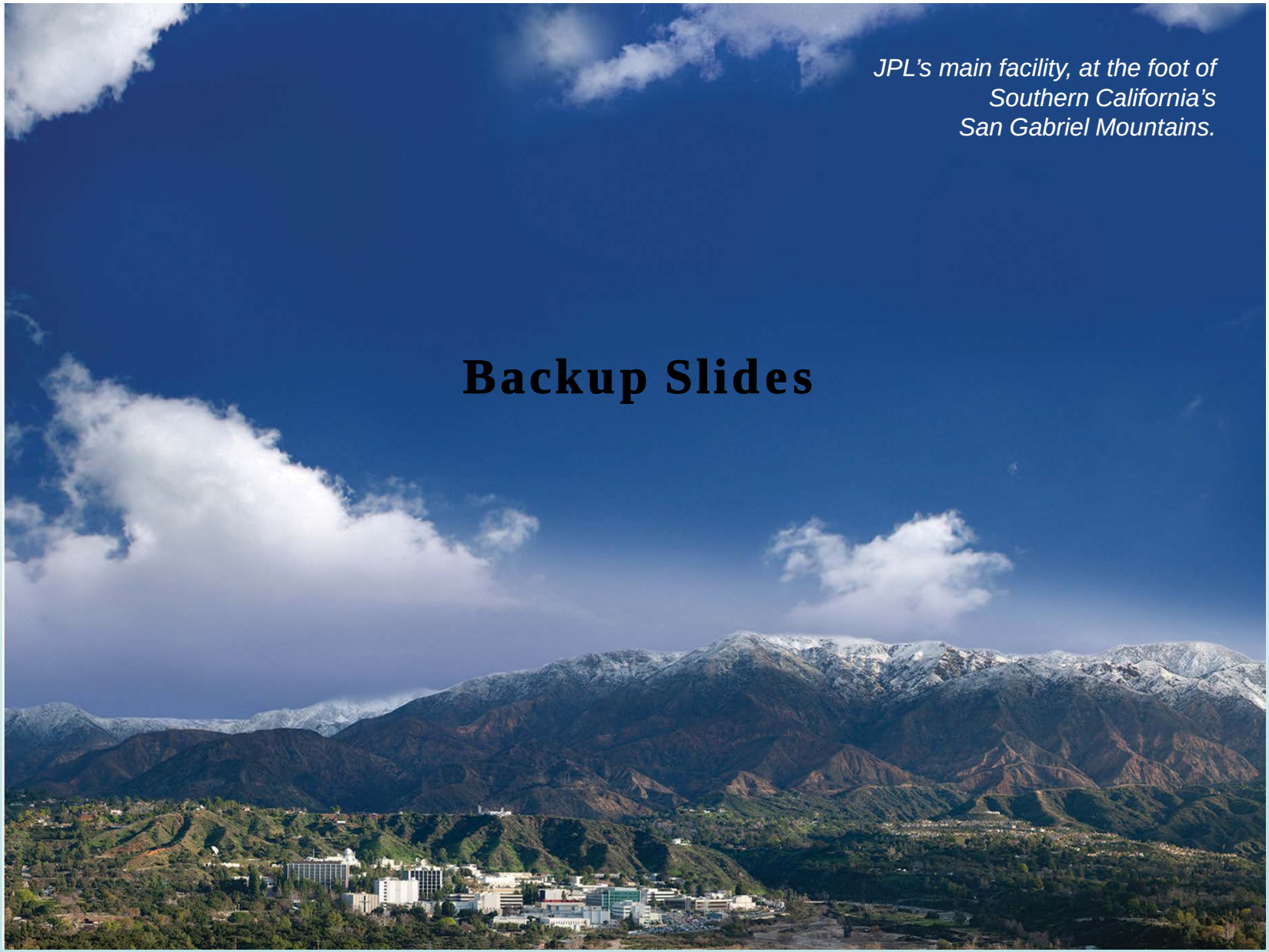
Other Major Activities

- Leak rate and residual gas analysis (RGA)
- New technology insertion (>2D packaging)
- GaN Working Group
- Hybrid element evaluation
- Passives
- Radiation hardness
- Plastic encapsulated microcircuit (PEM) screening and qual flows
- Copper bond wires qualification, testing

NEPAG

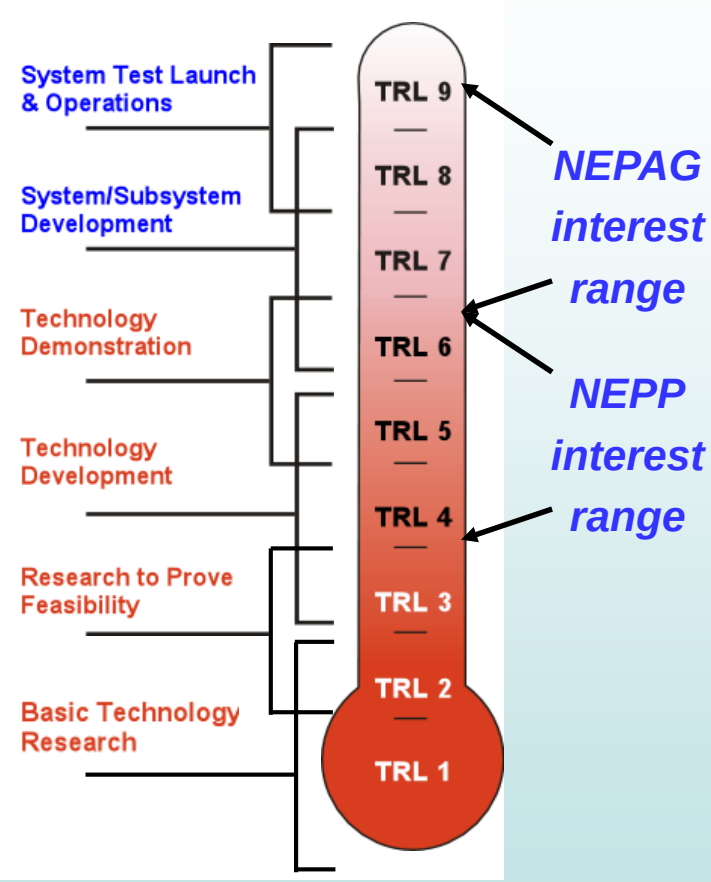


Backup Slides

NEPAG

NEPP/NEPAG Focus

- NEPP = NASA Electronic Parts and Packaging Program
- NEPAG = NASA Electronic Parts Assurance Group
- Funded by NASA Office of Safety and Mission Assurance (OSMA)
  - Through JPL 5X Assurance Technology Program Office (ATPO)



NASA Technology Readiness Levels (TRLs)

NEPAG

http://nepp.nasa.gov

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