

NISAR L-SAR Digital Electronics Subsystem

A Multichannel Distributed Processing System with Synchronous Timing Control for Digital Beam Forming and Multiple Echo Tracking

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Abstract— The NASA-ISRO Synthetic Aperture Radar (NISAR) L-band SAR instrument employs multiple digital channels to optimize resolution while keeping a large swath on a single pass. High-speed digitization with fine synchronization and digital beam forming are necessary in order to facilitate this new technique called SweepSAR. An architecture employing multiple FPGA based digital signal processors has been conceived to facilitate digital calibration on an individual channel basis as well as digital signal processing to optimize the receive signal. On-board processing and data compression has been implemented to reduce the volume of data in order to satisfy the operational requirements of near global coverage for the desired science targets. A novel command and timing architecture was developed to manage this complex system while providing detailed control of individual channel receive window timing required for digital beam forming. The NISAR L-band Digital Electronics Subsystem is the combination of the hardware, firmware and software components architected and implemented to operate this radar and return the desired quantity and quality of data for the science community.

Keywords—SweepSAR, Digital Beamforming, Distributed Processing, SCORE, PRF Dithering, Staggered SAR, HRWS SAR

I. INTRODUCTION

This paper is an update to a previously published paper at the 2016 Radar Conference [1]. The outline remains the same but the contents have been updated in various sections.

Software Defined Radios (SDRs) remain an attractive theoretical model to radar design. With advancements in ADC and digital signal processing technology, even the most advanced Synthetic Aperture Radars (SARs) are approaching this ideal receiver architecture. One key aspect of SDRs is direct sampling of the signal from the antenna without down-conversion to baseband [2]. For an L-band SAR, careful bandwidth and frequency selection and filtering can be used to allow direct digital down-conversion during the ADC sampling process [3]. Additional digital filtering is then employed to achieve temperature independent out-of-band rejection and suppression of aliased images. These techniques have been implemented in the design of the NASA-ISRO Synthetic Aperture Radar (NISAR) Digital Electronics Subsystem (DES) in the quad First Stage Processor (qFSP)

unit and their validation is a key element of the subsequent testing [4].

Another benefit of shifting much of the signal processing to the digital domain is the ability to digitize individual receive channels independently. Combined with a reflector antenna this enables the reception of multiple radar returns on different antenna patches simultaneously. It also allows the data to be digitally beam-formed to optimize the antenna and receiver response throughout the swath [4][5][6]. The NISAR DES utilizes three sets of qFSPs per polarization to implement twelve independent receive channels, which enables the instrument to have sufficient swath width to achieve global coverage on a 12-day cycle.

The NISAR L-band instrument is a side looking Synthetic Aperture Radar capable of supporting polarimetry, repeat pass interferometry, and split spectrum measurements in different modes to satisfy wide ranging scientific interests. Additionally, as a consequence of SweepSAR, it is necessary to employ a distributed radar timing control system with shared responsibility from the Control and Timing Board (CTB) and the qFSP. These factors led to the formulation of the NISAR L-band instrument command, control and timing architecture, details of which will be described in this paper.

The theoretical underpinning of SweepSAR [7], including SCan-On-REceive (SCORE) [8], digital beamforming, and PRF dithering (or alternatively called Staggered SAR [9]) techniques, have been described extensively. The mission concept for NISAR [10] as well as an airborne technology demonstration of a Ka-band analogy to the instrument concept [11] has also been presented previously. This paper will add to the existing literature by describing the actual hardware implementation designed to realize these concepts including practical problems encountered and the implemented solutions.

II. BLOCK DIAGRAM

The NISAR L-band radar instrument supports transmit and receive of Horizontal- and Vertical- polarizations with two copies of electronics to handle the digital signal processing for each polarization separately. Figure 1 shows the hardware associated with the H-polarization, a complementary set of hardware is also present for the V-polarization. Each polarization consists of 3 qFSPs, 1 Second Stage Processor

(SSP), and 1 Digital Signal Processing Power Conditioning Unit (DSPPCU). Two identical compact PCI chassis, each containing 1 RAD750 Single Board Computer (SBC), 1 Non-Volatile Memory (NVM) board, 1 Control and Timing Board (CTB), 1 House-Keeping Telemetry board (HKT), 2 Solid State Recorder InterFace boards (SIF), and 1 Discrete Output Board (DOB), make up the Prime and Redundant Radar Instrument Controller (RIC).

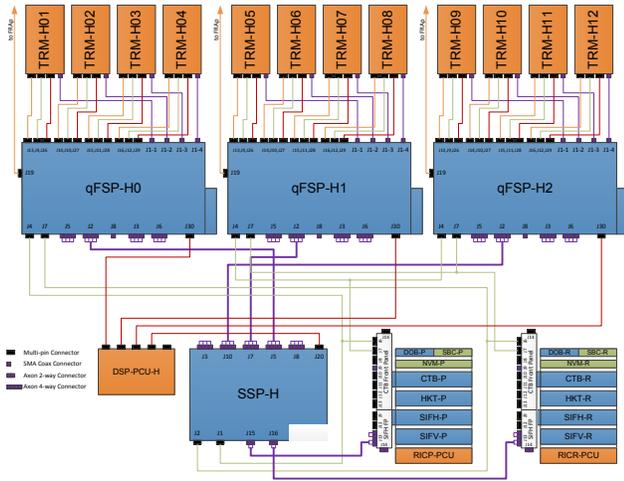


Figure 1 : Block Diagram of H-polarization components of NISAR Digital Electronics Subsystem

III. HARDWARE DESCRIPTIONS

A major function of the DES is on-board digital processing of the radar echo signal after digitization. Figure 2 shows the flow of the data through the DES.

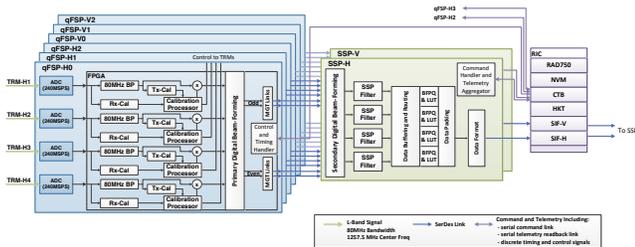


Figure 2 : DES Data Flow Block Diagram

The SweepSAR technique, while theoretically elegant, brings a host of practical complications in implementation. Primarily, the DES is required to track and process multiple echoes simultaneously. In the NISAR L-band instrument implementation, four simultaneous echoes are accommodated to support the maximum pulse repetition frequency (PRF) of 3100 Hz while maintaining 240 km swath coverage. Historically, radars process an individual echo within each pulse repetition interval (PRI), but the SweepSAR paradigm necessitates a shift to multi-threaded real time on-board processing.

Another consequence of the SweepSAR technique is the high data rates and resources required to accomplish multi-channel digitization, digital beamforming, and mode dependent filtering. The digital signal processing is

distributed in two stages to optimize resource utilization and minimize hardware complexity. The details of the signal processing at each stage will be described in the subsequent sections for the quad First Stage Processor and Second Stage Processor.

In order to facilitate proper beam formation, the DES has also implemented real-time closed loop calibration to allow channel-by-channel phase and amplitude correction to accommodate changes in individual transmitter and receiver responses due to variations from temperature and aging.

The collection of qFSP, SSP, SIF, and HKT are known as Down Stream Boards (DSBs).

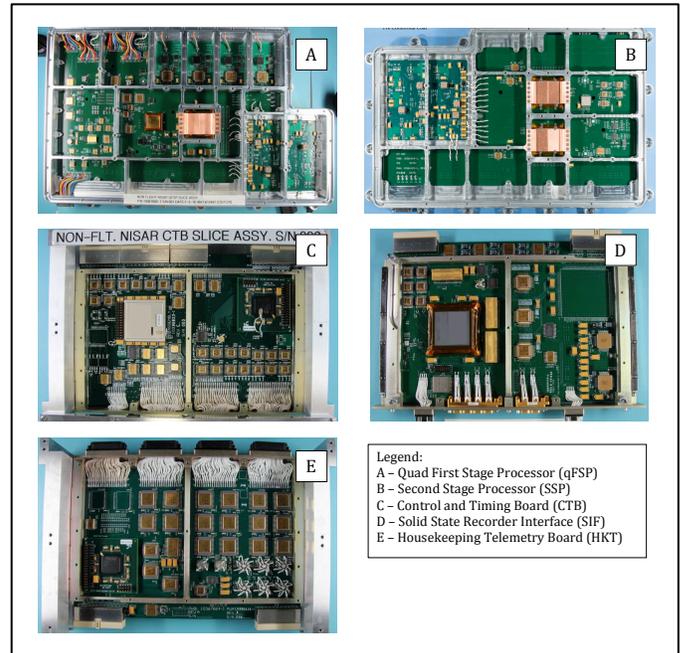


Figure 3 : Digital Electronics Subsystem Custom Developed Hardware

A. Quad First Stage Processor

The qFSP interfaces with 4 independent Transmit/Receive Modules (TRMs) to receive and digitize the RF signals from each TRM. The qFSP also calibrates each individual channel and provides the timing and control to the TRMs. After digitization the qFSP uses FIR filters [12] to digitally filter and decimate each channel and then scales the signals with a complex weighting coefficient and sums the contributing channels as part of the first step in onboard digital beam formation. Timing and synchronization are essential aspects of the operation of the qFSP and will be discussed in the context of the full instrument in a dedicated subsequent section.

In order to directly subsample the L-band received signal and still maintain sufficient signal-to-noise ratio to obtain close to 8 effective number of bits (ENOB), the sampling clock is required to have less than 400fs of random jitter. This was achieved by distributing the sample clock directly from the high fidelity frequency synthesizer (~100 fs rms jitter) to the qFSPs with an RF distribution network. Within the qFSP, a balun transformer is used to convert the single ended analog

clock to a differential signal to minimize the effect of noise. Clock distribution on the qFSP is kept to a minimum number of ICs to minimize the added random jitter. The system clock distribution including the data conversion implementation was tested in our system configuration with the results shown in Figure 4.

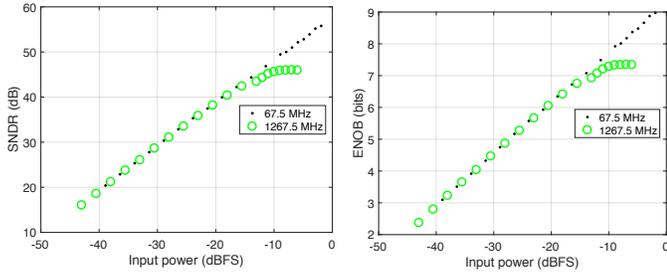


Figure 4 : SNDR and ENOB at baseband and L-band

B. Second Stage Processor

The SSP receives the partially beam formed radar return data and performs the final step of digital beam forming as well as the mode dependent filtering to support the different bandwidth and center frequencies within the 85MHz NTIA L-Band frequency allocation for active Earth remote sensing. The SSP also provides the secondary function of compressing the final processed data using Compact Block Floating Point Quantization (BFPQ) compression to reduce overall data volume for storage and downlink.

C. Control and Timing Board

The primary function of the CTB is to keep a stable time base and generate timing signals for the system to enable deterministic and synchronous system operations. The CTB is also the distributor of configuration information from the SBC to all the units within the DES. It also serves as the command and telemetry interfaces to the rest of the flight system.

D. Solid State Recorder Interface Board

The SIF receives the processed BFPQ blocks from the SSP and sorts and formats the data to allow range lines to be output contiguously as a single composite range line for each pulse. The SIF also adds timing and other telemetry information to each block of range line data to facilitate ground processing.

E. House-Keeping and Telemetry Board

The HKT collects temperature and voltage telemetry data from the entire radar instrument and reports the information on a one second basis to be stored as engineering telemetry data for instrument health and fault monitoring.

F. Single Board Computer

The SBC is a 3U cPCI RAD750 processor board that operates to sequence commands and generate orbital dependent parameters to update the system throughout datatake and observation collections.

IV. TIMING AND SYNCHRONIZATION

The Radar system has been segregated into 3 timing resolution zones in order to make the command and control achievable. The SBC operates in the most coarse resolution

zone and is required to respond on the order of milliseconds to seconds. The CTB operates in the mid-resolution zone and is capable of commanding and coordinating control of the instrument down to the 100ns timescale. The qFSPs are responsible for fine sampling control capable of resolution on the order of single ADC sample periods. Dependencies between the timing zones are kept to a minimum to simplify the implementation while maintaining synchronization.

In order to maintain a constant time base throughout the mission, the CTB will keep a continuous count of clock cycles generated by the instrument's 10MHz Stable Local Oscillator (StaLO). This counter is called the L-SAR Radar CLock (LRCLK) and will nominally be reset once at the beginning of the mission and will allow the radar to time-tag all critical timing events with an absolute resolution of 100ns. In order to relate the LRCLK to an absolute time reference, the radar will receive a 1PPS signal from the on-board GPS. Each time a 1PPS signal is received, the CTB will record the current LRCLK value and the associated GPS time from the GPS receiver as shown in Figure 5. Both the GPS and LRCLK time pair for the 1PPS event are then reported in the Detailed Radar Telemetry (DRT) at a 1 Hz rate to enable correlation of the two time references on the ground.

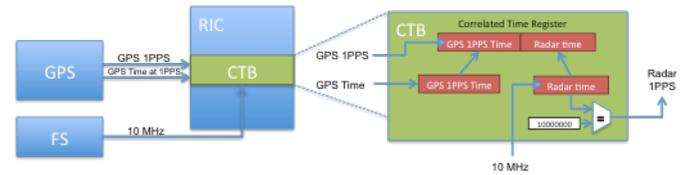


Figure 5 : Correlation of Radar Time to GPS Time

In the event of faults that interrupt the LRCLK the CTB can be directed to offset the LRCLK value by a commanded amount after nominal operations are restored. During operations, sequence commands such as datatake start, FPGA reprogram, and sequence-select are executed at the specified LRCLK time. Within a datatake, update commands are executed at the specified pulse count.

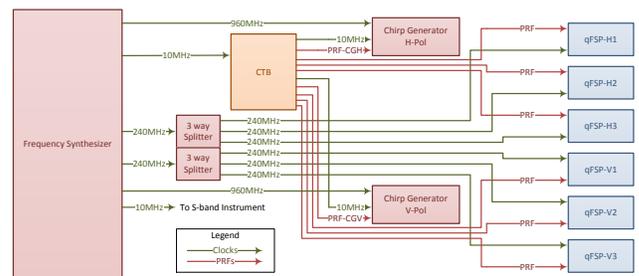


Figure 6 : PRF and Clock Distribution

In order to ensure proper beam formation during onboard digital beam forming, all channels on all qFSPs need to be synchronized. During datatake operations the master timing signal is the PRF signal, which precedes the transmit event of that pulse. All qFSP units will receive an identical time synchronized PRF signal aligned to within one ADC sampling interval. The ADC sampling clocks (240 MHz) are all phase locked to the 10MHz StaLO and distributed with phase-

matched cables. Figure 6 shows the distribution of timing signals to accomplish this synchronization. This allows channel-to-channel sample time alignment to within one ADC sampling clock period across all 12 channels per polarization. The sub-sample mismatches are adjusted digitally and have been shown to be acceptable in digital beamforming.

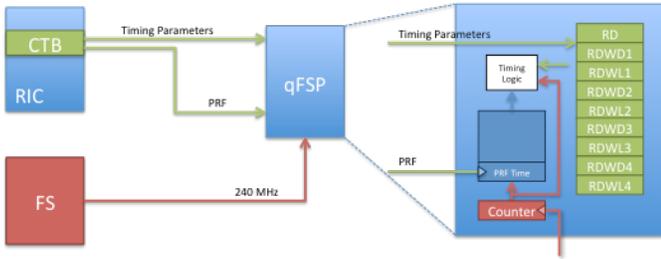


Figure 7 : Channel Receive Window Timing

Within the qFSP, the time gating is controlled by parameters that determine offsets with respect to the PRF signal as shown in Figure 7. The qFSP stores the PRF time of each PRF event based on the 240MHz clock and has a FIFO memory and separate counters to keep track of the receive window times for each pulse in the air. Since the receive window is tied directly to the transmit event that produced it, this scheme accommodates PRF dithering without any complication. The Range Delay (RD) parameter specifies the round trip time of the signal and the Range Data Window Delay (RDWD) and Range Data Window Length (RDWL) parameters specifies the specific timing of each ADC channel receive window. The timing relationship of the receive windows with respect to the supplied parameters are shown in Figure 8. The SCORE concept is accomplished by supplying the proper set of timing parameters to track the receive echo across the channels. Due to earth oblateness these timing parameters will need to be updated regularly as the instrument orbits the earth. Nominally, update commands are used to modify time gating parameters during observations at 10-second intervals.

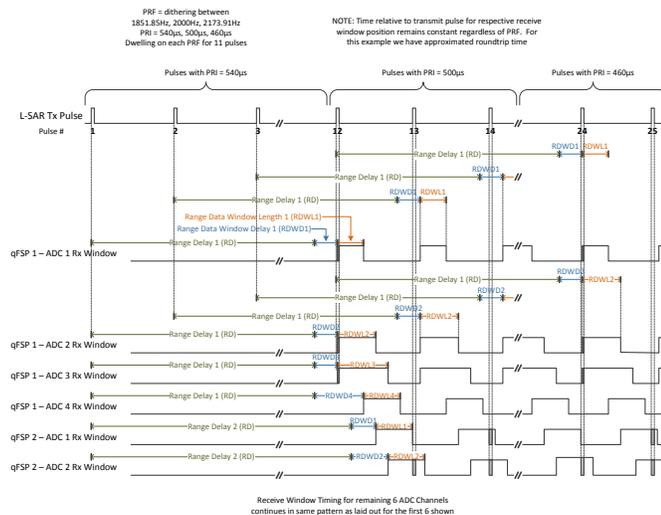


Figure 8 : Simplified Example of Receive Window Timings

V. COMMAND AND CONTROL

Commanding of the radar is based on an observation sequence schedule that is uploaded from the ground to the instrument flight software. The instrument flight software stores a radar configuration table in the non-volatile memory (NVM), which identifies all of the hardware parameters associated with the allowable modes of operation. The observation sequence will identify the entry in the radar configuration table associated with the desired mode for the observation and the start time and duration of the observation. Figure 9 shows the flow of the commanding from ground to the hardware.

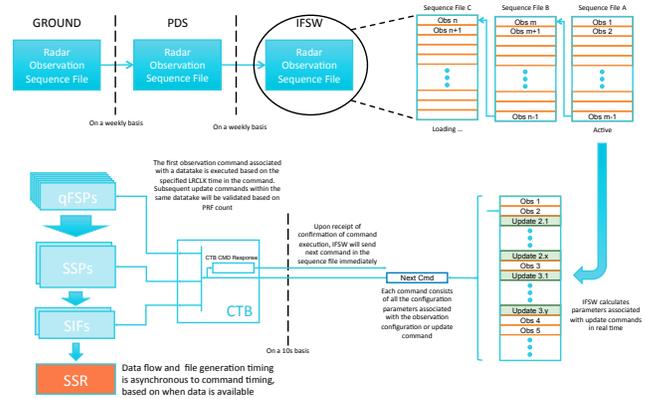


Figure 9 : Command Upload and Sequencing

Flight software calculates parameters to adjust receive window timing and issues update commands to the DES hardware within observations on a regular schedule. The commanding scheme from the flight software to the rest of the radar electronics is based on a start time, indicated in Radar Time (LRCLK), and update time, indicated in PRF counts. This scheme enables the radar to be very agile to mode changes accommodating seamless mode transitions without missing any pulses.

Commands need to be communicated to the distributed processing elements with sufficient information to direct synchronous radar timing operation as well as parameter updating in a deterministic and coordinated fashion. The following sections will describe the commanding protocol that was developed and implemented to accomplish this in our system.

A. Command and Telemetry Protocol

Commands for the DSBs have a defined packet structure known as containers. Containers are a collection of packets that includes header, PRF count, commands, and footer. Containers are used to transfer parameter updates to the DSBs.



Figure 10 : Container packet order

Figure 10 shows the order of the packets transmitted in each container. There is a PRF count associated with each container because the commands within each container will all need to be executed synchronously across the subsystem

VII. SUMMARY

The NISAR DES is a realized hardware implementation of a high resolution, wide swath (HRWS) SAR system utilizing an array-fed reflector antenna system employing the SweepSAR technique. This paper has described the complex system employing novel designs in hardware, firmware, and software to meet the performance and capability requirements of the NISAR project. The result is a highly capable system that digitally beam forms an array of 12 individual receive channels per polarization, supports mode dependent bandwidth processing, and provides deterministic timing control to coordinate the many simultaneous activities while capturing swaths greater than 240km.

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