

**Jet Propulsion Laboratory**  
California Institute of Technology

## **Trends in Radiation Performance of Modern Microprocessors and Microcontrollers**

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### **Acknowledgment:**

This work was sponsored by:

The NASA Electronic Parts and Packaging Program (NEPP)



- **Microcontrollers and Microprocessors**
- **Some Radiation Effects Data**
- **Can we be smarter?**
- **Technology impact – SRAMs and Logic**
- **Some Trends**

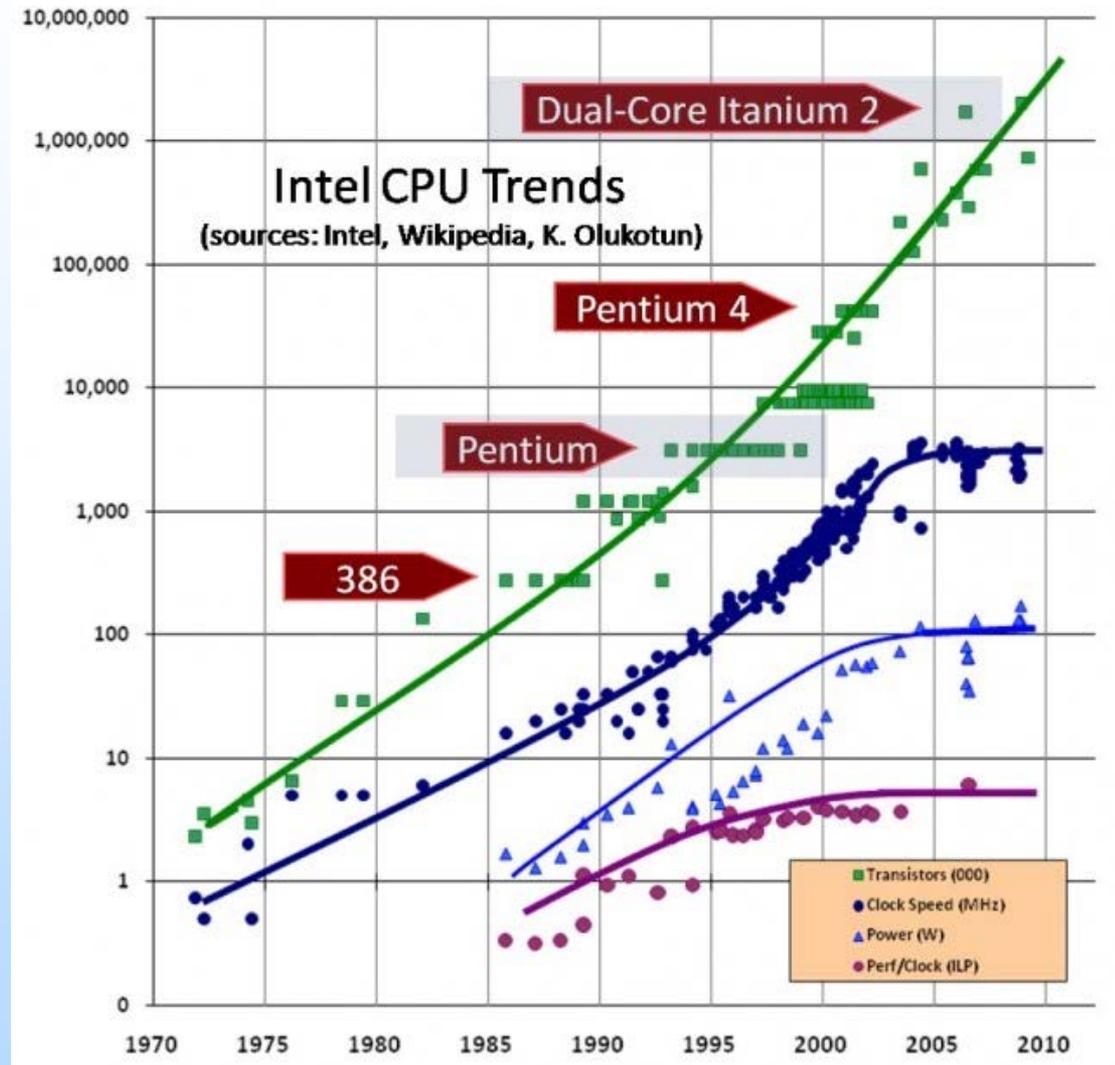
**Our goal is to explore test methods and efforts to try to extract trends that can be exploited to improve radiation testing of these devices.**



- **Microprocessors are**
  - The central processing unit (CPU) of a computer
  - Part of a system with RAM, ROM, and other peripherals
  - Intended for general operations that may not be defined at time of build – open-ended
- **Microcontrollers are**
  - More varied in internal technologies than processors
  - Usually used in embedded systems
  - Contain most of the circuitry necessary to implement a computer – may be called mini-computers
  - Have RAM and ROM on-board, along with peripherals
  - Usually provide well-defined application functionality
- **Both get referred to SOCs – story for another time...**
  - The names are sometimes used interchangeably...

# Commercial Trends

- Clarify what we're talking about
  - Shrinking features
  - Increasing complexity
- Recently, microprocessors are getting more complex, not faster, not higher power
- Microcontrollers are a little different because they mix multiple technologies



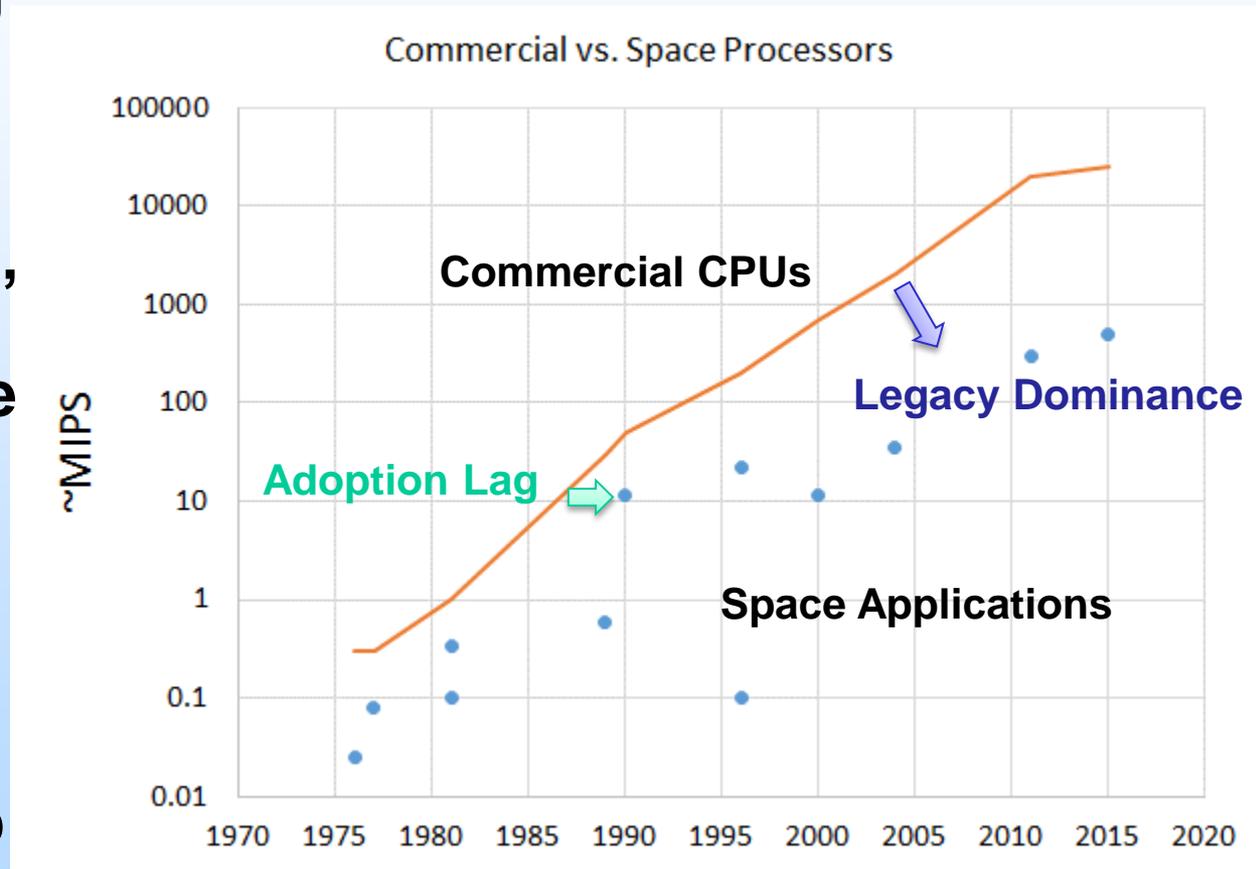
Hruska, 2012, *The death of CPU scaling: From one core to many — and why we're still stuck*, <http://www.extremetech.com/>

# Microcontrollers and Microprocessors in Space



- **Performance**
  - Latest flattening due to focus on efficiency...
- **Until about 2000, space processors were “close” to commercial devices.**
- **BAE’s RAD5500 series will bump up a bit.**

## Deployed devices in space missions



–Information adapted from [www.cpushack.com](http://www.cpushack.com)

# 1997 - Pathfinder



- **The Pathfinder mission is a microcontroller / microprocessor hybrid application**
- **Rover device used was 80C51**
  - RAM, ROM, IO, and other features
  - (Microcontroller)
- **The 80C51 would send data to the RAD6000 computer on the pathfinder base.**

(Device usage per Lloyd Keith:  
[http://quest.arc.nasa.gov/mars/ask/about-mars-path/pathfinder\\_computer.txt](http://quest.arc.nasa.gov/mars/ask/about-mars-path/pathfinder_computer.txt))

  - Rover was like an embedded system
  - Base provided general computing
- **The key here is that modern space missions commonly consist of microprocessors and microcontrollers at various performance points, as needed.**





- **Many different devices may be used today:**
  - **Microcontrollers for stand-alone instruments, wheel controllers, etc.**
  - **Low-to-Mid range microprocessors to enable high reliability operations at low power**
  - **High performance processors to handle large amounts of data.**
- **Architectures are exploding on us**
  - **ARM has moved the Microprocessor and Microcontroller markets significantly**
  - **There is still need to understand earlier architectures – Sparc, Intel, PowerPC, etc.**
  - **Every architecture is growing with multiple functions on the chip, and the number of cores is increasing...**
  - **And some of these are working into Rad Hard devices**



## For microprocessors and microcontrollers:

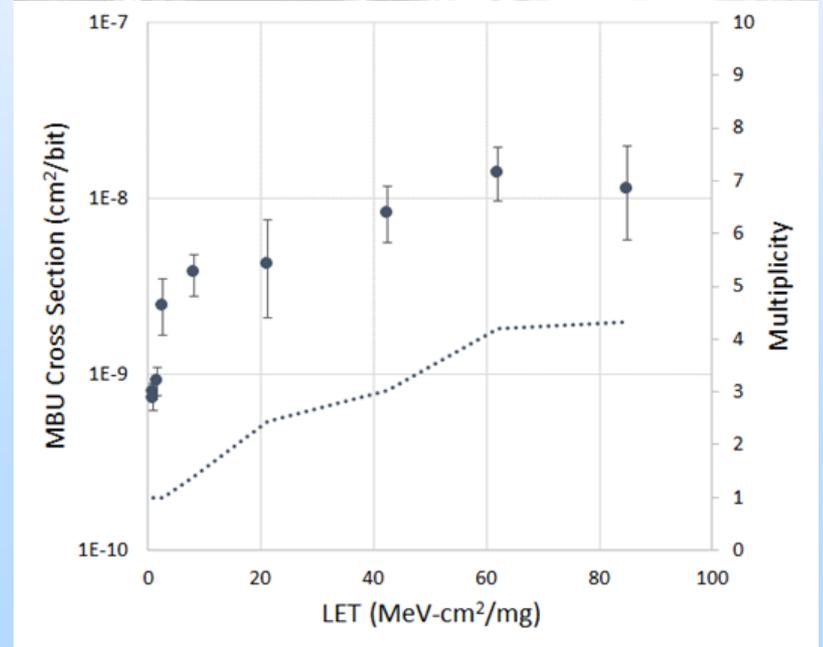
- **Total Ionizing Dose (TID) can cause:**
  - Slower switching – eventually unreliable and won't "boot"
  - Data loss – on-chip ROM degradation
  - Reduced drive current at outputs
  - Slower I/O
- **Single Event Effects (SEE)**
  - CMOS devices may show single event latchup (SEL)
  - For devices with on-chip power handling, gate rupture or burnout (SEGR or SEB) may be a risk
  - But mostly, these devices are affected by single event upsets and transients (SEU) and (SET) that can cause incorrect operations or bit flips
    - These lead to incorrect operation, sometimes called single event functional interrupt (SEFI)

# Rad Data Example

## Atmel AT91SAM9G20



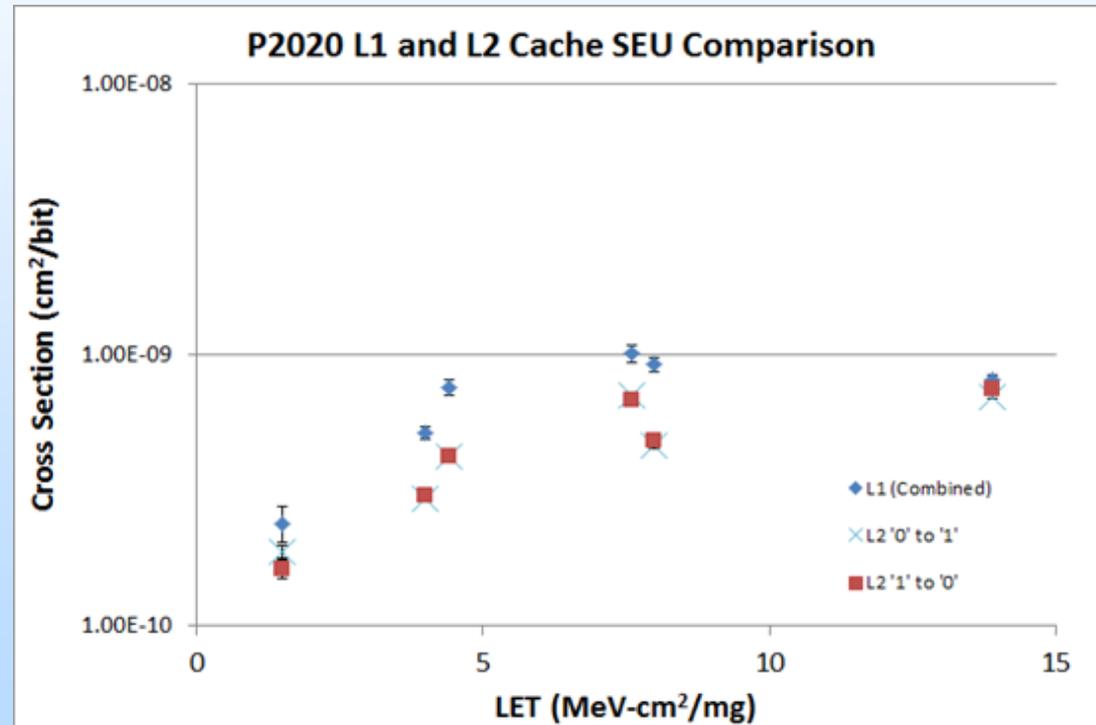
- **Heavy ion tests of AT91SAM9G20**
  - 90 nm “microprocessor” typically used as a “microcontroller”
- **Target was the On-chip-memory (OCM)**
  - Per last slide – OCM bits similar to leading cause of device errors.
  - (This is most likely to cause errors during execution – and bits are expected to be similar to CPU registers and caches)
- **Same data obtained using hardware debugging, and in-situ test code.**



# Another Example: Freescale P2020



- **P2020 Processor is a Freescale 45 nm dual e500 core microprocessor with many built-in features**
- **L1 and L2 caches are the most sensitive structures on the device.**
- **Unless L1 is operated in “write-through”, L1 bit upsets will cause threads to crash...**
  - **Usually ~50% or more such threads will kill the operating system.**





- Hardware setup**

	Processors					Controllers				
	Designing	Cost	Coverage	Swap DUT	In-Situ	Designing	Cost	Coverage	Swap DUT	In-Situ
Custom Test Board	Complex	\$\$\$\$	Complete	Yes	Good	Easy	\$\$	Complete	Yes	Good
Evaluation Board	N/A	\$\$	Partial	No	Good	N/A	\$	Partial	Maybe	Good
Computer	N/A	\$\$-\$\$\$	Partial	Maybe	Varies	N/A	N/A	N/A	N/A	N/A
3rd Party Remote	N/A	\$\$-\$\$\$	Complete	Yes	Poor	N/A	\$\$	Complete	Yes	Poor

- Some Notes:**

- For SEE testing, In-Situ operation is required
- Often the cost of an evaluation board is lower than the cost of preparing a DUT for testing
- 3<sup>rd</sup> Party Remote testing is only viable for TID or post-SEE device reliability testing



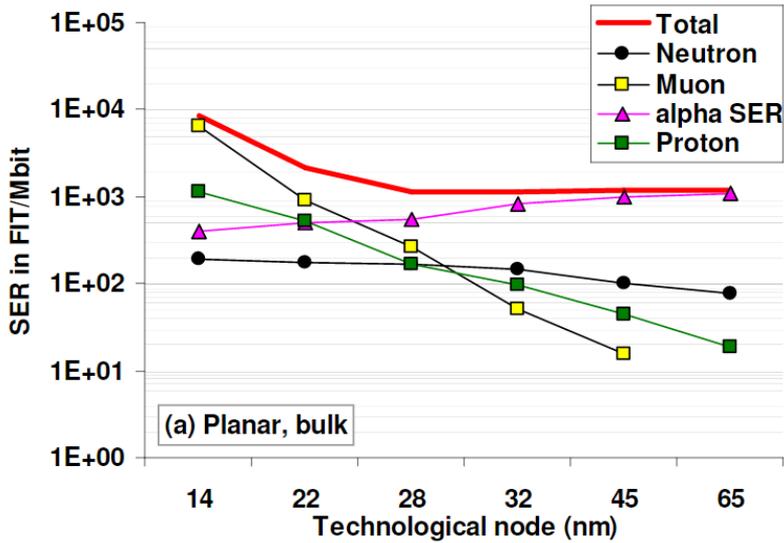
- **TID may be better suited by building static-bias fixtures and sending devices to 3<sup>rd</sup> party testing**
- **However, based on the previous table:**
  - Reduction in custom-built systems for both type of devices
  - Increased reliance on evaluation boards
  - A great example is the P2020RDB - the board is \$700, but buying P2020 parts individually is \$200
  - This trend is likely to continue - but...

# Eval Board Issues...

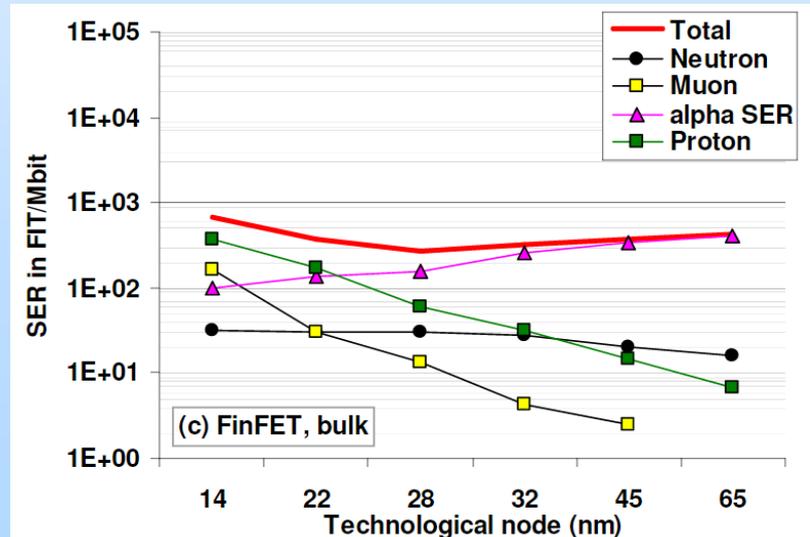
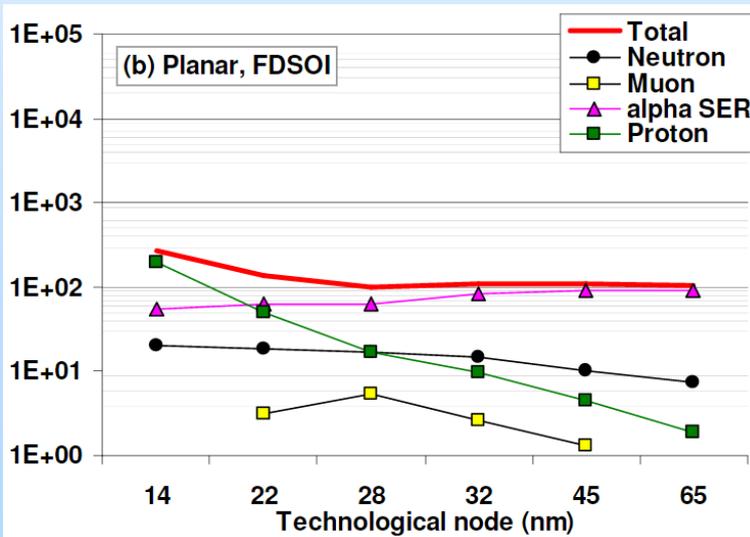
- We are finding some significant problems with some test boards, in terms of preparation for test...
- Package on package may become a significant problem...  
(May only apply to microprocessors)



# SRAM Scaling



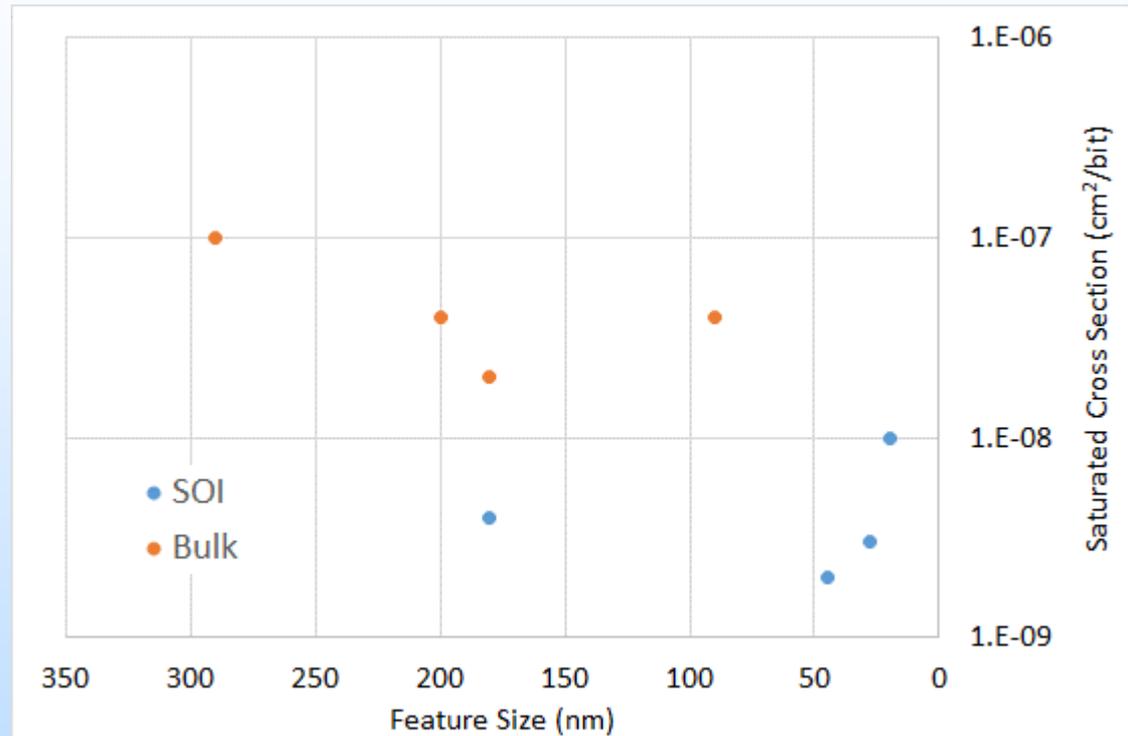
- This is great data, but it is FIT/MB, which doesn't correlate directly to space data...
- Proton and Muon sensitivity are becoming more important at smaller sizes – primarily due to reduced critical charge and sensitivity to direct ionization from particles with a charge of  $\pm 1$ .
- All technologies show flat trend down to 28nm, but perhaps sensitivity is actually increasing below that.
  - Space community worried about a possible increase since around 65nm – is it coming?



# Rad Effects Data Feature Size



- **Comparison of available data - several reports.**
  - Including both microprocessors and microcontrollers
  - Heavy ion saturated cross section
- **No clear trend is evident in saturated cross section as a function of feature size.**
- **Same type of problems as with earlier SER discussion.**

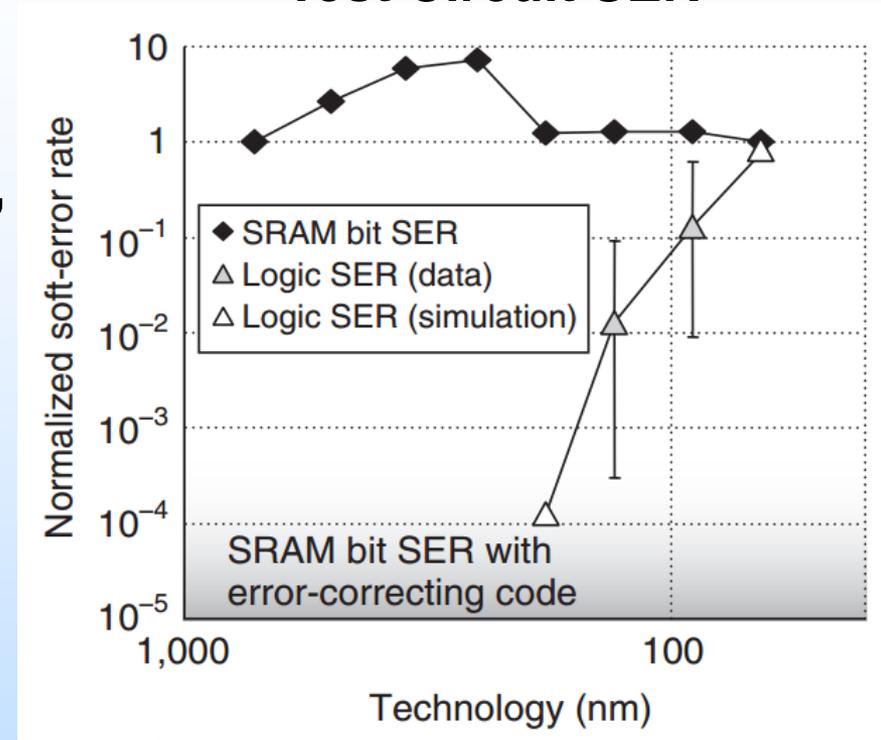




# Logic Sensitivity...

- 10-15 years ago logic sensitivity started to be a significant source of SER
- However, for a running circuit, logic masking is very important
  - E.g. processors (in both types of devices) are general-purpose, and on each clock cycle executes a few out of 100s-1000s of possible instructions
  - During execution of a set of instructions, the logic for unused instructions is masked.
- Testing for this requires operating the device...
  - Amount of logic and logic masking depends on device type and peripherals.

Test Circuit SER



Baumann, Texas Instruments  
(IEEE Design and Test of Computers, May/June 2005)

Realistically, it is difficult to know the highest possible logic utilization. Thus it is important to think of possible system use when designing a test.

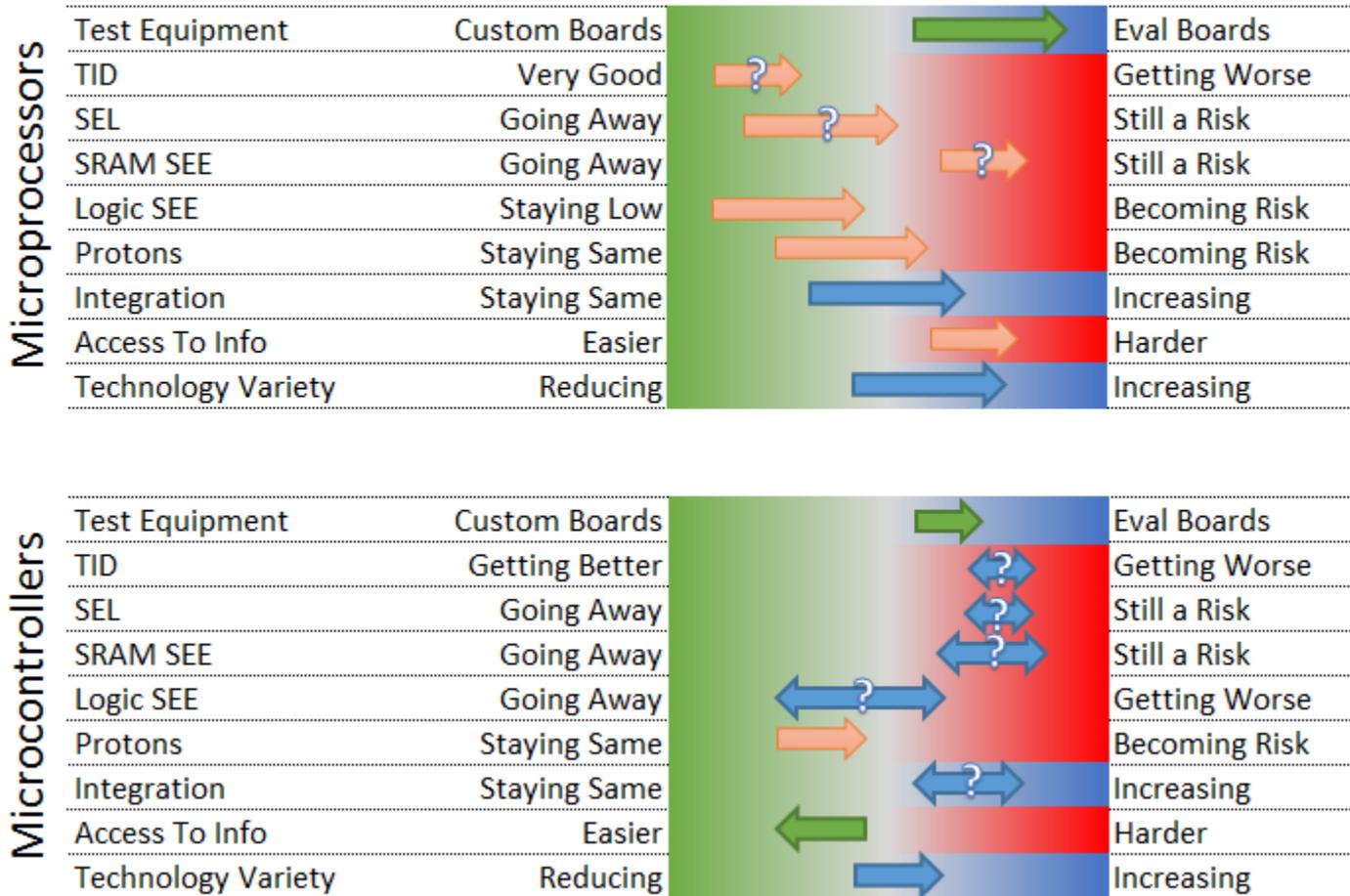


- **Generally, scaling is very good to TID performance but...**
- **Microprocessors**
  - **Sitting in the Mrad(Si) range now – this is a high bar...**
  - **But integration of multiple component types, including on-chip regulation and higher-voltage IOs, bipolar circuits, etc., threaten this TID performance**
- **Microcontrollers**
  - **These are currently somewhat TID limited already (at least commercially) – 10-20krad(Si) is common**
  - **There are multiple technologies in these devices, including bipolar, charge pumps, etc.**
  - **There is no reason to think that these devices will gain benefit from scaling of some portions when others will not scale and may remain the same or get worse.**



# Trends Going Forward

## General Trends for Microcontrollers and Microprocessors



**Differences here are primarily due to the mix of sub components in each device type. Also, microcontroller processors tend to be older technology.**

# Conclusions



- **The main thing is: is my mission going to do something incorrectly because of my microprocessor or controller?**
  - TID and SEL must be considered unless a compelling technology reason is known
  - The general approach of bounding the problem has traditionally been performed by studying memory cells
- **Memory cell scaling appears to be impacting SER in a way that will start impacting commercial devices.**
- **Due to increasing complexity and integration...**
  - It is necessary to functionally operate devices to determine possible logic sensitivity increase
  - Test boards and hardware efforts continue to evolve
- **Thus far there is no clear indication of scaling impact or trends moving forward. However, this work has informed future work, which will:**
  - Extend test methods to newer devices and architectures
  - And explore possible scaling issues related to memory cells and logic sensitivity