Jet Propulsion Laboratory
California Institute of Technology

NASA NEPP Program Memory Technology – Testing, Analysis and Roadmap

D.J. Sheldon, Assurance Technology Program Office (ATPO)

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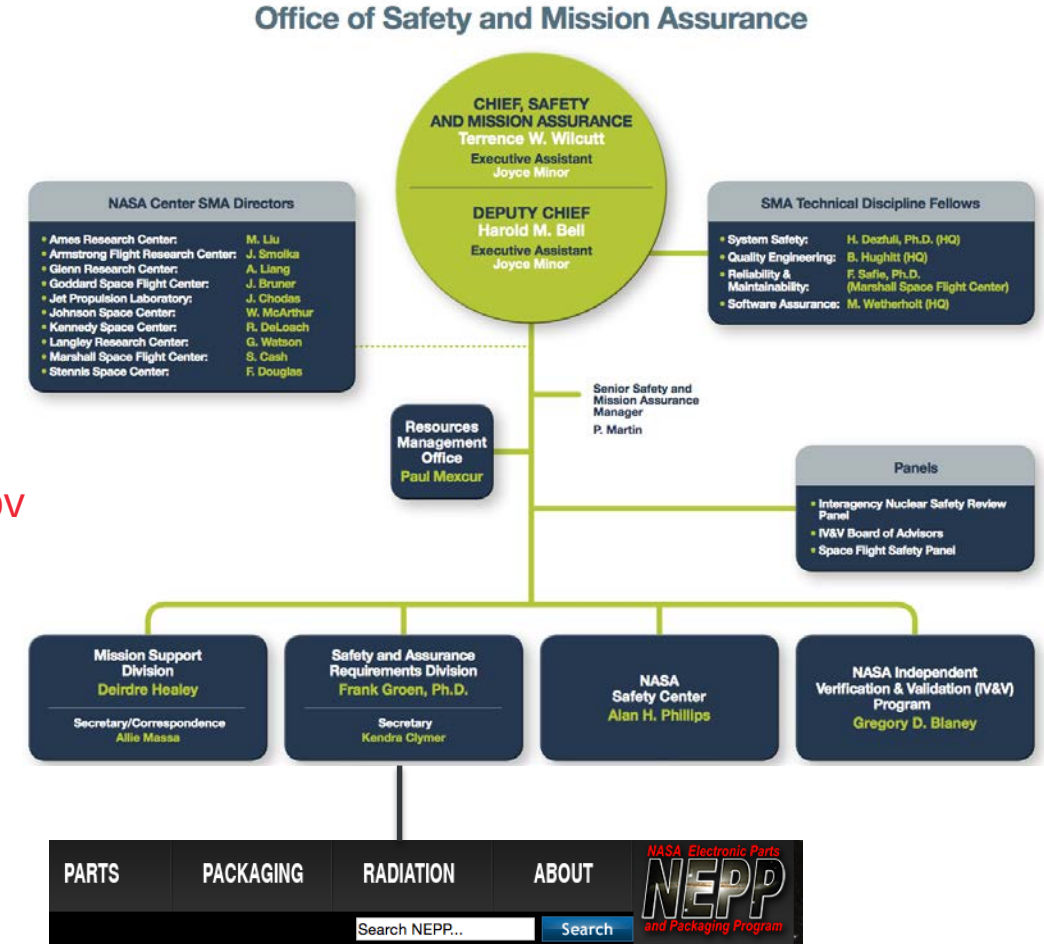
Overview

- Present recent examples of NEPP program sponsored memory IC activities
  - Reliability analysis
  - Radiation analysis
  - Technology review
  - Document/guideline generation
- Provide roadmaps for technology understanding and future activities
  - Complexity issues – convolution of a variety of failure mechanisms
  - Practical experimental concerns
  - Fault identification

Organization Chart

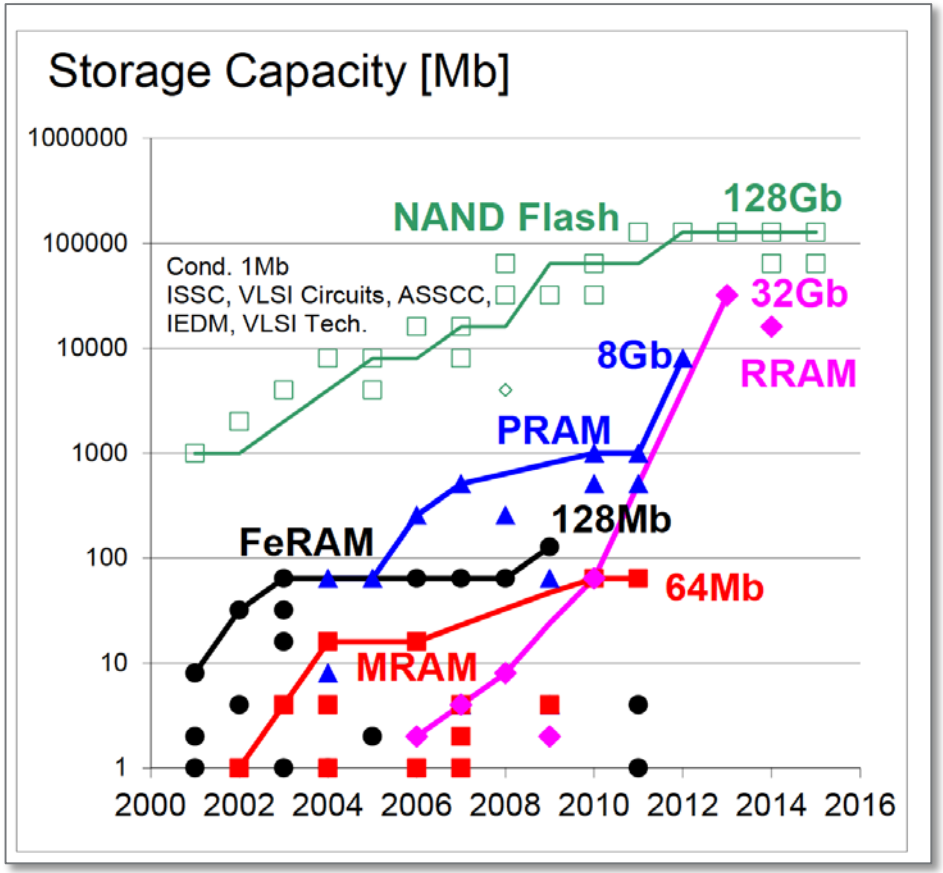
https://sma.nasa.gov



Memory Technology Covered by NEPP Program

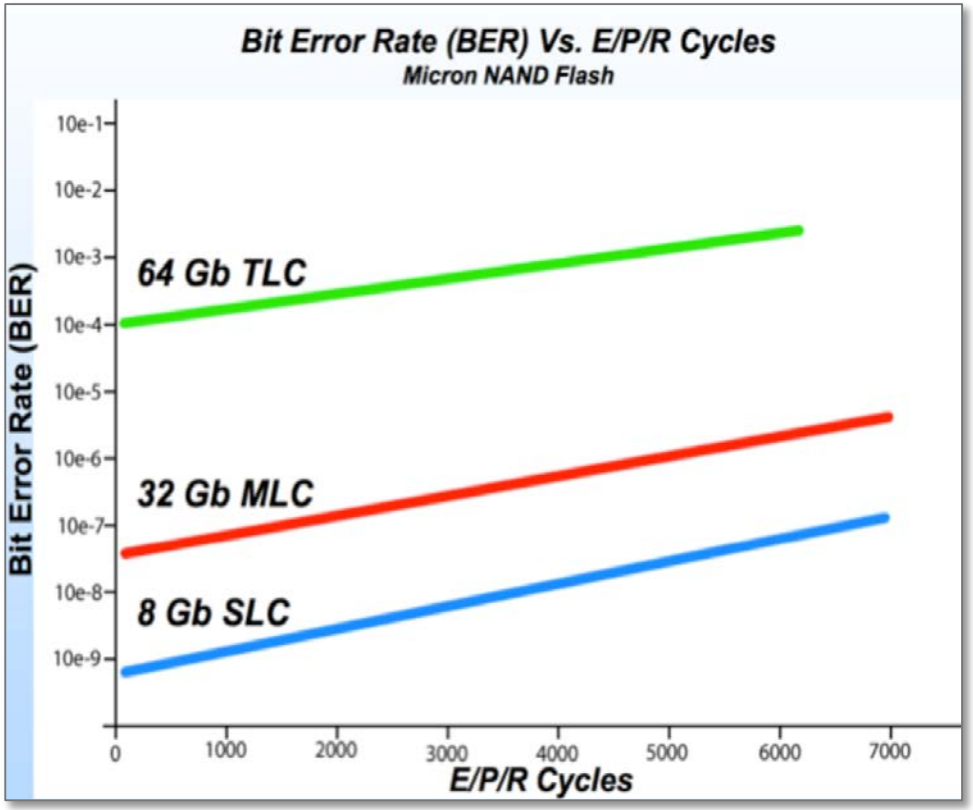
- Commercial technology (COTS) focused
  - Rad hard space qualified memory technology essentially is focused on mid density SRAMs (4-64Mb level)
  - Well documented and researched
- Volatile and Non-volatile
  - DRAM and the progression to SDRAM, DDR2, DDR3, etc…
  - Flash
    - NAND predominately
  - Alternative NV technologies
    - Anything but floating gate
- Mostly individual memory devices but…
  - Things are changing quickly
  - Embedded memory with processor
  - High density memory as part of large sub system

ISSCC 2015 Non-Volatile Memory Roadmap



- The dominance of NAND Flash
  - Floating gate based devices
  - Single level cell (SLC) devices in the 1990's
  - 2 bits per cell (MLC) appear early 2000's
  - Triple Level cell (TLC) appear 2008
- Unique charge storage mechanisms
  - FeRAM and MRAM
  - Scaling is very difficult
- Resistive based technologies
  - Scaling concerns minimized
  - Yield is main limiter
- Any non-floating gate based memory cell is by definition rad hard
  - The underlying CMOS, maybe…
- NEPP has tested all these types of non-volatile memory

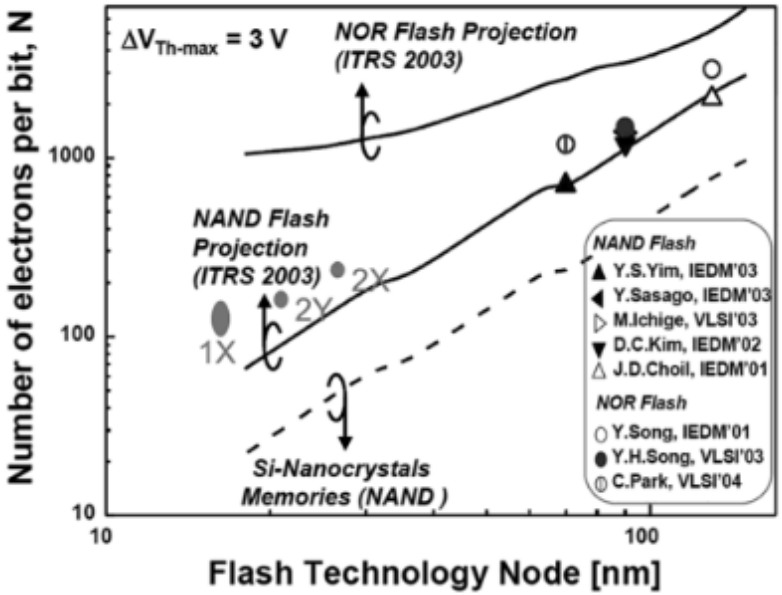
Bit Error Rates for NAND Flash

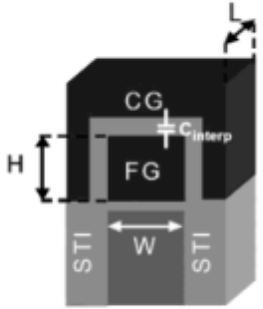


J. Heidecker "NAND Flash Qualification Guidelines"
NEPP ETW 2012

- NAND Flash has two types of reliability degradation concerns
  - Cycling
  - Data Retention (Storage)
- Tunnel oxide thickness DOES NOT scale as pass transistor gate length shrinks
  - Must remain constant (6-7 nm)
  - Prevent B-B tunneling and TDDB oxide breakdown
- Multiple bits per cell = different #'s of electrons stored
  - Changes read current
- Scaling area of cell shrinks number of electrons
  - <50 electrons for 25nm cell for 100mV shift
- Increasing program/erase:
  - Nearest neighbor interactions
  - Defect generation increased sensitivity

Number of Electrons per bit NAND Flash





$$\Delta V_{th\text{-}max} = N.q / C_{interp}$$

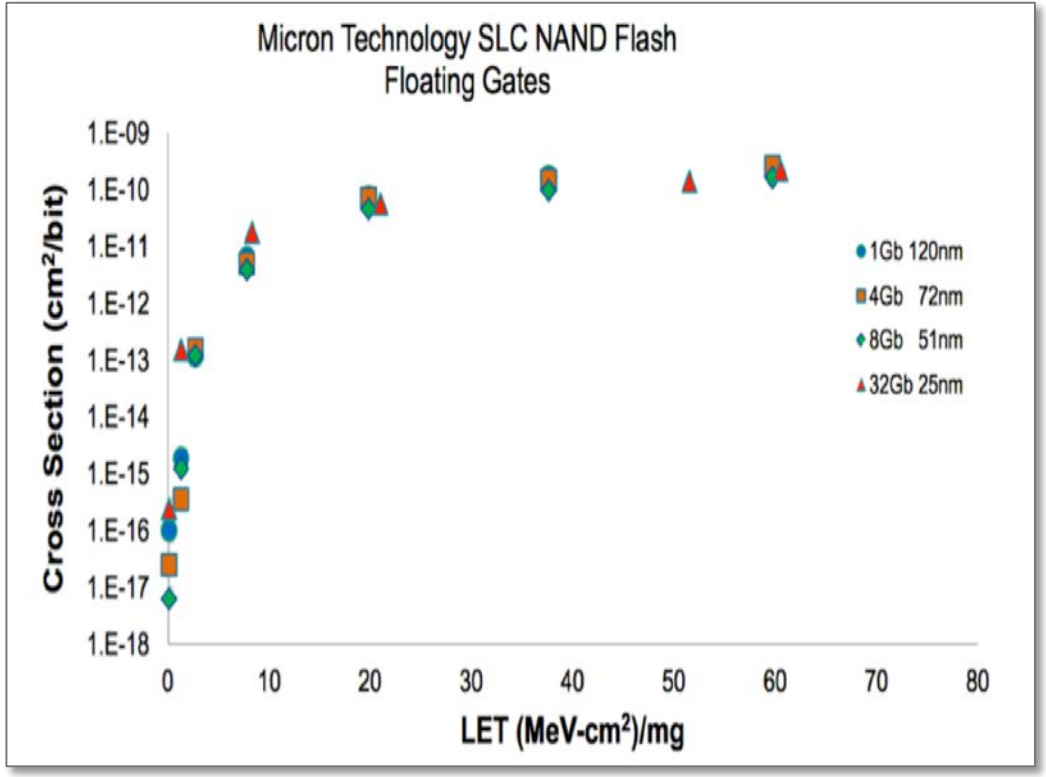
$$C_{interp} = \frac{\varepsilon_{ox} \cdot S_{interp}}{EOT_{interp}}$$

$$S_{interp} \sim W.L + 2.H.L$$

- Hundreds of electrons to represent per bit data values => great risk to upset in space environment and degradation due to total ionizing dose conditions

"NAND Flash Memory Technology" S. Aritome 2015

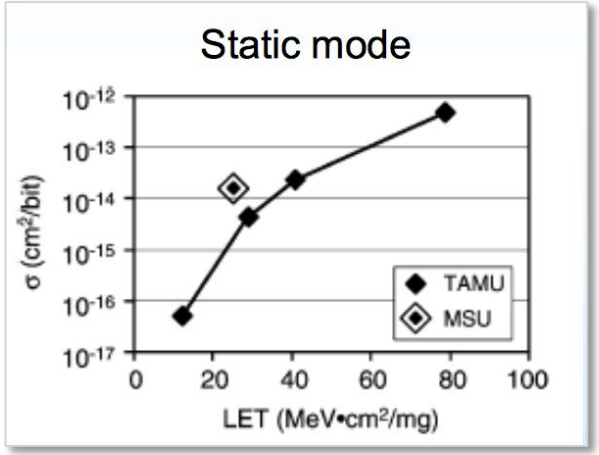
SEE Testing SLC NAND Flash

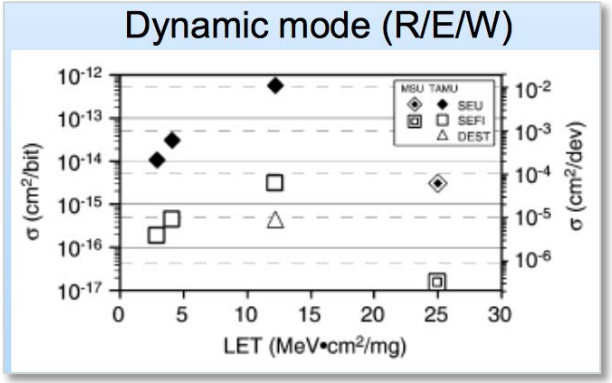


- Extremely low threshold for errors
- Saturation also occurs at relatively low values of LET (<30 MeV-cm2/mg)
- NAND flash will experience large numbers of Single Event induce errors

F. Irom "Nonvolatile Flash Memory Tests"
NEPP ETW 2012

SEE Error Modes





D. Chen "Radiation Qualification of Flash Memories" "Nonvolatile Flash Memory Tests" NEPP ETW 2013

- Single bit upset
  - Memory cell charge leakage
- Multiple bit upset
  - Typically due to control circuit error
- Stuck Bits
  - Micro-dose effects
- Functional Interrupt
  - Control logic error leading to large scale errors (page or block errors)
- Functional Failure

NEPP NAND Radiation Guidelines

Radiation Effects Test Guideline Document for Nonvolatile Memories: Lessons Learned

Prepared by:
Timothy R. Oldham[1], Dakai Chen[2], Stephen P. Buchner[3], and Kenneth A. LaBel[2].

1. Previously with Dell services Federal Government, Inc. in support of NASA Goddard Space Flight Center
2. NASA Goddard Space Flight Center
3. Naval Research Laboratory

For:
NASA Electronic Parts and Packaging (NEPP) Program

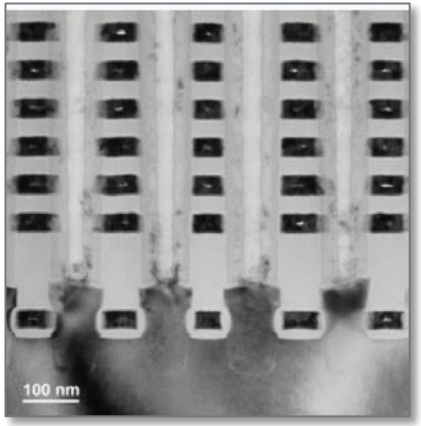
And
Defense Threat Reduction Agency

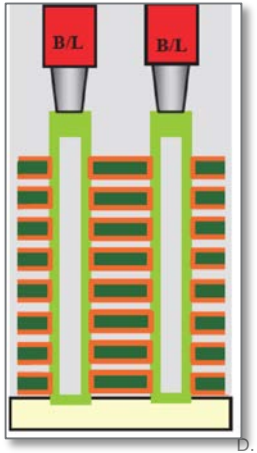
- Specific experimental information & guidance
  - Sample size
  - Pattern sensitivity
  - Test modes
  - Angular effects
- Laser and Proton testing
  - Beam parameters
  - Data analysis
- TID testing
  - Functional and destructive failures
- Error Correction
- Displacement Damage testing

https://nepp.nasa.gov/files/24671/Oldham_2013_NVM_Guideline.pdf

Individual Part vs. Solid State Drives (SSD)

Accelerated cycling endurance test shows 9% wear after writing 72TB in 3 weeks.

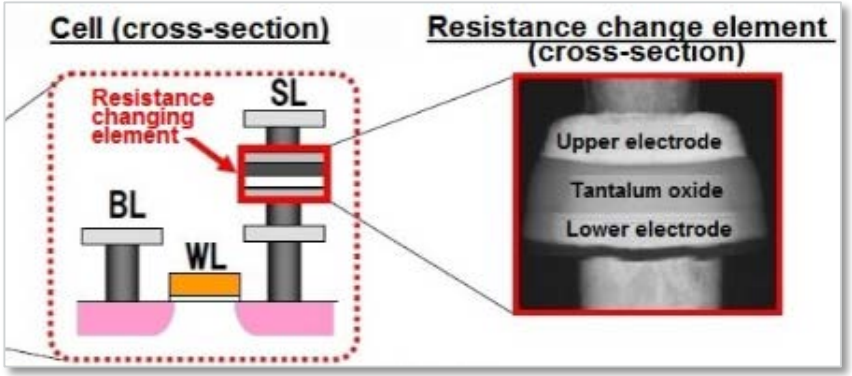


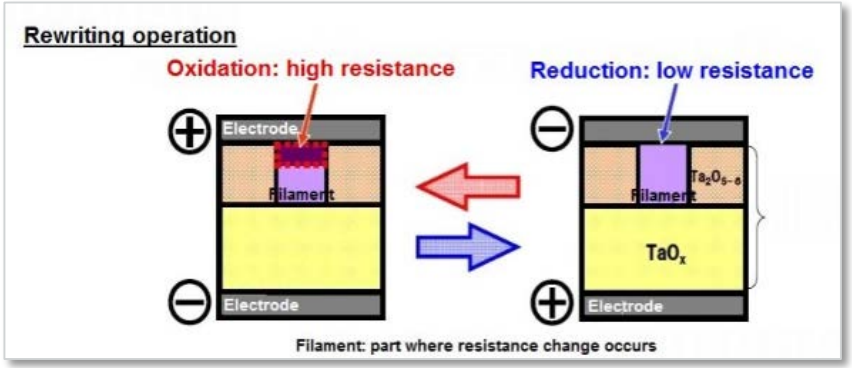


- Individual parts simply not offered, data sheets not provided.
- In SSD, the NAND performance is carefully managed via controller chip and DRAM cache chip with error correction code, wear leveling techniques, spare blocks, data mapping and write buffering.
- SSD Key Metrics
  - Endurance is specified by total bytes written (TBW)
  - Uncorrectable bit error rate (not accessible to the user)
- NAND Key Metrics
  - Endurance is specified by Program/ Erase cycles for each block
  - Raw bit error rate
  - Data retention

Jean Yang-Scharlotta "Nonvolatile Memory Reliability Update", NEPP ETW 2015

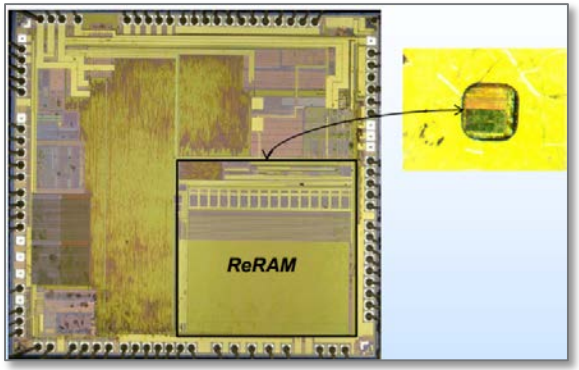
Alternative Non-Volatile Memory Technologies - ReRAM

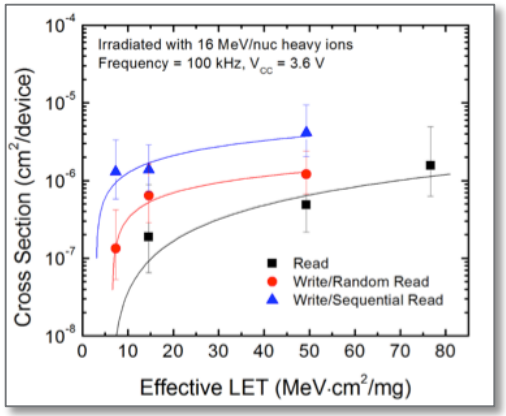




- Simple
- Resistive element between two metal conductors
- Based on reversible reduction reaction at filament near anode due to oxygen vacancy motion
- Difference between high & low resistance states $>10^4$

Alternative Non-Volatile Memory Technologies - ReRAM

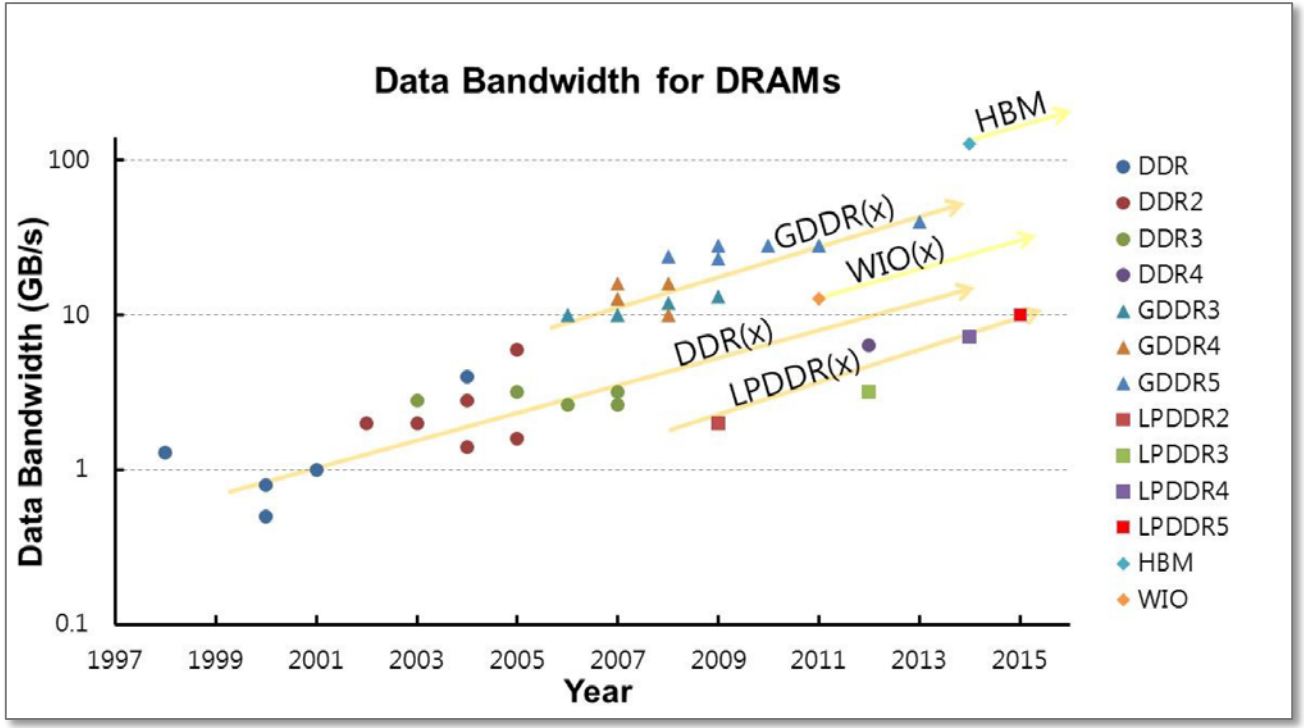




D. Chen "Radiation Effects of Commercial Resistive Random Access Memories" NEPP ETW 2014

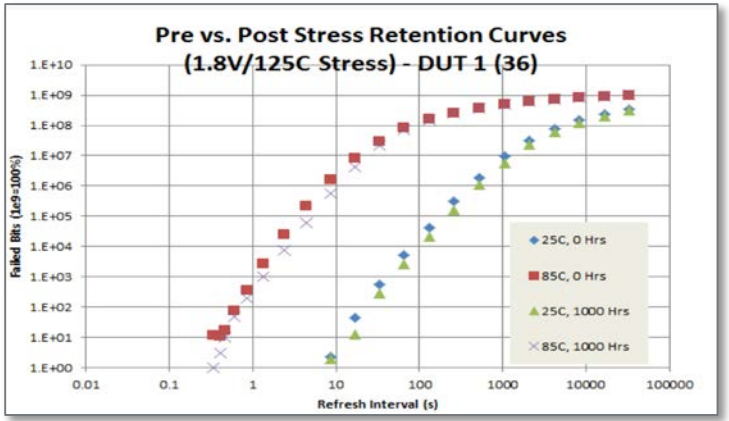
- NEPP has tested:
  - Panasonic – TaO_x
  - Adesto Ag/GeS_2/W
- Embedded with microcontroller and stand alone memory devices
- TID >300krad
- Very small density (<1Mb)
- Complex metallurgy
- Limited P/E cycles
  - 100 to 10,000 cycles

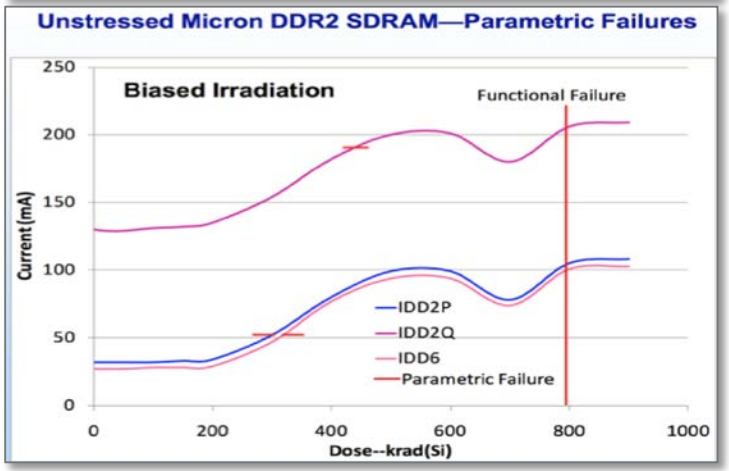
ISSCC 2015 Volatile (DRAM) Bandwidth Scaling



- G=Graphics
  - Less latency and increased bandwidth
  - Internal terminators to handle higher speeds
  - Not related to JEDEC DDRx specification
- LP=Low Power
  - Lower voltage
  - Temperature compensated refresh
- DDR – 2.5V
- DDR4 – 1.2V
- HBM = High Bandwidth Memory

NEPP DDR2 Reliability and Radiation Analysis

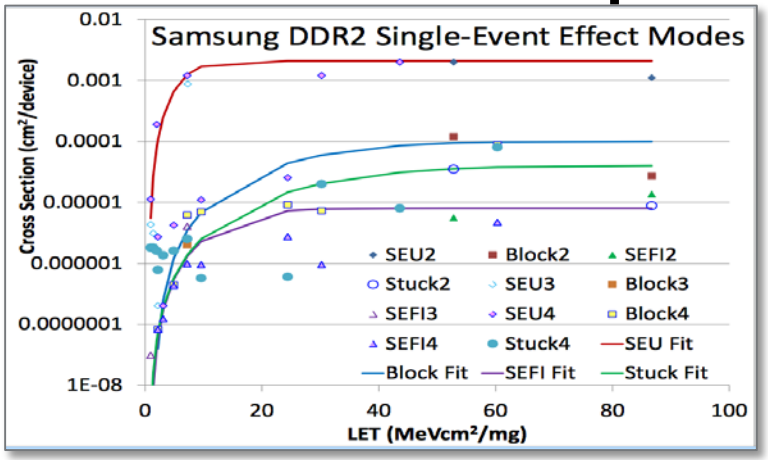


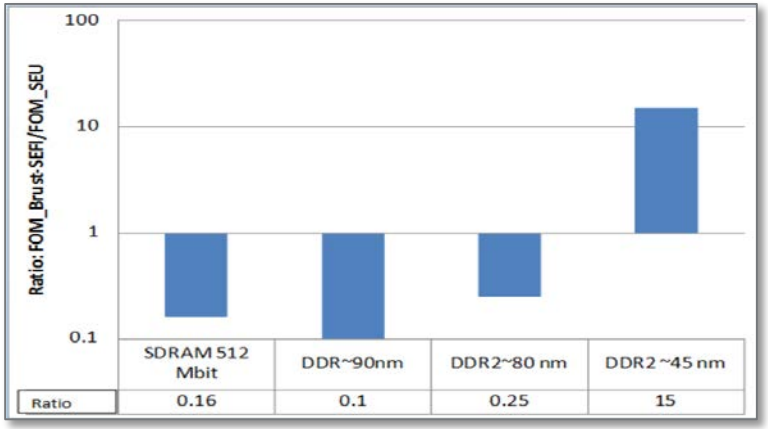


- High resolution testing of refresh bit failures before and after long term life stress
  - No changes in distributions 25C and 85C
  - Strong indicator of long term quality
- Parametric vs. Functional failures demonstrated in TID testing
  - Difference can be 100's of krad
  - Mission specific failures modes can be cultivated

S. Guertin, "DDR2 Device Reliability Update", NEPP ETW 2012

SER in DDR2 and implications for SSR



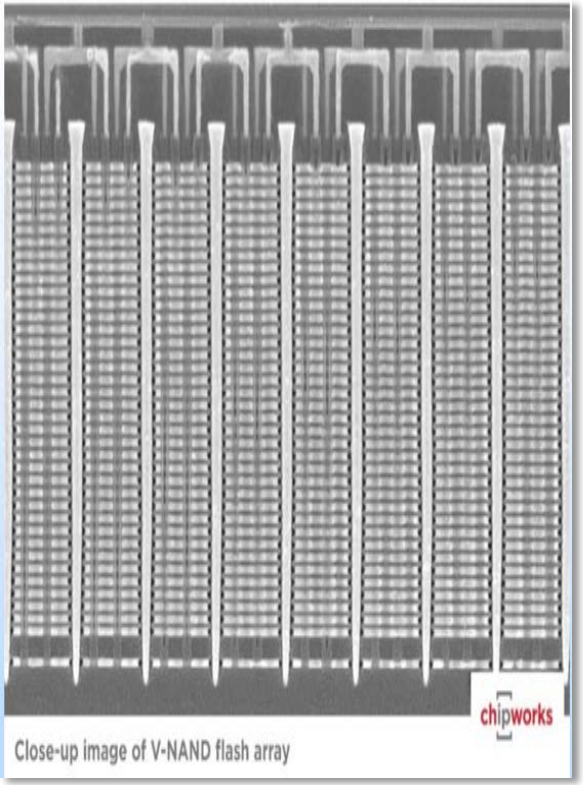


- For DDR2/3, SEU cross section does not scale with effective LET
- Introduces more uncertainty into rate estimation
- SEFI/ block errors still scale, but estimation poor due to poor statistics
- Increasing prevalence of SEFI/block errors vs. SEU
  - Some applications may get by with limited EDAC
  - Some may really need multi-symbol correction
- Commercial memories are too complicated to test completely
- Cannot test all possible operating-mode combinations
- Parts exhibit a variety of disruptive error modes (e.g. SEFI, SEL)

Ray Ladbury, "Update of SSR Guidelines: What Twenty Years of Solid-State Recorders (SSR) Tells Us about the Next Twenty" , NEPP ETW 2013

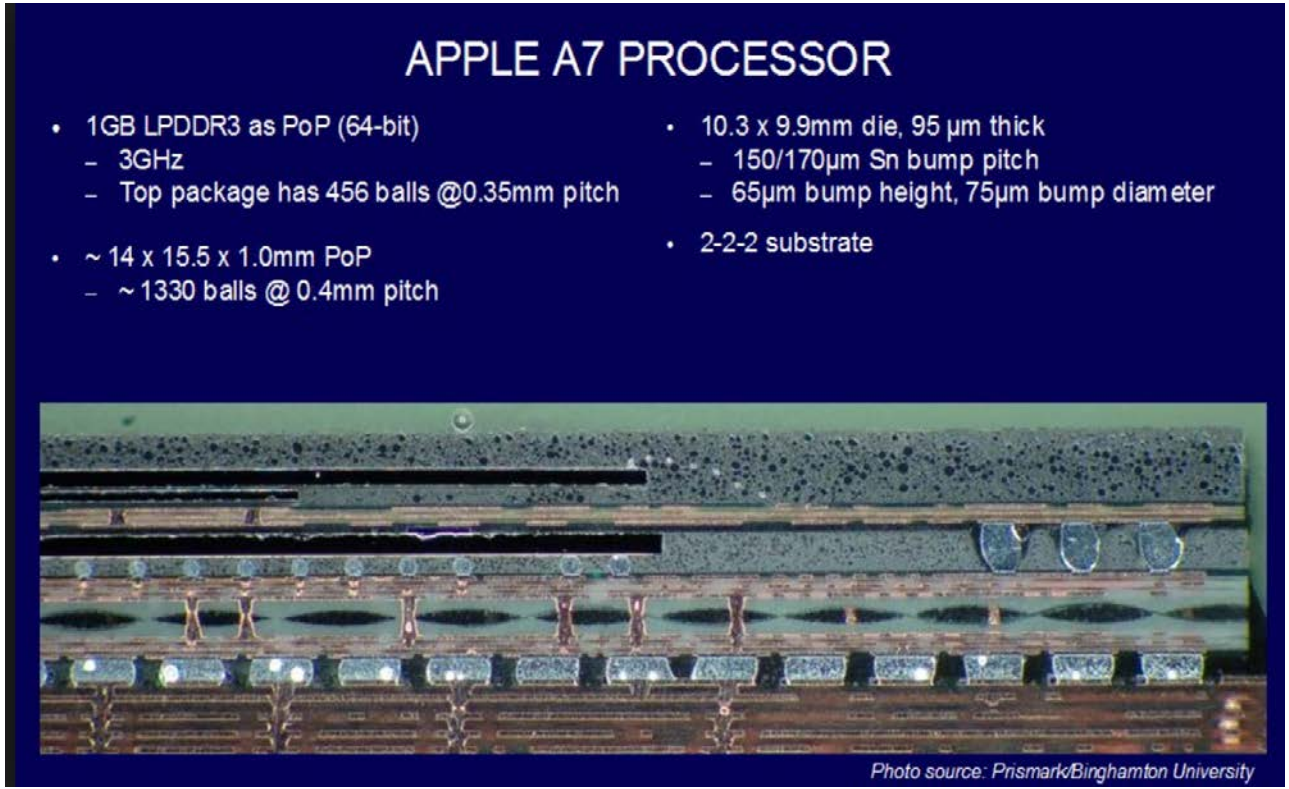
The 3D Revolution is here

Silicon and Packaging



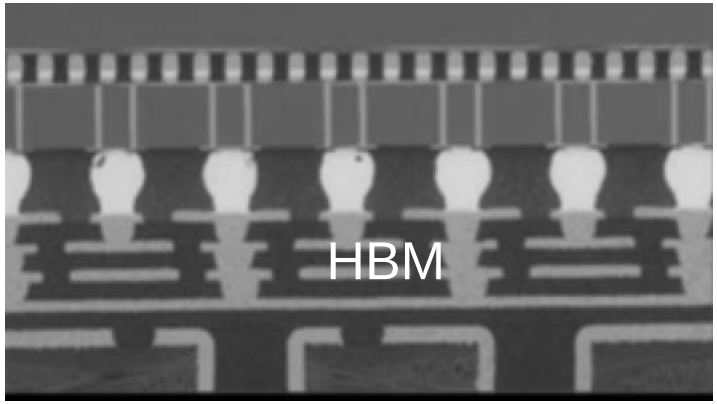
- Moore's law now goes vertical
- NAND devices now have 32-48 different layers of transistors
- Packaging use of interposers are 65nm wafer technology
- Orders of magnitude improvement throughput

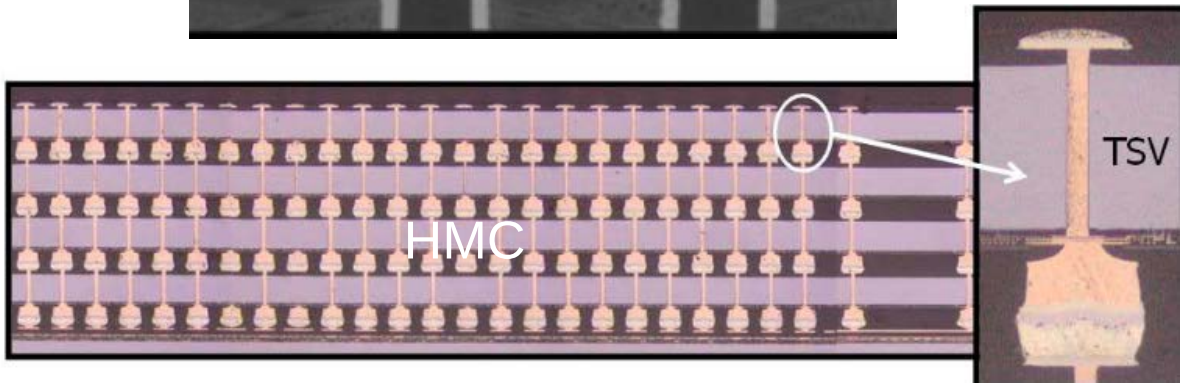
3D is accepted norm in modern COTS



- High throughput memory now can be tens of microns away from processor
- Number of I/O connections increases by 1000X
- Aftermarket (NASA) - To test one you must test both
- Ability to de-process is extremely challenging

High Bandwidth Memory (HBM) vs. Hybrid Memory Cube (HMC)





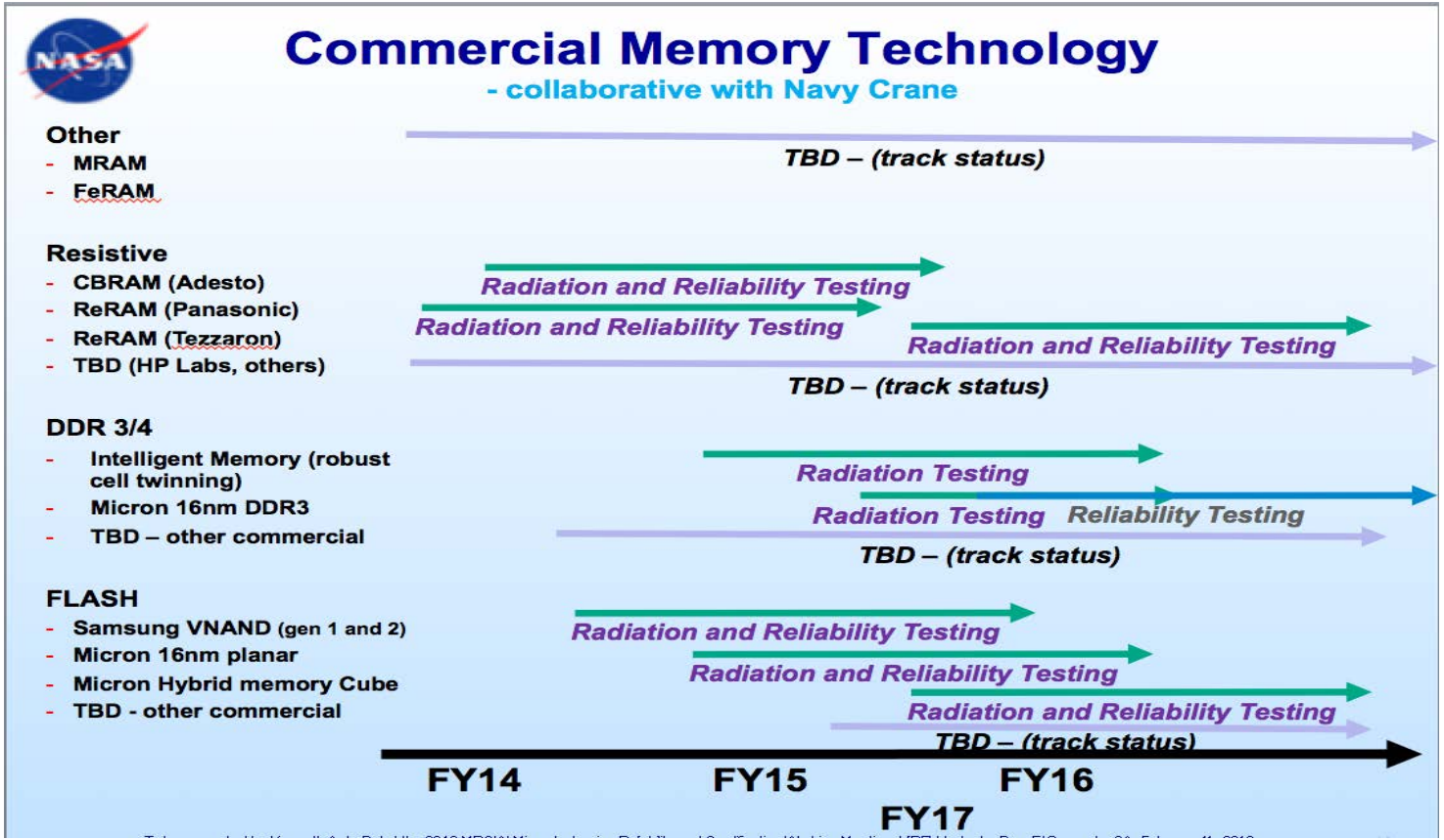
www.techdesignsforums.com

- NEPP is beginning to investigate
- HMC = chip to chip SERDES
- HBM = wide parallel multichannel, DDR signaling
- HMC requires special controller and cross bar switch die
- 256 vs. 240 GB/s
  - (HBM vs. HMC)

Concerns for Space Application of 3D

- Extreme sophistication of 3D devices mean technology qualification and possible failure analysis requires significant increase in practitioner skills and related tools and hardware
- Failure modes have been compounded and confounded
- Many parts are integrated into sub-systems, not available as individual packages
- Radiation interactions with multiple layers of silicon and metal layers

NEPP Memory Roadmap



Conclusions

- NASA's NEPP Program actively monitors, characterizes and analyses the continual evolution of EEE parts memory technology.
- Memory devices remain a fundamental part of any electronics design
- Density and bandwidth now available will have enormous impacts on spacecraft architectures and capabilities.
- The revolution in 3D memory technologies is here now and presents fundamental and gaming chaining challenges to heritage risk assurance methods and processes.
  - Approval, verification, validation, etc. all must evolve to comprehend the changes in the technologies
- Collaboration on qualification is an important means to leverage knowledge and capability

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