

Total Ionizing Dose Response of SDRAM, DDR2 and DDR3 memories

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Abstract— Total Ionizing Dose response of SDRAM, DDR2 and DDR3 memories is reported in static bias, and auto refresh modes. Data analysis reveals some types of memory have significant increases in stuck bits during TID exposure when refreshed.

I. INTRODUCTION

Dynamic Random Access Memory (DRAM) cells are the basis of many high-density and high-speed systems for space applications. This is because DRAM devices are relatively low power compared to faster Static Random Access Memory (SRAM) while still being fast enough to provide high speed main memory or data buffering services. Synchronous DRAMs (SDRAMs) may operate at very slow speeds (a few MHz is the effective lower limit) all the way up to nearly 200 MHz. Newer Double Data Rate (DDR, DDR2, DDR3, DDR4) memories can operate at data speeds in excess of 2 GHz.

This workshop paper provides data on the total ionizing dose (TID) response of one SDRAM, one DDR2, and three DDR3 devices. The devices were studied for their ability to store data over relatively high amounts of TID. We examine the performance of the devices up to target dose levels of around 100 krad(Si) for the SDRAM devices, and 300 krad(Si) (and beyond) for the DDR2 and DDR3 devices.

Although these devices are made of many internal structures, failures are generally limited to two problems. The first is loss of ability to store data, and the second is loss of general functionality of the device. The latter situation sometimes manifests as a rapid increase in the loss of ability to store data in a relatively narrow range of TID. The two failures can easily be confused, and we do not determine which type of failure applies to any given test device.

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Data bits are stored in a DRAM cell by setting the charge in the storage capacitor of the cell. An example DRAM cell is shown in Fig. 1.

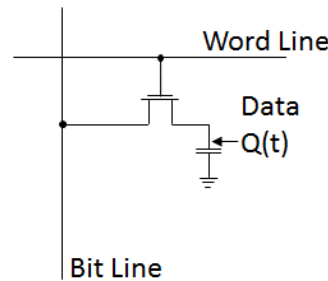


Fig. 1: The structure of a DRAM cell. An access transistor is controlled via the word line. A data bit is stored by forcing charge into the storage capacitor via the bit line. The bit line is connected to a sense amplifier that senses the stored charge during read and resets the cell charge.

The charge stored in the cell, once set, is constantly decaying. This occurs because the circuit has leakage paths, including through the access transistor and directly through the capacitor [1]. Leakage is strongly dependent on temperature, with cells quickly losing too much charge at high temperature and failing to store data. To keep data for a useful period of time, each bit must be periodically refreshed by reading and resetting the stored data. A cell that is unable to return the correct value when read, constitutes a bit error. Fig. 2 shows an example charge vs. time plot.

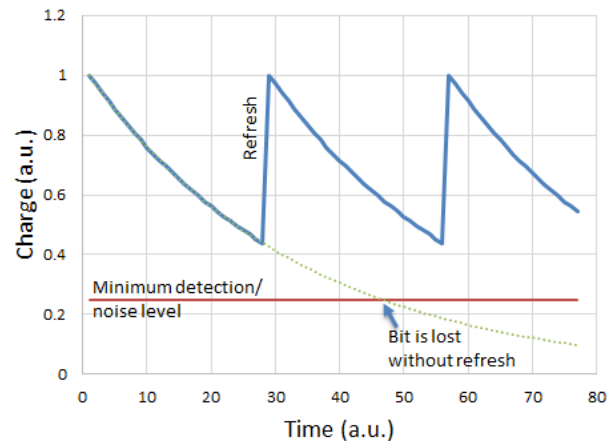


Fig. 2: Example plot of $Q(t)$ for the charge in a DRAM cell. Note that without refresh the bit will eventually fall through the minimum detection level and the bit is lost.

One type of problem that an SDRAM memory cell can experience is the stuck bit. For this workshop, a stuck bit is defined as a bit that is unable to store the data written to it under the conditions of the test being performed. For example, during a test with 64 ms refresh, a bit is stuck if it cannot hold data for 64 ms.

Our experimental results show that there is a geometric relationship between refresh period and increase in the operating temperature. Doubling the refresh period is similar to increasing the operating temperature by 10°C.

To measure the impact of refresh rate, we use four refresh intervals: 32 ms, 1 s, 4 s and 16 s. 32 ms is chosen because it is a standard application period and sometimes required by manufacturers for high temperature operation. 1 s is chosen because it is 32 ms * 2⁵, and therefore similar to operating around 75°C, while 4 s and 16 s are chosen to be arbitrarily larger (something like 95°C and 115°C).

II. TEST SETUP

A. Test Devices and Exposures

TID testing using the JPL high dose rate Cobalt-60 room irradiator was performed on one SDRAM device type, one DDR2 device type and three DDR3 device types. The SDRAM was the ISSI IS42S86400B-7TLI. The DDR2 was the ISSI IS43DR81280. The DDR3 devices were the Micron MT41J128M8JP-15E IT:G, the Samsung K4B1G0446G-BCH9000, and the ISSI IS43TR81280A-15GBLI.

B. Test Procedure

The key to this work is the comparison of static TID sensitivity (where devices are irradiated after being only powered on, and no initialization or operation is performed) and TID sensitivity observed when devices are refreshed (i.e. they are powered-on, configured, initialized with data, and then refreshed during TID exposure). The detailed operation of the test systems for static bias (no-refresh) and refresh-on are provided here.

Devices were irradiated at room temperature, using specification maximum voltage since it is worst-case for TID testing. After initial operational verification, devices were irradiated, then tested to determine if they are working properly, and to identify any inability to store data, and finally they are returned to exposure with less than 30 minutes between the end of one exposure and the beginning of the next one. Generally speaking, devices showing 1% or more of their bits in error at 32 ms or 1 s refresh were considered failures and removed from the study at that TID level.

For “static” testing, devices were biased as is usual for TID testing of CMOS components. The DUT was biased on the power and ground pins to the specification maximum and minimum levels, respectively. All other pins were biased nominally. At power up, no control signals are toggled to the DUT, and the internal state is per the default at power up.

For “no refresh” testing, the following procedure was used. First, devices were tested to verify operation in the test fixture.

Then, the FPGA in the test fixture was reprogrammed, returning the interface to an inactive state (no refresh, and clock enable off, all control signals in nominal state – e.g. chip enable held high). It should be noted that these DUTs were not power cycled, so the internal state remained as during operation. Devices were then exposed to the next TID increment at a rate of 15-20 rad(Si)/s. Following exposure, the devices were tested for stuck bits in the test room using the same bias fixture used for the static testing. After the final stuck bit characterization, devices were stored unbiased at room temperature and allowed to anneal (this is not worst case and is intended for indication only).

For “refresh on” testing, the test procedure is similar to that for “no refresh” bias. In this case, after reprogramming the FPGA, the system is initialized for operation of clock and refresh. For SDRAMs, the last test pattern before FPGA reprogramming is the one in the array at the time of exposure.

C. Test Setup – SDRAM and DDR2

Testing was performed with a custom daughter card mounted to a Xilinx Virtex-4 FX12 [2] development kit by Memec. A forty-pin ribbon cable connected the motherboard to an OpalKelly XEM3005 card [3]. Power was provided to the DUT separately from the test board, and set at 3.6 V for SDRAM and 1.9 for DDR2 (specification maximum voltage). Fig 3. Shows the mentioned test setup.



Fig. 3: SDRAM and DDR2 test setup. interposer card connected to mezzanine card to the FPGA development board.

D. Test Setup – DDR3

Testing was performed with a custom daughter card connected to a Xilinx Virtex-6 ML605 [5] development kit by Xilinx. Power was provided to the DUT separately from the test board, and set at 1.575 V (specification maximum voltage). Fig. 4 shows the mentioned test setup.

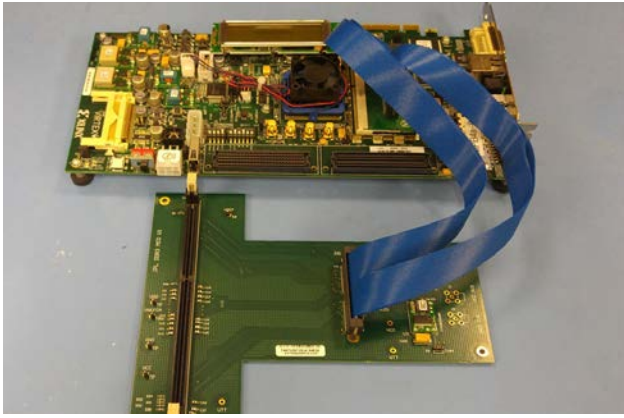


Fig. 4: DDR3 test setup. ML605 board connected to daughter card with a cable.

E. Error Bars

For the data presented here, error bars come from various sources. Most data points in the plots are the result of test data on two devices. In this case, the error bars are the difference between the two measurements. When there are no error bars, it is because one of the two parts has no data (in the case of “full static” data points below, many were single test parts), or because the error bars are smaller than the plotting symbols.

III. TEST RESULTS – SDRAM

A. Nominal Case

For SDRAMs, results are shown in Fig. 5 for the case where the devices are refreshed at 32ms both during exposure (for the refreshed devices) and during post-irradiation readout of the stuck bits conducted at room temperature. Before annealing, the DUTs have a small number of stuck bits for the no-refresh case at 100 krad(Si) while the refresh on DUTs show 10,000s of stuck bits. The figure also shows the effect of a ~168 hour room temperature anneal. After annealing, both the no-refresh and refreshed DUTs improved by multiple orders of magnitude. No-refresh DUTs had significantly lower number of stuck bits after annealing. By contrast, under nominal TID test conditions, represented by the full static point at 150 krad(Si), clearly the full static test condition is not worst-case for these devices.

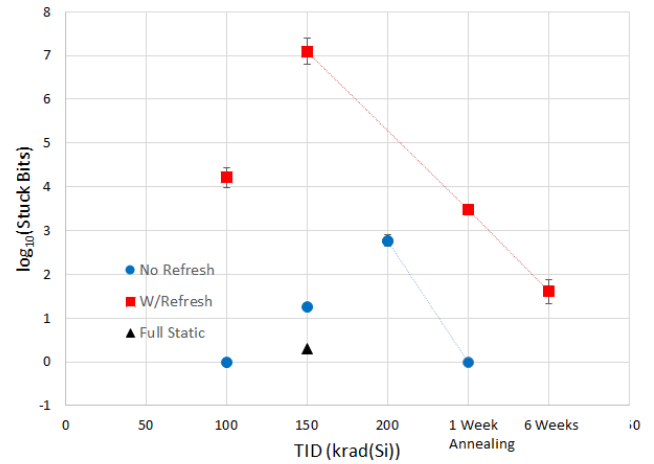


Fig. 5: SDRAM stuck bits vs. TID for devices with refresh on, no refresh, and in full static mode. Devices were irradiated with and without refresh, but stuck bit measurements were taken with device refresh set at 32 ms. The annealing points were taken after 168 hours of unbiased room temperature annealing and after 6 weeks of annealing. No refresh points at value zero are one device with one stuck bit and the other without. The full static point reflects only one test device.

Fig. 6 below shows results for the same parts as in Fig. 5, but where the stuck bit counts were taken between exposure with the DUTs refreshed at 1 s instead of 32 ms. That is, the devices were irradiated at 32 ms refresh rate, and then they were characterized for performance after each exposure with refresh rates of 32 ms and 1 s.

We also explore the number of stuck bits as a function of the selected refresh period in Fig. 7. As discussed earlier, the selected refresh periods roughly equate to operating at room temperature, 75°C (for the 1 s points), and around 95°C for the 4 s points). This shows that what appears to be acceptable at room temperature (especially considering the annealing in Fig. 5) is clearly not acceptable at higher temperature.

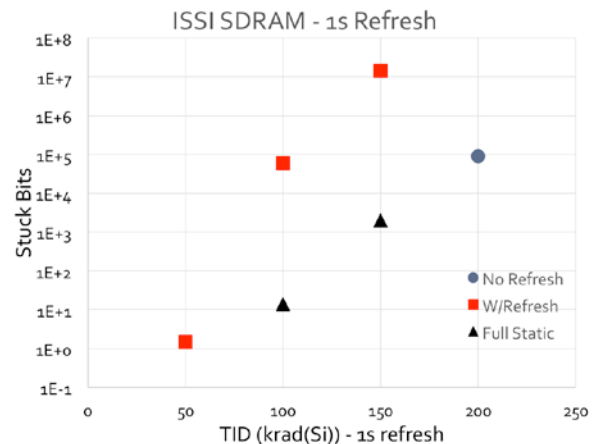


Fig. 6: SDRAM stuck bits vs. TID for devices with refresh on, no refresh, and in full static mode. Devices were irradiated with and without refresh (refreshed at 32 ms during exposure), but stuck bit measurements were taken with device refresh set at 1 s. The annealing points were taken after 168 hours of unbiased room temperature annealing.

B. Refresh Period

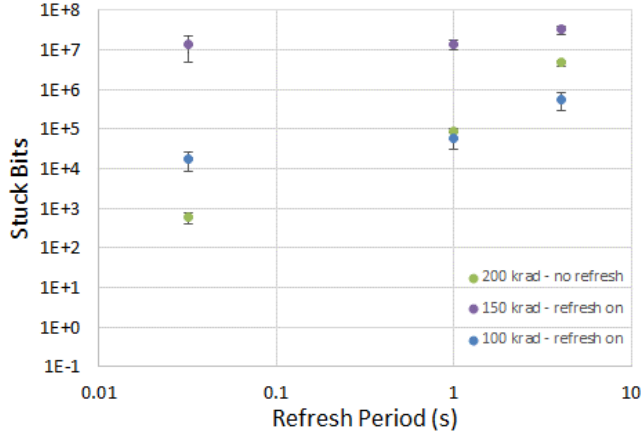


Fig. 7: SDRAM stuck bits vs. refresh period at the highest TID point tested. Note that the refresh-on devices show a flatter response curve.

C. Stuck Bit Distribution

Stuck bits that occur during irradiation by a uniform source, such as Co-60 photons, protons, or neutrons, are believed to be due to the combination of a statistical distribution of damage applied to a statistical distribution of cell properties. An underlying assumption is that neither of these distributions is dependent on position within the device. This can be explored by examining the distribution of stuck bits. A visual representation of stuck bits is presented in Fig. 8.

In Fig. 8 each cell reflects the stuck bit information collected from all the rows in a single column in a single bank after proton exposure (which creates a pseudo-uniform TID and displacement damage distributions). Each cell thus represents 2,048 bytes. The darkest cells are rows with no errors. The next brightest cells are those with one error. And the very brightest cells are those with two or more. No individual column was observed to have more than a single stuck bit (i.e. no single transfer of an 8-bit data output showed more than a single stuck bit).

As can be seen in the figure, the distribution of stuck bits appears to be random. We have not formally tested this for consistency with a uniform distribution; however, the patterns seen in the figure, and the wide-spread nature of single stuck bits strongly suggest a uniform distribution. If a specific portion of the array, or a specific decoding operation – data transfer, or row or column contributed to stuck bits, then bands, clumps of bright spots, or other obvious patterns would be expected in Fig. 8.

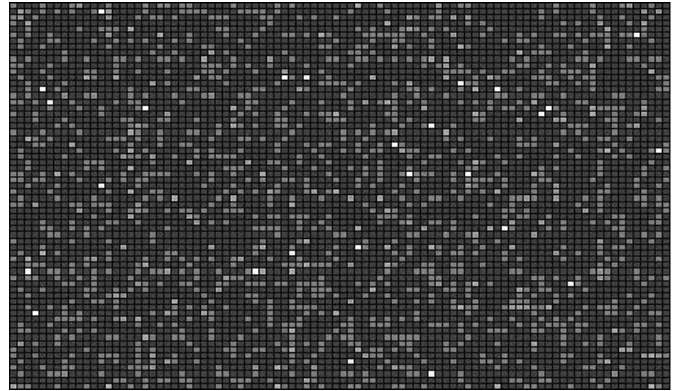


Fig. 8: Distribution of stuck bits in a sample SDRAM device. Darkest to lightest represent 0 to 2 or more stuck bits in a single DRAM row (where an individual row contains 2,048 columns (each column is a single byte of storage)).

IV. TEST RESULTS – DDR2

The DDR2 devices were exposed in both the full static and refresh-on conditions. The results are presented in Fig. 9 and Fig. 10 where the devices were allowed to sit for 4s and 16s respectively after writing before reading (in order to simulate an elevated temperature). We show only 4 s and 16 s because the 1 s data showed no stuck bits throughout all the testing. The goal for device usage was 300 krad(Si) so data collection was discontinued after 400 krad(Si), no device failures were observed.

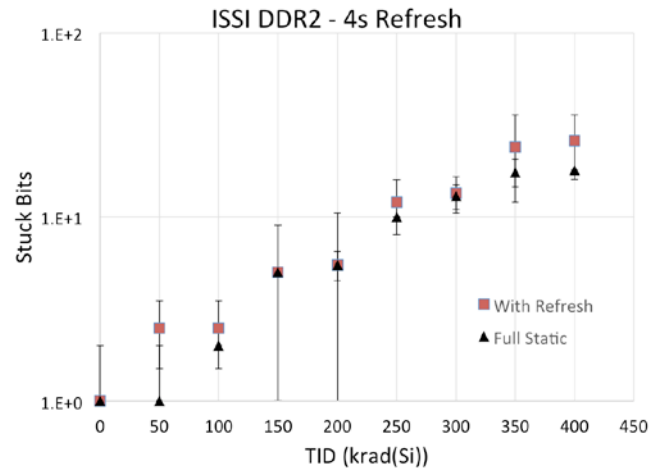


Fig. 9: Comparison of no-refresh and refresh-on stuck bits at room temperature for the ISSI DDR2 devices (using 4 s delay).

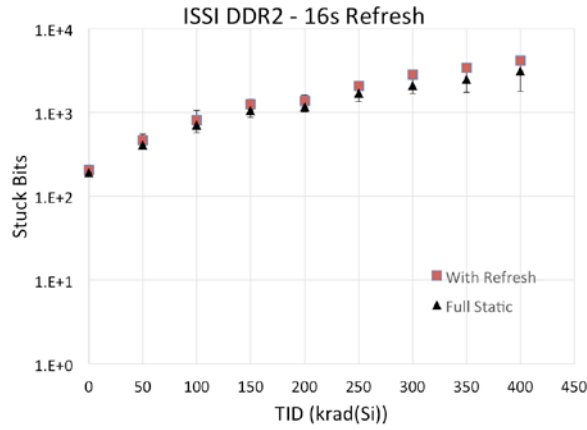


Fig. 10: Comparison of no-refresh and refresh on stuck bits at room temperature for the ISSI DDR2 devices (using 16 s delay).

For DDR2, stuck bit distributions were only checked to verify there were not multiple stuck bits in a single column (a single read of data bits from the device). With this method we verified that our test devices only rarely provided data from a single transfer of data with more than one stuck bit. The occurrence rate of these multiple bit errors was consistent with uncorrelated coincidence of single bit errors.

V. TEST RESULTS – DDR3

The three DDR3 devices were exposed in both the no-refresh and refresh-on conditions. During irradiation the refresh-on devices were refreshed at 32 ms. The results discussed below refer to the post-irradiation characterization tests on these exposed devices, where the post-irradiation tests are performed with varying refresh rates on the same devices. Some of the no-refresh exposures were fully static-biased, while others involved initialization of the device with a data pattern. The former are referred to as Full Static, while the latter are referred to as Without Refresh.

The results are presented in Fig. 11 for the Micron devices where the devices were allowed to sit for 1 s after writing before reading (in order to simulate an elevated temperature), Fig. 12 for the Samsung devices where the devices were allowed to sit, without refresh, for 1 s after writing before reading (in order to simulate an elevated temperature), and Fig. 13 for the ISSI devices where the devices were allowed to sit for 1 s after writing before reading (in order to simulate an elevated temperature).

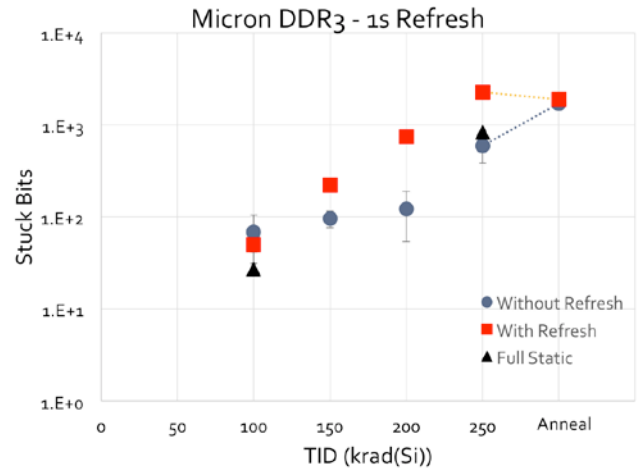


Fig. 11: Comparison of no-refresh and refresh on stuck bits at room temperature for the Micron DDR3 devices.

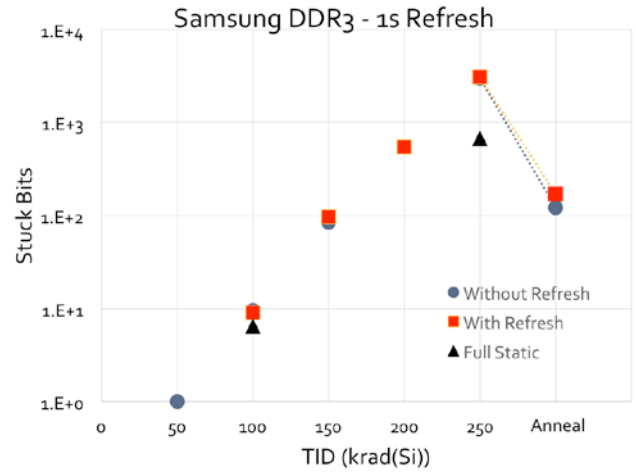


Fig. 12: Comparison of no-refresh and refresh on stuck bits at room temperature for the Samsung DDR3 devices.

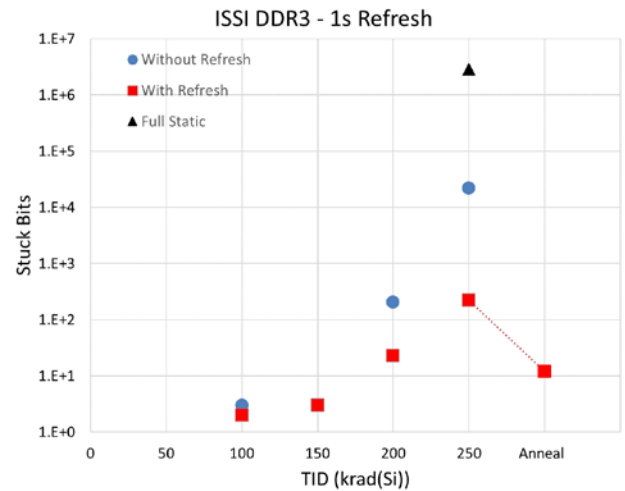


Fig. 13: Comparison of no-refresh and refresh on stuck bits at room temperature for the ISSI DDR3 devices.

Micron and Samsung DDR3 device types show more stuck bits in most test patterns and delays, except that at room temperature the devices that were not refreshed show more

stuck bits than the refreshed devices. ISSI DDR3 devices on the other hand show more stuck bits in cases of no-refresh and full static compared to refresh on case.

VI. CONCLUSION

Total Ionizing Dose responses of SDRAM, DDR2 and DDR3 memories have been presented. The difference in stuck bit sensitivity between testing in full static and using refresh was studied. Stuck bit sensitivity to refresh can be severe in SDRAM devices as we have seen up to 5 orders of magnitude higher stuck bits when using refresh. DDR2 devices show not much difference and DDR3 devices showed inconclusive results.

As the mechanism or mechanisms involved in the varied results are not known, no clear recommendation for test mode can be made. Results seem to indicate that refresh on and static bias test modes should both be used when worst-case testing is required. Similarly, for possible flight situations, such as cold sparing, no clear recommendation can be made.

Annealing appears to reduce the difference between test methods. The method for examining stuck bit and annealing effects is unclear because the worst case for stuck bit behavior (high temperature) is the best case for annealing, and it is difficult to provide general data when flight profiles can complicate this interplay significantly.

VII. ACKNOWLEDGMENT

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VIII. REFERENCES

- [1] J. Yu, and K. Aflatooni, "Leakage Current in DRAM Memory Cell", University/Government/Industry Microelectronics Symposium, 16th Biennial, pp. 191-194, (2006)
- [2] Memec Virtex-4 MB development board user's guide, version 3.0, (2005)
- [3] Opal Kelly XEM3005 datasheet; <https://www.opalkelly.com/products/xem3005/>
- [4] ML605 Hardware User Guide UG534 (v1.8) October 2, 2012 http://www.xilinx.com/support/documentation/boards_and_kits/ug534.pdf