Single Event Testing of SDRAM, DDR2 and DDR3 memories

Steven M. Guertin, *Member, IEEE,* and Mehran Amrbar

***Abstract*— SEE test results are presented for SDRAM, DDR2, and DDR3. No tested devices exhibited SEL. SBUs were observed, but no MBUs were observed in data words. SEFI data were taken at low and high speed.**

I. Introduction

Dynamic Random Access Memory (DRAM) devices are used in many electronics systems for space use. DRAMs are the most common and effective memory type for providing a balance between high performance, high density, and low power. Some space systems utilize older Synchronous DRAM (SDRAM) devices for heritage or low operating speed reasons. Other applications have used the more recent Double Data Rate devices (DDR), with the 2nd and 3rd generations being the most common for space use (DDR2 and DDR3).

Single-Event Effects (SEE) performance was studied for use in a high total ionizing dose (TID) environment. The devices studied include one SDRAM type, one DDR2 type, and three DDR3 types. The SDRAM tested was the ISSI 512 Mb IS42S86400B-7TL which was reported on for heavy ion SEE in [1], and is used in some SDRAM-based modules from 3D Plus [2]. Other SDRAM options were excluded from study here due to TID considerations. The DDR2 device studied is the ISSI 1 Gb IS43DR81280B-25DBLI. This device functioned sufficiently for the program that no other devices were tested. And the DDR3 devices tested were Micron 1Gb MT41J128M8JP-15E IT:G, Samsung 1 Gb K4B1G0446G-BCH9TCV, and ISSI 1Gb IS43TR81280A-15. Multiple DDR3 devices were tested as part of an effort to identify the device type best suited for the high TID environment.

This paper is organized as follows. Background on the test methods is presented in Section II. We then present the SDRAM testing and results in Section III. This is followed by the DDR2 testing and results in Section IV. DDR3 testing and results are presented in Section V. And finally the conclusions are presented in Section VI.

Manuscript received July 15, 2016. The research in this paper was carried out at the Jet Propulsion Laboratory, California Institute of Technology, under a contract with the National Aeronautics and Space Administration. Reference herein to any specific commercial product, process, or service by trade name, manufacturer, or otherwise, does not constitute or imply its endorsement by the United States Government or the Jet Propulsion Laboratory, California Institute of Technology. This work was supported by NASA flight projects.

Steven M. Guertin is with the Jet Propulsion Laboratory, California Institute of Technology, Pasadena, CA 91109 (USA), phone: 818-393-6895, e-mail: steven.m.guertin@jpl.nasa.gov.

Mehran Amrbar is with the Jet Propulsion Laboratory, California Institute of Technology, Pasadena, CA 91109 (USA), phone: 818-354-1390, e-mail: mehran.amrbar@jpl.nasa.gov.

II. Background

As indicated above, the device types studied here are of general interest for spacecraft designers for several reasons. The primary reason why the devices meet all the performance parameters they do is because the basic unit of data storage is a 1-transistor, 1-capacitor cell as indicated in Fig. 1 The charge in the capacitor is constantly decaying through leakage paths. The charge is read by opening the access transistor and allowing the charge to create a pulse on the bit line which is observed by a sense amplifier. Once the pulse direction is detected, the sense amplifier forces the value back down the bit line, which refreshes the bit. There are two key properties of the individual cell that give rise to radiation phenomena. The first property is that the data stored in the capacitor can be lost due to ionizing radiation causing a pathway through the access transistor or another part of the circuit. This phenomenon is referred to as a single bit error (SBU). Alternately, an ionizing radiation event may weaken the cell by increasing leakage current. This can result in cells that are unable to store data during the period between refreshes (the refresh period). A bit that loses data before it is refreshed is referred to as a stuck bit.

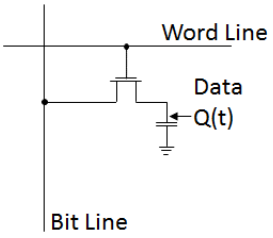

Fig. 1: The standard 1-T, 1-C DRAM cell.

DRAM devices are constructed as complimentary metal-oxide semiconductor (CMOS). For SEE considerations, this means they are potentially sensitive to single-event latchup (SEL) occurring in parasitic silicon controlled rectifier structures in the device. The sensitivity of devices to SEL must be tested to ensure devices meet requirements for flight systems.

The block structure, or architecture of a device gives rise to two other types of SEEs of interest. First, when an ion hits, it is likely in advanced device nodes, for more than one bit to upset as a result. The logical-to-physical arrangement of the

bits determine whether the bits with upsets are delivered to the output pins together. If a set of bit upsets from a single ion are observed together at the output pins, we refer to this case as a multiple bit upset (MBU). Another type of SEE that is architecture dependent is the single event functionality interrupt (SEFI). Although SEFI is used as a catch-all term for SEEs that do not fit the other categories, they are generally the result of control circuitry in the device being upset, and this results in the data delivered to the output pins being essentially unrelated to the original data, so that in an 8-bit device most addresses would be expected to deliver information with several bits in error. We have loosely defined a few types of SEFIs as follows: a row SEFI results in multiple columns in a specific row having errors; a band SEFI results in multiple rows having one or more columns in error; and a million-error SEFI (MSEFI) is an event where a large region (or the entire device) exhibits corrupt data. MSEFI observations may due to the device becoming non-responsive.

Stuck bits are difficult to deal with in the context of a heavy ion or proton test because they result in damage that exhibits annealing behavior. The mechanism where stuck bits manifest – leakage current – is greatly amplified as temperature is increased, so they should be observed with the device operating at maximum temperature. However, this results in accelerated annealing. Further, during SEE testing, it can often be very difficult to control the amount of time between exposures, resulting in lack of control on how much annealing occurs. In order to have a controlled method for reporting stuck bits, we observe the number of bits that lose their charge when not refreshed for one second while operating at room temperature. By utilizing the approximation that every 10°C results in approximately a doubling of leakage current, we can compare 32 ms refresh at room temperature with 1 s refresh at room temperature, where the latter is similar to testing the device at 75°C with 32 ms refresh. This relationship can be inferred from bit retention data taken at different temperatures in [3].

The cross section for stuck bits can be determined under three conditions. First, the baseline number of stuck bits before an exposure is known (i.e. due to previous dose history on the test device). Second the exposure time is small compared with the annealing time. And third, if the measurement is repeated several times, showing an approximately linear relationship between TID level and number of observed stuck bits.

III. SDRAM

A. Test Setup

Proton testing was performed on the ISSI IS42S86400B-7TL SDRAM at the University of California, Davis (UCD) Crocker Nuclear Lab (CNL) in April, 2015. Three samples were used for this testing, indicated as DUT0 (device under test 0), DUT1, and DUT2. These devices experience some changes to performance with TID values in excess of 80 krad(Si). Most test runs were performed at an effective dose rate of 135 rad(Si)/s, although some were as low as 10 rad(Si)/s.

Devices were irradiated with 65 MeV protons only, as the device performance suggested that lower energy protons would produce very few SEEs while resulting in significant accumulation of TID. 65 MeV protons have a range of about 19 mm in Si. Care was taken to keep proton exposure limited to 80 krad(Si) on individual DUTs, however the data were taken in a way to enable evaluation of possible TID influence on SEE behavior.

Testing was performed with a custom daughter card mounted to a Xilinx Virtex-4 FX12 [4] development kit by Memec. A forty-pin ribbon cable connected the motherboard to an Opal Kelly XEM3005 card [5]. Power was provided to the DUT separately from the test board, and set at 3.6 V (specification maximum voltage). Tested devices were mounted to grand daughter cards that held them away from the test hardware. Although there were likely some changes to DUT temperature during exposure (due to increased current), we were careful to indicate and require a minimum temperature for testing, and estimate uncertainty in temperature at less than 5°C. The devices did not require any package modifiction to facilitate proton SEE testing.

B. Test Results – General and SBU

The test results are separated into SBUs, SEFIs, and stuck bits. The summary of proton-induced SBUs observes is given in Table I, below. This table gives the observed SBUs for each DUT and the total fluence on each DUT. The overall SBU sensitivity is seen to be $6.0\pm1.8\times10^{-20}$ cm^2/bit for 65 MeV protons on the ISSI IS42S86400B-7TL SDRAM, when tested with a pseudo-random pattern. Note that the uncertainty indicated is 2-σ. It should be noted that for DUT1 and DUT2, the data were taken at 1×10^{11}/cm^2 steps, with observed counts having no discernable pattern and varying from 0 to 6 SBUs observed. Some SBUs were mixed with stuck bits, especially later in the TID exposure of the DUTs. The stuck bits were subtracted from the observed SBU count to arrive at values that were due to actual SEE.

Table I: Proton SBU Sensitivity of ISSI IS42S86400B-7TL SDRAM

DUT	Proton Fluence	SBUs	Cross Section	Dose
0	1.1×10^{11} /cm^2	6	1.0×10^{-19} (cm^2/bit)	15 krad(Si)
1	6.0×10^{11}	20	6.2×10^{-20}	80
2	6.0×10^{11}	16	5.0×10^{-20}	80
All	1.3×10^{12}	42	$6.0\times10^{-20}\pm1.8\times10^{-20}$	175

C. SEFI Results

The SEFI sensitivity of the ISSI IS42S86400B-7TL SDRAM is given in Table II. In fact, with 175 krad(Si) exposure divided among the three DUTs, there were no SEFIs observed. As a result, the upper bound for the cross section is seen to be 2.8×10^{-12} cm^2/device at 65 MeV, where the observed 0 is replaced by 3.7 as the 2-σ estimate when no events are observed.

Table II: Proton SEFI Sensitivity of ISSI IS42S86400B-7TL SDRAM

DUT	Proton Fluence	SEFIs	Limiting Cross Section	Dose
0	1.1×10^{11} /cm^2	0	3.3×10^{-11} (cm^2/device)	15 krad(Si)
1	6.0×10^{11}	0	6.2×10^{-12}	80
2	6.0×10^{11}	0	6.2×10^{-12}	80
All	1.3×10^{12}	0	2.8×10^{-12}	175

D. Stuck Bit Results

During collection of SEE phenomena, the devices were accumulating dose and the cells were losing the ability to store data efficiently. We evaluated the stuck bit sensitivity of the device, as discussed in Section II, by measuring the number of bits that cannot store data for one second, when programmed with a pseudo-random pattern. This data retention period mimics high temperature operation while being relatively simple to perform and having little impact on potential annealing. Fig. 2 shows the observed stuck bits at one second refresh for all three DUTs as observed after each test run, with the exception of DUT0 which was measured after several test runs that included some experimental delays that resulted in time for limited annealing. The DUTs show a sensitivity of about 30 stuck bits/krad(Si). DUT1 was placed in an oven after the final exposure and allowed to anneal at 75°C for three hours. After this annealing, more than 50% of the stuck bits recovered.

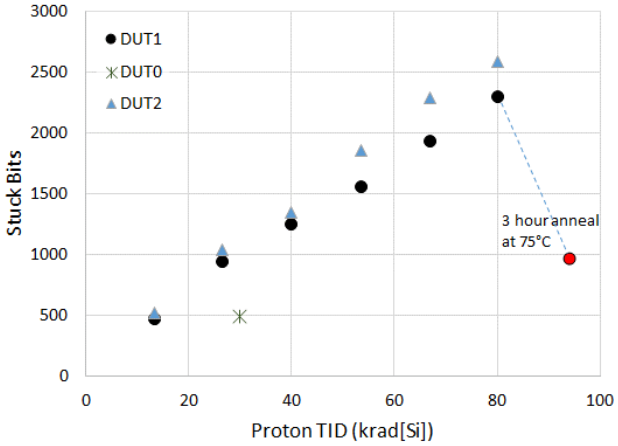

Fig. 2: Stuck bit accumulation during proton testing of three ISSI IS42S86400B-7TL SDRAMs.

E. MBU Analysis

Data files were analyzed for multiple bit upsets (MBUs). A standard numerical method for determining the number of expected read operations with more than 1 bit in error, assuming all the bits in the read operation were uncorrelated, yielded an expected number of read operations with more than 1 bit in error. The ratio of observed MBUs to predicted MBUs (from statistical chance) is shown in Fig. 3.

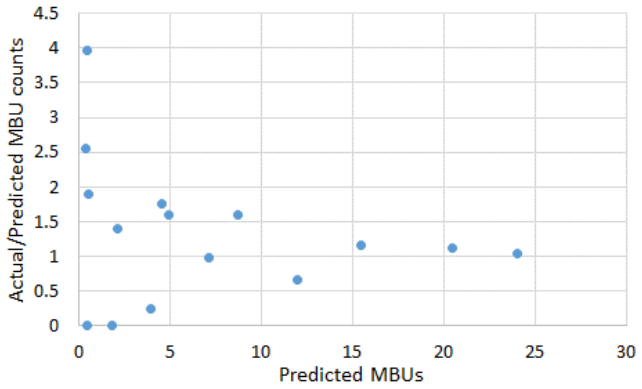

Fig. 3: The ratio of observed MBUs to expected MBUs (due to independent pileup) for all proton test data (including those taken with refresh delays of 1 and 4 s)

IV. DDR2

Because of the observed performance in TID testing related to this work, and the observed heavy ion data reported here, the ISSI 1 Gb, 1.8 V IS43DR81280B-25DBLI was tested only for heavy ion SEL, SBU, MBU, and SEFI.

Testing was performed at the Texas A&M University (TAMU) cyclotron facility in October, 2015. The ions used are given in Table III.

Table III: Ions used in heavy ion testing of ISSI IS43DR81280B-25DBLI

Ion	LET after 80 μm Si	Total Fluence
Ta	85.3 MeV-cm^2/mg	4.1×10^7/cm^2
Ag	53.6	3.1×10^6
Cu	26.4	1.1×10^6
Ar	10.4	3.6×10^7
Ne	3.1	8.9×10^7

The DDR2 hardware was the same as the SDRAM hardware except for a couple specific differences. First, the mounted test devices were thinned so that the beam could penetrate the back of the die and reach the sensitive region. All DUTs were thinned to thicknesses between 60 and 80 um. Second, in order to enable collection of bit-level data for saving to a capture file, a low-speed operations firmware (DUT clock of 33 MHz) was developed. But this firmware did not run the device with the delay-locked loop (DLL) enabled. Thus, a second firmware was used in testing that operated the DUT at 125 MHz, provided bit error information, but did not provide error maps.

A. SEL Results

Three devices were tested for SEL sensitivity. No SEL was seen with a total exposure of 4.1×10^7/cm^2, of Ta with linear energy transfer (LET) of 85.3 MeV-cm^2/mg, although only 1×10^7/cm^2 of the exposure occurred at an operating voltage of 1.9 V. The remainder was applied at 1.8 V. SEL testing was performed with the device temperature set at 95°C, with a thermocouple placed on the DUT card near the device and a heat gun directed at the die. Devices did demonstrate increased-current operating modes, but self-recovered,

indicating the events were not SEL. A current strip chart for the 1.9 V exposure is provided in Fig. 4.

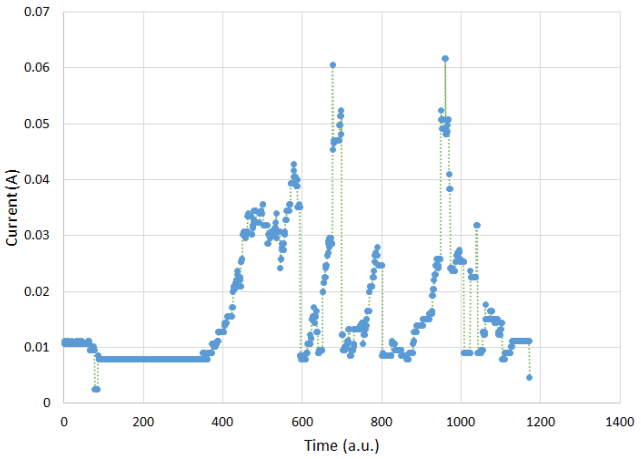

Fig. 4: Current strip chart of device during exposure to 1×10^7/cm^2 of Ta at LET of 85.3 MeV-cm^2/mg

B. *SEFI Results*

The ISSI IS43DR81280B-25DBLI was observed to have MSEFI events. These events resulted in the device no longer functioning correctly and requiring device reset to recover. The cross section for these events is shown in Fig. 5. Note that the two data points at LET 10.4 MeV-cm^2/mg demonstrate that for the MSEFI event type there is little difference between low-speed read operation and high-speed write operation. The data point at LET 53.6 MeV-cm^2/mg demonstrates something of an outlier behavior, but the results are statistically limited. All MSEFIs were recoverable by re-initializing the device, power cycle was not required.

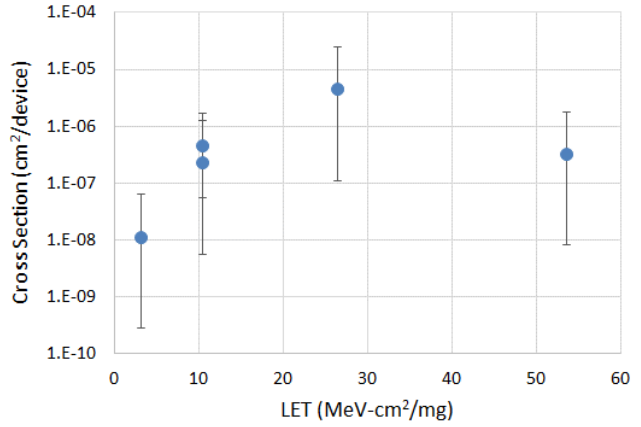

Fig. 5: The cross section for MSEFI events in the ISSI IS43DR81280B-25DBLI is shown. The two data points at LET 10.4 show the MSEFI sensitivity of the low-speed read operation compared to the high-speed write operation.

Other SEFIs were observed, including one type that results in a few hundred errors occurring in the device. Another, called a phantom SEFI resulted in a few hundred errors in the device, but those errors would correct themselves on the next read of the device. The cross section for these SEFIs (all other types, combined) is shown in Fig. 6. All SEFIs categorized as "other" were recoverable by re-initializing the device, power cycle was not required.

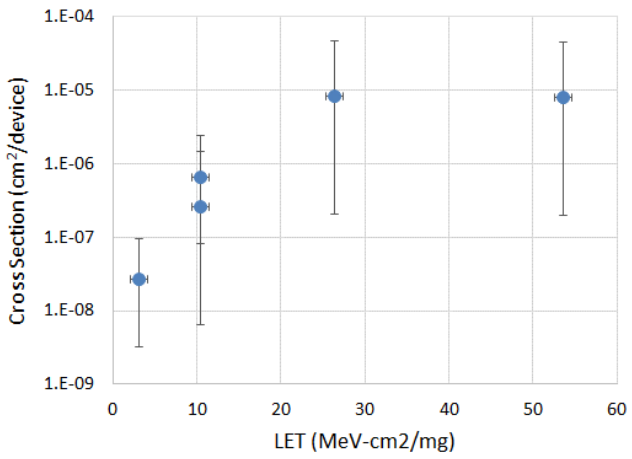

Fig. 6: Cross section for other SEFI types (multiple types, combined) in the ISSI IS43DR81280B-25DBLI DDR2.

C. *SBU Results*

SBU data were collected on the ISSI IS43DR81280B-25DBLI DDR2. At higher LETs the data are difficult to separate from the SEFI behaviors. For lower LETs the SBU data are presented in Fig. 7.

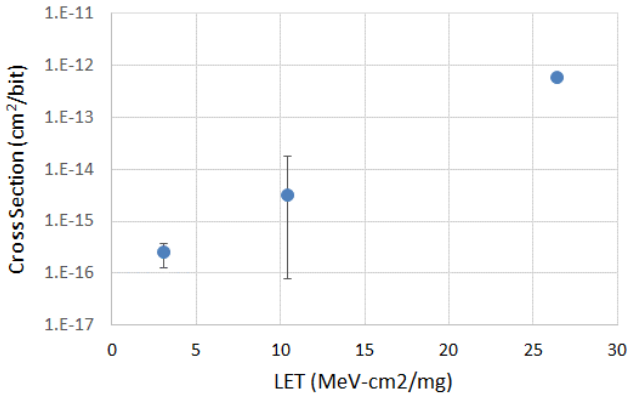

Fig. 7: The SBU sensitivity of the ISSI IS43DR81280B-25DBLI DDR2.

D. *MBU Results*

During data collection some images of errors were observed with a graphical interface that allowed quick determination of the apparent uniformity of the bit upsets. Later statistical analysis was performed on error counts to determine that only a small number of individual read operations from the DUT resulted in MBUs (unless there was a SEFI). The number of events observed was consistent with uncorrelated coincidence, and our data shows no evidence of MBUs from individual ion strikes.

V. DDR3

Testing was performed on three DDR3 devices, selected to obtain a general understanding of behavior across various options for a high TID NASA flight project concept. The devices tested were the Micron 1 Gb MT41J128M8JP-15E IT:G, Samsung 1 Gb K4B1G0446G-BCH9TCV, and ISSI 1

Gb IS43TR81280A-15. These devices were tested for SEL, SEFI, and SBU, using both protons and heavy ions. For programmatic reasons, the ISSI device was eliminated from consideration after the SEL testing (due to TID limitations).

The primary test system was based on the Xilinx ML-605 Virtex 6 evaluation board. The test system is shown in Fig. 8. DUTs were mounted to unregistered dual inline memory modules (U-DIMMs, or UDIMMs). For detailed test data, custom firmware was used. This firmware was not reliable at high speed, so it is used for indication of error patterns, and it is combined with data taken at high speed to ensure that error types (including bit errors and SEFIs) provide consistent results – otherwise high speed data should be used, rather than low speed. Low speed operation was performed with the delay-locked-loop (DLL) in disabled mode. Because this is not a standard mode, low speed data alone cannot be trusted.

The high-speed test system is the same as the low-speed system except that the DUT is mounted to small outline DIMMs (SODIMMs) rather than UDIMMs and the SODIMMs are mounted directly to the evaluation board. The high-speed test system only tests 128 Mb of the Samsung parts, and 256 Mb of the ISSI and Micron parts. This is because the number of tested addresses is only 32 million. The high speed system performs writing and reading repeatedly.

The low-speed test system only tests 512 Mb of the Samsung parts, so that the number of addresses tested between the two architectures is the same. The low-speed system can run static (write, dwell, read after exposure), read mode (write, then repeat read during exposure), and write mode (write, then read, and repeat).

A. SEL Results

SEL testing on the devices was performed at TAMU in September, 2014. Testing was performed with a bias system based on a Xilinx ML-605 board [6], but unable to interact with the DUT to determine functionality. After each test, functionality was confirmed by utilizing a Eureka-2 test system [7] to perform functional verification tests of the DUTs. All SEL testing was performed with a heat gun used to bring the DUT temperature over 70°C, measured using an infrared thermometer before the start of exposure. The results are presented in Table IV. The ISSI device type was subsequently removed from study for reasons other than SEE response.

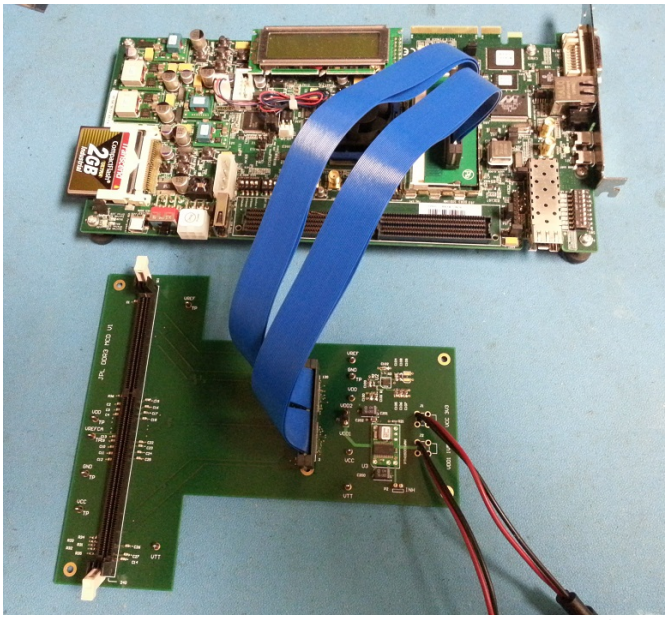

Fig. 8: The custom DDR3 test system - low speed testing was performed using the UDIMM socket. High speed testing was performed on DUTs mounted to SODIMM cards and plugged directly into the ML-605 motherboard.

Table IV: Summary of SEL exposures for DDR3 devices at 70°C.

DUT ID	Manufacturer	Exposure	LET @ 60°	Voltage	SEL
9389	Micron	2.70E+07	75 MeV-cm^2/mg	1.58	No
2699	Micron	2.00E+07	75	1.58	No
2695	Micron	2.00E+07	75	1.58	No
9390	ISSI	2.00E+07	75	1.58	No
9387	Samsung	2.00E+07	75	1.58	No
9388	Samsung	2.00E+07	75	1.58	No
2697	Samsung	2.00E+07	75	1.58	No

B. Proton Results

Devices were tested for protons at UC Davis in April 2014, and at TRIUMF in August 2014. Testing covered two energies – 65 and 108 MeV. We present first the SEFI results, followed by the SBU results.

SEFIs dominated the proton testing for the Micron parts, though some SBUs were observed (but they cannot be separated from possible stuck bit behavior). The primary SEFI type observed during proton testing was corruption of 4 bits in approximately 4096 addresses for each SEFI. Results are presented in Fig. 9. It can be seen that the fast and slow systems have consistent SEFI response even though operating speed is different by a factor of 10.

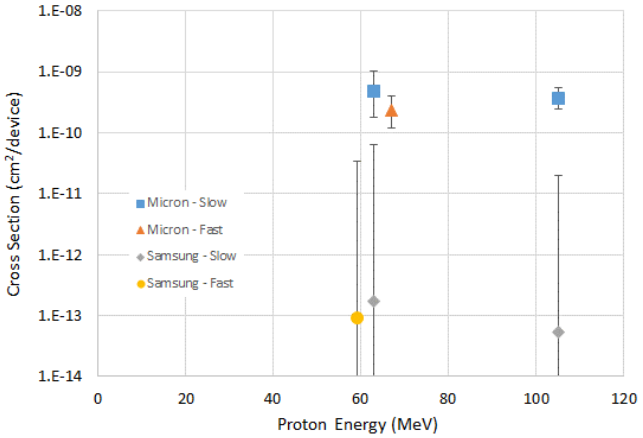

Fig. 9: SEFI results for fast and slow operation of Micron and Samsung devices under proton exposure. Some x-axis values are offset for clarity.

Limiting SBU cross section for the Micron parts was determined, along with the cross section for SBUs observed in the Samsung parts. The cross sections are provided in Fig. 10.

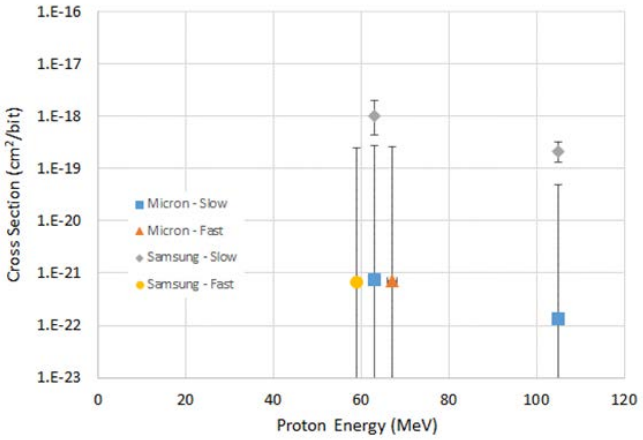

Fig. 10: SBU results for Micron and Samsung DDR3 devices - note that error bars on 0-SBU points are drawn with the data point at 0.01 events.

C. *Heavy Ion SEFI Results*

The primary SEFI type observed during proton testing of the Micron part was corruption of approximately 4,096 addresses. The test record indicates that errors are only observed in 4 out of 8 bits (i.e. as SEFIs occur, they are seen to result in increases of about 2048 errors in 4 of the bit reports). This suggests these SEFIs actually impact 4096 addresses, with an average of two incorrect bits per address (this level of detail was not verified directly).

The primary SEFI type observed during heavy ion testing of the Samsung part was similar to the MSEFI described above for the ISSI DDR2 device. In this case, the Samsung x4 SDRAM appears to have errors at essentially every address in the device.

The cross section versus LET is provided for the DDR3, devices using both the fast and slow test systems, in Fig. 11.

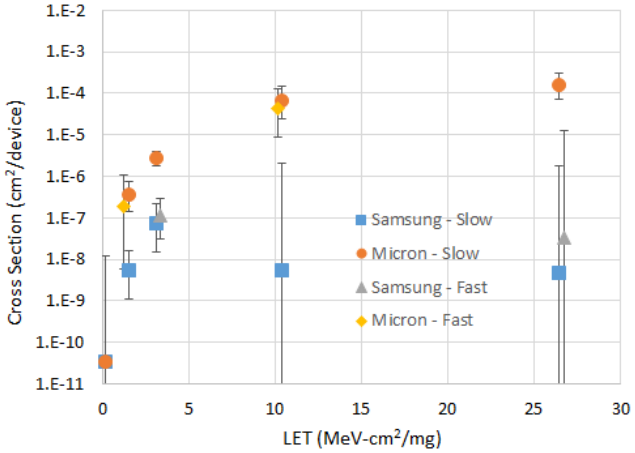

Fig. 11: Heavy Ion SEFI results. Note that in places where fast and slow data are both available, the results are consistent for both devices.

D. *SBU Results*

Up to the limits of the SEFI contamination, SBU results were obtained on the Samsung and Micron DDR3 devices. The results are shown in Fig. 12. Although the Micron data are dominated by SEFIs before SBUs could be observed, the limiting cross sections are not significantly lower than for the Samsung. And they both saturate around 3×10^{-13}cm^2/bit.

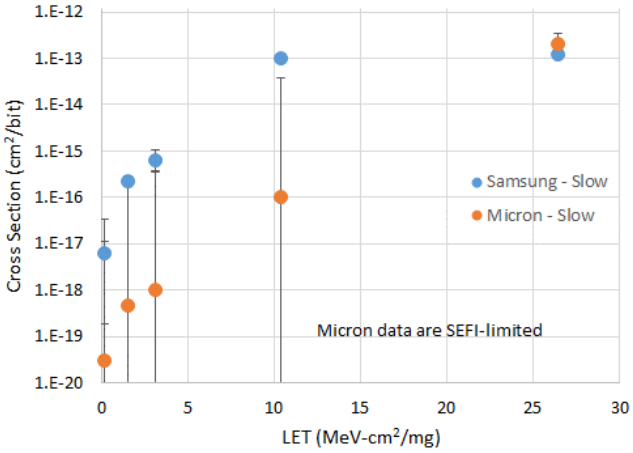

Fig. 12: SBU results for both Micron and Samsung devices. At lower LET, the SEFI response dominates the Micron data.

VI. Conclusion

SEE testing of SDRAM, DDR2, and DDR3 devices was performed as part of an effort to identify options for use in a NASA flight project concept. The devices were selected based on availability and expectation of TID performance, which is why only one option for SDRAM (ISSI IS42S86400B-7TL), and one for DDR2 (ISSI IS43DR81280B-25DBLI) are reported on here. DDR3 devices were less known in terms of TID performance and as a result three devices were tested (Micron MT41J128M8JP-15E IT:G, Samsung K4B1G0446G-BCH9TCV, and ISSI IS43TR81280A-15).

The ISSI SDRAM heavy ion performance was previously reported. This workshop covers proton testing of these devices, showing an SBU cross section of $6.0\pm1.8\times10^{-20}$ cm^2/bit and SEFI cross section with an upper bound of

2.8×10^{-12} cm^2/device at 65 MeV. We also looked at stuck bits as a result of proton testing, where we observed an effective cross sensitivity of 30 stuck bits/krad(Si).

The ISSI IS43DR81280B-25DBLI DDR2 was tested for heavy ion SEE. The device was shown to be immune to SEL to an LET of 85.3 MeV-cm^2/mg, at 95°C. It showed two general categories of SEFIs that influence SEE testing. The first is an MSEFI sensitivity. The other consists of sections of memory that have errors and/or errors observed during read, that upon rereading the data, it goes away. SBU data were collected on the device, but may be contaminated by SEFIs at higher LETs.

Testing of DDR3 devices included the Micron 1Gb MT41J128M8JP-15E IT:G, Samsung 1 Gb K4B1G0446G-BCH9TCV, and ISSI 1Gb IS43TR81280A-15. All three devices were shown to be immune to SEL. The ISSI device was subsequently removed from study. SBU and SEFI results on the Samsung and Micron devices were collected using both fast and slow (DLL-disabled) test systems. Results showed that the Micron devices had significantly higher SEFI sensitivity – with a proton cross section of around 1×10^{-9} cm^2/device and heavy ion saturated cross section of around 3×10^{-4}cm^2/device compared to the Samsung device's below 5×10^{-11}/cm^2 for protons, and approximately 1×10^{-6} cm^2/device for heavy ions. Both devices were observed to have SBU and SEFI at the lowest test LET (though cross sections were significantly smaller than saturation). Heavy ion SBU saturated cross section on both devices is around 3×10^{-13} cm^2.

VII. Acknowledgment

The research was carried out at the Jet Propulsion Laboratory, California Institute of Technology, under a contract with the National Aeronautics and Space Administration. This work was supported by NASA flight projects.

VIII. References - TBD

[1] F. Irom, and M. Amrbar, "Heavy Ion Single Event Effects Measurements of 512Mb ISSI SDRAM", Radiation Effects Data Workshop, IEEE, pp. 1-6, Boston, 2015

[2] 3D Plus website, http://www.3d-plus.com/index.php (January 2016).

[3] K. Saino, et. al. "Impact of the Gate-Induced Draing Leakage Current on the Tail Distribution of DRAM Data Retention Time," IEDM Technical Digest., pp. 837, 2000

[4] Memec Virtex-4 MB development board user's guide, version 3.0, (2005)

[5] Opal Kelly XEM3005 datasheet; https://www.opalkelly.com/products/xem3005/ (January 2016)

[6] Xilinx ML605 Evaluation Kit, http://www.xilinx.com/products/boards-and-kits/ek-v6-ml605-g.html, (January, 2016).

[7] Eureka-2 tester website, http://www.simmtester.com/page/products/eureka/eukinfo.asp, (January 2016).