

# Fabricating with crystalline Si to improve superconducting detector performance

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**Abstract.** We built and measured radio-frequency (RF) loss tangent,  $\tan \delta$ , evaluation structures using float-zone quality silicon-on-insulator (SOI) wafers with 5  $\mu\text{m}$  thick device layers. Superconducting Nb components were fabricated on both sides of the SOI Si device layer. Our main goals were to develop a robust fabrication for using crystalline Si (c-Si) dielectric layers with superconducting Nb components in a wafer bonding process and to confirm that  $\tan \delta$  with c-Si dielectric layers was reduced at RF frequencies compared to devices fabricated with amorphous dielectrics, such as  $\text{SiO}_2$  and  $\text{Si}_x\text{N}_y$ , where  $\tan \delta \sim 10^{-3}$ . Our primary test structure used a Nb coplanar waveguide (CPW) readout structure capacitively coupled to LC resonators, where the capacitors were defined as parallel-plate capacitors on both sides of a c-Si device layer using a wafer bonding process with benzocyclobutene (BCB) wafer bonding adhesive. Our control experiment, to determine the intrinsic  $\tan \delta$  in the SOI device layer without wafer bonding, also used Nb CPW readout coupled to LC resonators; however, the parallel-plate capacitors were fabricated on both sides of the Si device layer using a deep reactive ion etch (DRIE) to access the c-Si underside through the buried oxide and handle Si layers in the SOI wafers. We found that our wafer bonded devices demonstrated  $F \cdot \delta = (8 \pm 2) \times 10^{-5}$ , where  $F$  is the filling fraction of two-level states (TLS). For the control experiment,  $F \cdot \delta = (2.0 \pm 0.6) \times 10^{-5}$ , and we discuss what may be degrading the performance in the wafer bonded devices as compared to the control devices.

## 1. Introduction

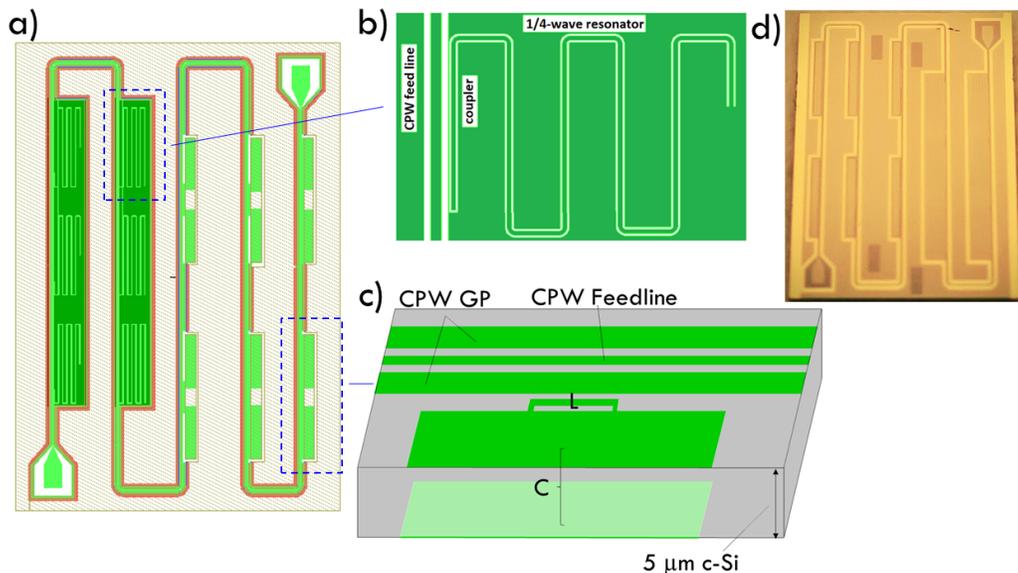
Future space-borne missions using spectrometers operating in the sub-millimeter (sub-mm) and millimeter wave (mm-wave) region require technological advancements over the state-of-the art to meet flight mission design goals and objectives. Superconducting kinetic inductance detectors (KIDs), superconducting microstripline structures in phased-array antennae, and superconducting microstripline networks for filtering and light routing hold great promise for space-mission instrument needs if lower loss dielectrics can be utilized in construction. Currently, amorphous dielectrics such as  $\text{SiO}_2$  and  $\text{Si}_x\text{N}_y$  are used due to their simplicity in fabrication. The loss tangent,  $\tan \delta$ , in amorphous dielectrics is approximately  $10^{-3}$ . Amorphous, hydrogenated Si (a-Si:H) has been reported to have lower loss with  $\tan \delta$  between  $0.3\text{-}5 \times 10^{-5}$  [1]. However, among common semiconductor fabrication materials, crystalline Si (c-Si) has been reported to have the best reported  $\tan \delta$ , with  $\tan \delta$  as low as  $10^{-6}$  [2]. We briefly describe the benefits which c-Si may afford in superconducting KIDs and microstriplines before describing how we pursued c-Si in this report.

Superconducting phased-array antennae rely on microstriplines formed from superconductor-dielectric-superconductor structures to define beam shapes from the sky and route signals through on-

chip filters before detection by other superconducting detectors such as transition edge sensors (TESs) [3] or KIDs [4]. Losses in the microstrip require the detectors to be placed near the antenna, potentially leading to unwanted absorption of light that has not been coupled through the antennae. Furthermore, the efficiency of the phased array antenna is ultimately affected by loss in the microstrip. By reducing this loss through the use of c-Si dielectrics, as opposed to amorphous  $\text{SiO}_2$  or  $\text{Si}_x\text{N}_y$ , detectors can both be moved further away from the antennae to reduce stray pickup and larger, multiscale antennae covering more spectral bandwidth could be designed.

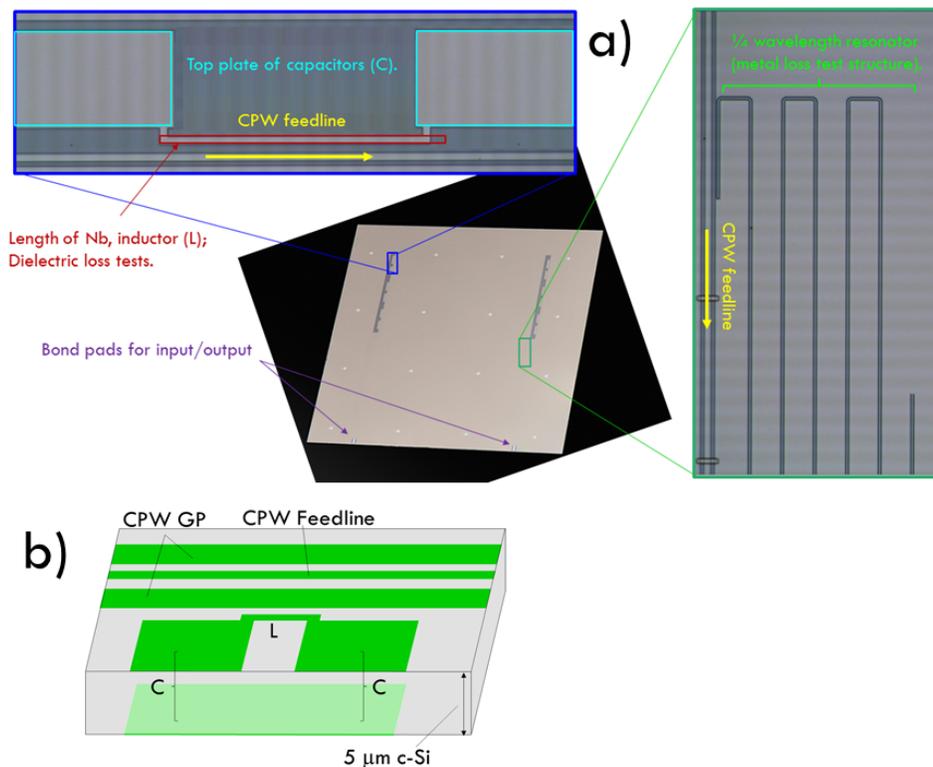
Spectrometers-on-a-chip, such as SuperSpec [5], also use superconducting microstripline networks to effectively couple light onto the chip and route the light to different detectors to produce lower mass, smaller spectrometers. Currently, the resolving power of such spectrometers is  $R \sim \lambda/\Delta\lambda \sim 1/\tan\delta=1,000$ . By utilizing c-Si,  $R$  may improve to on the order of 100,000. Such a development would enable resolved extragalactic mm/submm spectroscopy, where intrinsic line widths are  $\Delta\nu/\nu \sim 10^{-4}$  to  $10^{-3}$ .

Finally, KID noise performance degrades when amorphous dielectrics with two-level states (TLS) reside in the portion of the detectors where electric fields exist [6]. Experiments reveal that moving KIDs to other substrates, such as sapphire that lack TLS, greatly improves baseline noise performance. Due to the crystalline structure, c-Si will not contribute TLS, thus expanding the range of applications where KIDs can obtain photon noise-limited performance [7].



**Figure 1:** Our wafer bonded RF test structure. a) A schematic of the whole device, which consisted of six LC resonators and six  $\frac{1}{4}$ -wave resonators made using superconducting Nb and crystalline Si (c-Si) of  $5\ \mu\text{m}$  thickness. The Nb was patterned on both sides using a robust wafer bonding fabrication process. We determine the loss tangent,  $\tan\delta$ , by measuring the frequency shift of the LC resonators versus temperature. There are two bond pads for connection to the coplanar waveguide (CPW) readout in the bottom left and top right of the device. [b]The  $\frac{1}{4}$ -wave resonators serve as metal loss test structures but are not examined in this work. c) A schematic slab-cut of the LC resonators showing the CPW feedline readout capacitively coupled to a length of Nb serving as the inductor (L). The capacitor for each of the LC resonators is a parallel-plate capacitor (C). d) An optical picture of the actual device.

Here, we report on our effort to use this extremely low loss material for dielectric layers in superconducting KIDs and microstriplines. The scope of this report focuses on validating low loss at RF frequencies, and future work will explore sub-mm and mm-wave validation of low loss tangent in c-Si. We quantify the loss tangent of c-Si from two experiments using c-Si layers in silicon-on-insulator (SOI) wafers. One experiment, our control experiment, measured LC resonators at RF frequencies formed using the c-Si device layer in a SOI wafer using a deep reactive ion etch (DRIE) process to make parallel-plate superconducting Nb capacitors. Our main experiment used wafer bonding to build more robust LC resonator structures using the c-Si layer. The wafer bonded structure was robust because the parallel-plate capacitors were supported on the underside, whereas the control structure resulted in free standing capacitors that were essentially membranes of thickness equal to the c-Si thickness of  $5\ \mu\text{m}$ . Robust construction is important for the future production of superconducting KIDs or microstriplines to be used in actual instruments, which must survive qualifications such as shake testing.



**Figure 2:** Our control experiment RF test structure. a) Optical images of the actual device showing zoomed in images of the LC resonators, which have 2 parallel-plate capacitors (C) and an inductor (L) formed from a length of superconducting Nb. The devices were also made with superconducting Nb and c-Si of  $5\ \mu\text{m}$  thickness. In contrast to the wafer bonded test device, we patterned on both sides of the c-Si using a deep reactive ion etch (DRIE) process. The DRIE results in suspended membranes of  $5\ \mu\text{m}$  thickness, which is not robust for larger scale production of devices or flight hardware. However, this device allows us to determine if wafer bonding affects the loss tangent of c-Si dielectrics. (Again, the metal loss test structures are shown but not discussed in this work.) b) A schematic of the LC resonators with two parallel-plate capacitors to clarify how this device differs in LC resonators from the wafer bonded device in Fig. 1. (There is no qualitative difference in using 1 or 2 parallel-plate capacitors, and the use of two in this device was based solely on the availability of photomasks.)

## 2. Design and fabrication

The wafer bonded RF test device and RF control test device both began with a SOI substrate consisting of a 5  $\mu\text{m}$  thick, float-zone quality, c-Si device layer with  $> 10,000 \Omega\cdot\text{cm}$  sheet resistivity. Below the device layer was a buried oxide (BOX) layer of thickness 750 nm, below which was a Si handle wafer of 500  $\mu\text{m}$  thickness. Both sides of the wafer were polished. The 5  $\mu\text{m}$  c-Si device layer served as the c-Si for our measurements, and it was important that the c-Si was float-zone quality and with high sheet resistivity to avoid unwanted TLS states and other loss mechanisms seen in lower quality c-Si due to dopants and impurities. The superconducting metal used for these tests was superconducting Nb, with transition temperature of around 9 K.

### *2.1. Wafer bonded RF test structure*

The main test structure we built was an RF frequency loss test structure using a wafer bonding process. We expect the wafer bonding process to produce robust fabricated structures that could be modified and infused into devices usable by instruments, especially flight projects. In Fig. 1, we show a schematic and picture of the wafer bonded RF test structure. The readout is carried out through a Nb coplanar waveguide (CPW) line that meanders from one bond pad to another, capacitively coupled to 6 LC resonators and 6 metal loss test structures. The metal loss test structures are designed for future measurements and not discussed further here. The LC resonators were designed to operate at RF frequencies between 2-4 GHz, and consisted of an inductor with a parallel-plate capacitor, as shown schematically in Fig. 1.

Initially, the SOI wafer was dipped in buffered oxide etch (BOE) for 45 seconds, to remove native oxide, and immediately loaded into our Nb sputtering chamber. A 190 nm thick Nb film was sputter deposited and subsequently etched to define a ground plane and the bottom plate for capacitors in the LC resonators. A rim of Au was then lifted off around the rim of the ground plane, to allow us to later etch down from the other side of the c-Si layer to short the top and bottom grounds together—the Nb etch, a F-based reactive ion etch (RIE) etches Si but not Au. Due to the thickness of the c-Si, we were not able to view fabrication alignment marks through the c-Si from the other side, so our final step on this side of the c-Si layer was to use DRIE to etch alignment marks through the c-Si to allow alignment from the other side. Benzocyclobutene (BCB) [8] was then applied to the patterned side of this wafer, as well as a new float-zone quality,  $>10,000 \Omega\cdot\text{cm}$ , c-Si substrate, and we bonded the two together at 10 kN of force at 250 C for 1 hour, similar to Ref. [7] and Ref. [9].

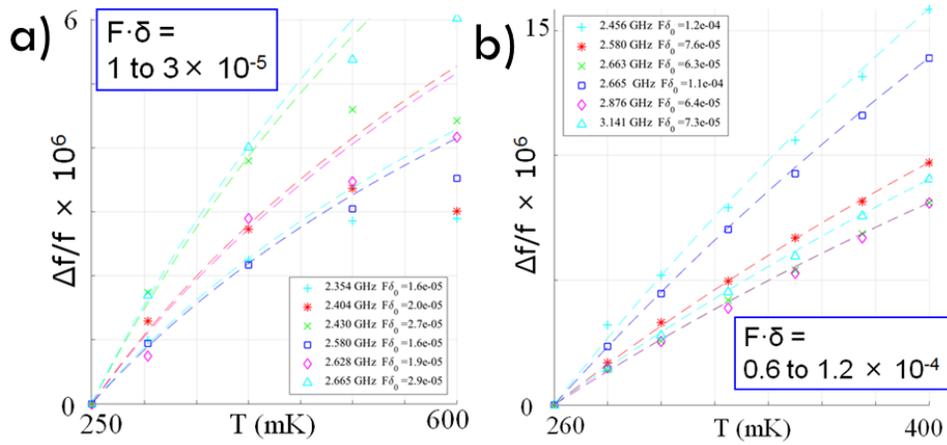
The bonded wafer stack was then sent out for commercial grinding of the Si handle of the SOI down from 500  $\mu\text{m}$  to tens of  $\mu\text{m}$ . The remaining Si in the handle was removed using a DRIE process, and the BOX was removed using BOE. Immediately, a 115 nm thick layer of Nb was sputtered on and etched back to form the CPW ground plane, CPW feedline, and the top plates and inductors of the LC resonators. Additionally, the metal loss test structures were etched in this step.  $\text{SiO}_2$  straps were then lifted off periodically along the length of the CPW feedline, and Nb straps were lifted off on top of the  $\text{SiO}_2$  straps to short the ground plane together at regular intervals along the length of the CPW readout. A trench was then etched between the ground planes on the exposed side of the c-Si down to the Au rim on the other side using a DRIE process. Gold was then electroplated between the two to short the two ground planes together.

### *2.2. Control RF test structure*

In order to determine if wafer bonding degraded the loss tangent in the c-Si layer, we also built an RF test structure using the SOI wafer and using a DRIE process to access the other side of the c-Si layer. This structure is not expected to be as robust as the wafer bonded structure because it results in membranes with thickness equal to the c-Si device layer thickness of 5  $\mu\text{m}$ . The best loss tangent,  $\tan \delta = 10^{-6}$ , was obtained from aluminium LC resonators made in a similar manner to the process we describe below [2]. Our control experiment device is shown in Fig. 2. It also had six LC resonators

and six metal loss test structures, with the LC resonators consisting of an inductor and two capacitors in series.

A BOE dip, to remove native oxide, was performed before sputtering 190 nm of Nb immediately. The ground plane, straps between the ground plane along the length of the CPW readout, and the inductor and two top plates of the parallel-plate capacitors were then patterned by etching the Nb. A 230 nm layer of SiO<sub>2</sub> was sputtered on top of the Nb, and another 300 nm of Nb was sputtered for the CPW feedline. The SiO<sub>2</sub> above the LC resonators and metal loss test structures was then removed to eliminate TLS from affecting fringing electric fields in the capacitors. Finally, the back plate for the two capacitors in the LC resonator circuit was fabricated by using a DRIE and lift-off pattern technique. The Si handle of the SOI wafer was etched through using a DRIE process, the BOX layer was removed using a hydrofluoric (HF) acid vapor phase etch, and the HF etch was followed by immediate sputtering of 300 nm of Nb and lift off to avoid allowing native oxide states under the Nb.



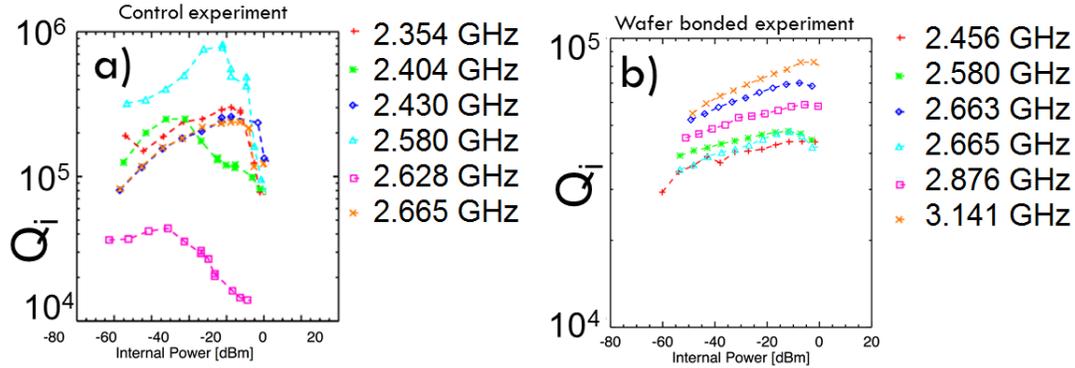
**Figure 3:** Normalized frequency shift vs. temperature data. a) The normalized frequency shift vs.  $T$  for the control experiment, RF test device. Points are data, and the lines are fits using Eq. (1). We find  $F \cdot \delta = (2.0 \pm 0.6) \times 10^{-5}$ , where  $F$  is the filling fraction of two level system (TLS) states and  $\delta$  is the loss tangent. b) The normalized frequency shift vs.  $T$  for the robust, wafer bonded RF test device. Points are data, and the lines are fits using Eq. (1). We find  $F \cdot \delta = (8 \pm 2) \times 10^{-5}$ .

### 3. Measurement and analysis

To evaluate the loss tangent of our devices, we cooled the devices down to temperatures between 250 mK and 600 mK, and the resonance frequency and internal quality factor,  $Q_i$ , were characterized. We use the relationship [6] governing frequency shift versus temperature to determine the value of  $F \cdot \delta$ , where  $F$  is TLS filling fraction:

$$\frac{f(T) - f(0)}{f(0)} = \frac{F\delta}{\pi} \left[ \text{Re}\Psi \left( \frac{1}{2} - \frac{\hbar\omega}{2j\pi k_B T} \right) - \log \frac{\hbar\omega}{2\pi k_B T} \right]. \quad (1)$$

Here,  $j$  is the imaginary constant,  $f(T)$  is the resonant frequency at temperature,  $T$ , and  $\omega = 2\pi \cdot f(0)$ . The values of  $F \cdot \delta$  found from this analysis are nearly independent of power and reflect the low power values relevant to mm-wave and sub-mm wave power expected in the LC resonators.



**Figure 4:** Internal quality factor,  $Q_i$ , versus internal power applied to readout the resonators. a)  $Q_i$  vs internal power for the control experiment, RF test device, which was fabricated with a DRIE process instead of a wafer bonding process. The  $Q_i$  values are consistently above  $10^5$  for almost all the resonators. b)  $Q_i$  vs internal power for the robust wafer bonded RF test device. The  $Q_i$  values are consistently above  $10^4$  for all the resonators. In both cases, we expect that the higher power regime ( $-40 \text{ dB} < \text{internal power} < 0 \text{ dB}$ ) is more relevant for improvement of capacitors in kinetic inductance detectors (KIDs) where readout power can be increased to saturate TLS states [10]. For low power (internal power  $< -40 \text{ dB}$ ), this regime reflects the power expected to be on the resonators when illuminated by mm-wave and sub-mm wave light based on the pW power levels expected. We expect this regime applies more to improving microstripline architecture like phased array antennae and spectrometers-on-a-chip.

In Fig. 3a, the normalized frequency shift,  $\Delta f/f = [f(T) - f(0)]/f(0)$ , versus  $T$  is shown for the control experiment and may be fit to Eq. (1) to obtain  $F \cdot \delta = (2.0 \pm 0.6) \times 10^{-5}$ , which is the best loss tangent among the two RF test structures measured. In Fig. 3b,  $\Delta f/f$  versus  $T$  and fits to Eq. (1) for the wafer bonded device are shown with resulting loss calculated to be  $F \cdot \delta = (8 \pm 2) \times 10^{-5}$ , about a factor of four higher in loss than the control experiment. Both measurements shown in Fig. 3 were taken with  $-20 \text{ dB}$  of internal power. In Fig. 4a and 4b, we show the measured internal quality factor,  $Q_i$ , as a function of internal power for the control experiment (Fig. 4a) and with the wafer bonded device (Fig. 4b). As expected the higher loss in the wafer bonded device corresponds to lower  $Q_i$  in this device than in the control experiment.

The power dependence of  $Q_i$  is interesting when divided into two regimes, higher internal power ( $-40 \text{ dB} < P < 0$ ) and lower internal power ( $P < -40 \text{ dB}$ ). The higher internal power regime is more relevant for capacitors in KIDs, because we can apply higher readout power to operate in a more favorable, higher  $Q_i$  regime where TLS are saturated. In such a regime, we obtain estimated loss tangent ( $=1/Q_i$ ) of  $1\text{-}5 \times 10^{-5}$  in the wafer bonded test device and  $0.13\text{-}1.3 \times 10^{-6}$  in the control test device, significantly lower than that obtained from the frequency shift data because the high readout power saturates the TLS loss [10]. In contrast, the lower power regime resembles what we expect for mm and sub-mm wave operation. Such a comparison has been confirmed by comparing mm-wave and RF test devices in the MUSIC instrument, which is a microwave-KID instrument operating at mm-wave with additional diagnostic structures at RF. Indeed the pW optical power levels expected at mm-wave and sub-mm wave should correspond to low internal power. The loss tangents obtained from  $\Delta f/f$  versus  $T$  measurements and fitting to Eq. (1) correspond to the values of  $\tan \delta$  expected at low power, even when measured at higher internal power, because the frequency shift induced by TLS is nearly independent of power and reflects the value at low power levels [10].

Both devices exhibit lower  $\tan \delta$  than in sputtered  $\text{SiO}_2$  and  $\text{Si}_x\text{N}_y$ , which is typically in the range of  $10^{-3}$ . In Ref. [2], which closely resembles our control experiment, the low power  $\tan \delta$  reached four times lower than what we measured, at  $\tan \delta = 5 \times 10^{-6}$ . It is possible that our SOI wafers are of different quality than in those experiments. Another possibility is that we are affected by oxides of Nb, while

Ref. [2] used Al and had less or different thicknesses of oxide affecting performance. The wafer bonded devices are a factor of 4 worse than our control experiment. Here, the BCB layer may be close enough to the parallel-plate capacitors for the fringe electric fields to travel through the BCB and add loss and filling fraction of TLS in the wafer bonded device. In future work, we could confirm this idea by additional patterning steps using a DRIE to etch through the backside and remove the BCB from behind the resonators for proof of our conjecture. At higher power, Ref. [2] obtained  $\tan \delta = 10^{-6}$ , and our control experiment is again a factor of a few worse while our wafer bonded device is at least a factor of 10 lower in  $Q_i$ . The same reasons of different SOI quality or oxides, as in the low power regime, would apply here too, but we continue to try to deduce other reasons for reduced performance as well. Ultimately, our wafer bonded devices are more robust for applications than the DRIE-type structures and are a significant improvement over  $\text{SiO}_2$  and  $\text{Si}_x\text{N}_y$  for comparison. Finally, if we consider the loss in a-Si:H reported in Ref. [1],  $\tan \delta$  varies from  $4 \times 10^{-4}$  at lower electric field (low internal power) to  $3 \times 10^{-6}$  at higher electric field (higher internal power). Our control experiment devices have better loss at low power and better loss at high power if we can assume TLS states are saturated by readout power and  $\tan \delta = 1/Q_i$  holds. In contrast, the wafer bonded devices have about double the loss at low power as a-Si:H and a factor of 3-17 higher at higher power if TLS are saturated. We aim to confirm that we can produce such high quality a-Si:H in a future control experiment for comparison and aim to continue to improve our wafer bonding process.

#### 4. Conclusions

We have measured the loss tangent,  $\tan \delta$ , and internal quality factor,  $Q_i$ , for two test devices at RF frequencies between 2-4 GHz. One device used a wafer bonding technique to robustly produce superconducting Nb LC resonators on both sides of a c-Si device layer 5  $\mu\text{m}$  thick, while the other device, our control test device, built similar structures using a less robust method with a DRIE process to test if wafer bonding degraded the performance. We find that the performance based on  $\tan \delta$  and  $Q_i$  outperform traditional amorphous dielectrics like  $\text{SiO}_2$  and  $\text{Si}_x\text{N}_y$  in both cases, but the performance is reduced in the wafer bonded device compared to the control test device. The wafer bonded device outperforms a-Si:H, but the wafer bonded device does not. Future work will try to identify the extra loss in the wafer bonded device to improve the performance to meet the promise of low loss that c-Si offers for superconducting detectors.

#### Acknowledgements

The research was carried out at the Jet Propulsion Laboratory, California Institute of Technology, under a contract with the National Aeronautics and Space Administration. Copyright 2016 California Institute of Technology. U.S. Government sponsorship acknowledged.

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