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RECENT ADVANCES IN COMMERCIAL MEMORIES AND POTENTIAL CONTRIBUTION TO GN&C MINIATURIZATION

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The last few years have seen a surge in technology, device, and architecture introductions in commercial memories such as SDRAM and NAND driven by the explosion of handheld and portable electronics. Some of the resultant devices provide high density in very small and light packages, which may be possible to leverage for the miniaturization of future GN&C systems in addition to providing considerable memory capacity to enable advanced capabilities such as image-based navigation or adaptive/autonomous operations. We will show that these advanced SDRAM and NAND technologies are worth serious consideration for the next generation of GN&C needs by highlighting reliability and radiation effects results from some of these devices.

INTRODUCTION

A quick look at the very capable smart phones right in our own pockets today gives ready evidence that certain sectors of consumer electronic have experienced unprecedented growth in technology. SDRAM and NAND flash memories fall into those sectors. Older generations of these commercial memories already have flight heritage but the latest parts can offer significantly higher densities and data rates in very small packages. Properly implemented, they can be utilized in miniature space crafts, such as cubesats and smallsats, and advanced spacecraft and instrument technologies that need significant memory, such as flash LIDAR, high-rate RADAR, hyper spectral imaging, adaptive and autonomous systems, image-based optical navigation, and formation flying.

Current radiation hardened (>100krad) memories such as SRAM, FeRAM, and MRAM are limited in density to a few tens of Mb on both the volatile and non-volatile sides. Utilizing true rad-hard memories would require hundreds if not thousands of dice to reach the Terabit (Tb) density and (Gigabit-per-second) Gbps data rate necessary to support the aforementioned technologies. Therefore, the test and use of advanced commercial memories in spacecraft can provide significant advantages in mass, power, size and cost.

Initial radiation results from various sources have shown that the DDR3 DRAM (SDRAM) have good total ionizing dose (TID) performance with some candidates usable up to 350-400krad (Si).[1] NAND is also showing stable TID performance with technology shrink. For example, SLC NAND performs reasonably well until about 30-70krad (Si) for 25 and 32nm.[1] It will be very interesting to see how the 3D versions of

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NAND and SDRAM perform under radiation stress, and to see the impact of the architecture change. There are no data currently in the literature.

The positive initial radiation and reliability performance for new nodes of NAND and DDR3 DRAM suggests that they are worthy of serious consideration for bringing performance and density to miniaturizing GN&C systems especially for advanced spacecraft technologies.

NONVOLATILE NAND FLASH MEMORY

NAND flash is currently the highest density nonvolatile memory available, as shown in Figure 1, even at a time when many emerging memories such as MRAM, PRAM and RRAM are receiving much attention and development. These high densities are made possible by both advances in wafer technology node, multi-chip packages, and novel chip architectures. Planar NAND technology node has advanced through many technology nodes: 32nm, 25nm, 19nm, and now 16nm.

The maximum density per chip for NAND is 128Gb at the 1Xnm node planar geometry (see Figure 1 left).[2] With multichip packaging, 8 chips can be stacked to deliver 128GB of data storage per package.

Adoption of MLC architectures also increased density by storing multiple bits in a single cell. The MLC cells store 2 bits per cell by distinguishing 2^2=4 current levels while the TLC cells store 3 data bits in 2^3=8 current levels (see Figure 2). This increase in levels from 2 to 4 to 8 increases storage density at a cost in program speed, power consumption, error rate, reliability, and radiation performance. For high reliability applications, storing only 1 bit per cell can deliver better reliability. The trade-off between density and reliability can be determined based on application.

Another new NAND architecture development is the 3D NAND: a 3D device architecture utilizing strings of cylindrical vertical gates to create a true 3D array of memory cells on a single wafer. The advances result in high density, nonvolatile memory that can be used to store mission information at the source of data collection, at the processor, and at the radio transmission queue.

3D NAND is currently commercially available from only one vendor: Samsung. The newest version of 3D NAND is available in a complete solid state drive (SSD) format with 32 vertical device layers and TLC 3 data bits per cell. Other major NAND partnerships, such as Intel/Micron and SanDisk/Toshiba have all announced samplings of their 3D NAND. The industry appears to be supporting 3D NAND as the replacement for NAND beyond the 1Xnm node as showing in the roadmap on Figure 1 right.[3]

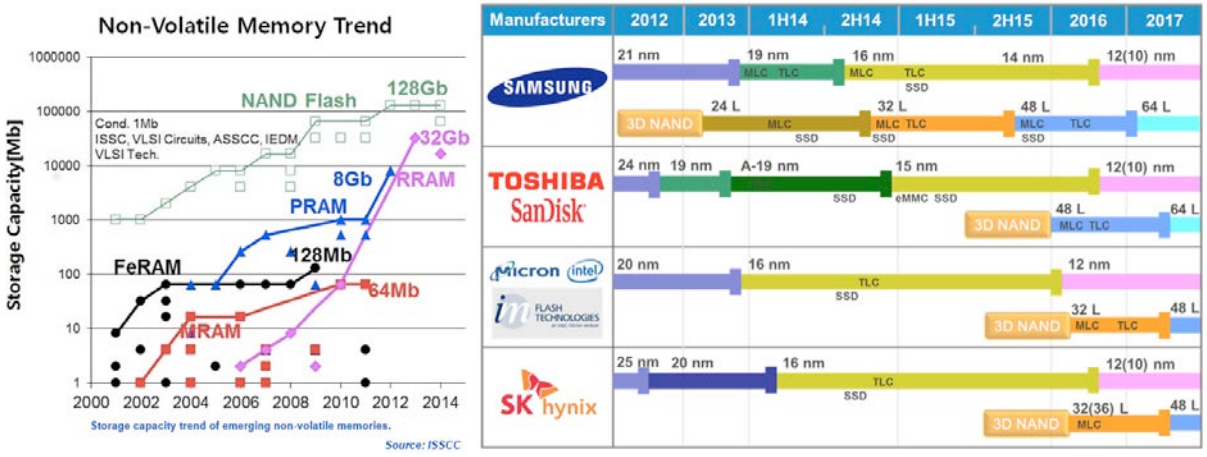

Figure 1. Technology Scaling for NAND[2] [3]

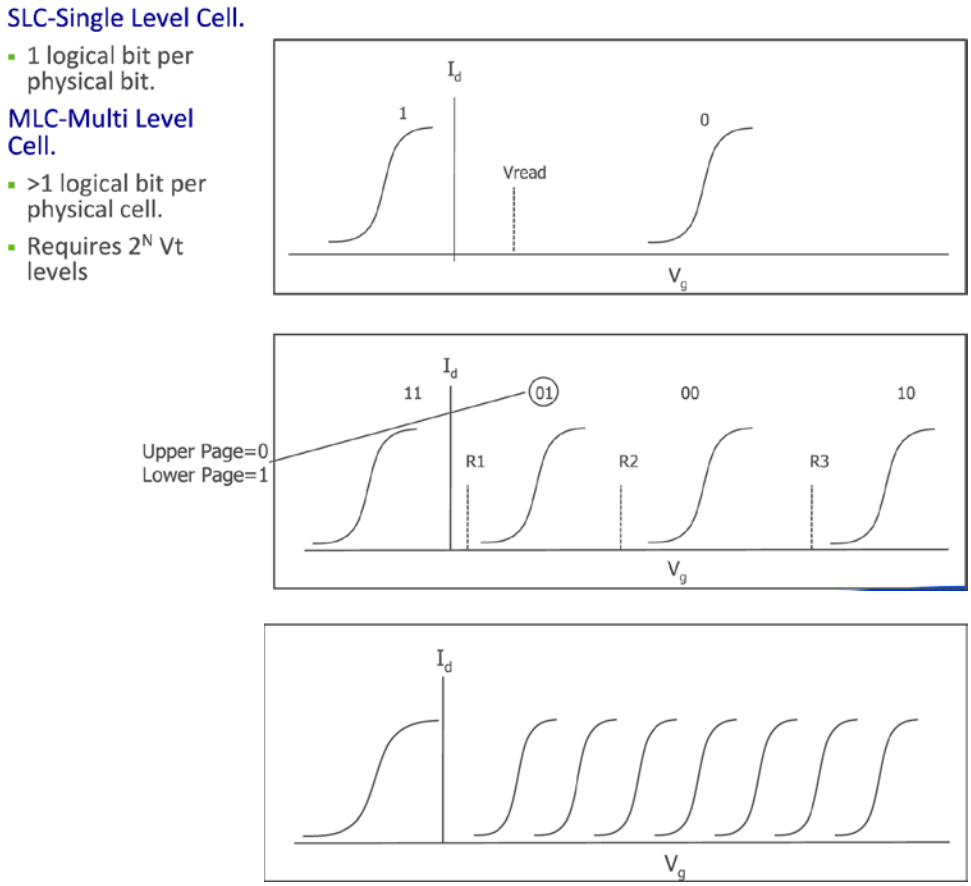

Figure 2. Multi Bit Per Cell Programming[4]

NAND Flash Use in Space

Commercial NAND flash has been utilized for data storage on space missions such as Mars Exploration Rover, Stardust, Genesis, and JUNO in a flash data card configuration.[5] The data card is capable of a total capacity of ~2Gb built with 128Mb NAND chips. Unfortunately, consumer semiconductor products tend to have limited production time. The 128Mb NAND chips are no longer in production due to being 1000x lower in density than the state of the art chips.

Over the last few years there has been a number of studies to investigate the suitability of more advanced Gb density NAND for space applications. In particular, high reliability and radiation tolerance are key factors in such assessment. We review here a few representative radiation and reliability studies for Gb density level NAND with SLC and MLC architecture. Some of the studies were conducted for the qualification of the NASA SMAP mission data storage card.

Radiation Impact on NAND Flash

A NAND flash chip contains not just the individual floating gate devices on which each bit of memory is stored, but also addressing transistors to select the rows of columns. Due to the high voltages required for program and erase of ~20V, these addressing transistors can be quite large with gate oxides in the tens of nm. In addition, these chips are designed for typical supply voltages of 5.0, 3.3, or 1.8V, so charge pumps are typically present on these chips. Further logic circuits can be present to manage the program and erase algorithm as well as read references. Past studies have shown that the memory arrays are fairly robust to total ionizing dose (TID) but the sensing circuits as well as the charge pumps are often the most vulnerable aspects of these chips and can determine ultimate TID robustness.[6]

NAND flash chips have been well characterized for their radiation tolerance for many generations now and the TID tolerance is typically better than the 10's of krads required for many space applications.[7] A study of 32-64Gb parts of 25-32nm node SLC, MLC and TLC NAND showed that radiation induced data retention error tend to be significantly higher for TLC parts over MLC parts and SLC parts (Figure 3).[8] The authors noted that the TLC parts had such high data retention errors at the initial read point that they were dropped out of the reading. Similarly, single event upset cross-sections were higher for TLC than MLC and SLC. As expected, when voltage levels are divided in smaller increments as shown in Figure 2 for TLC and MLC and as compared to SLC, margins for radiation tolerance decrease as a smaller amount of Vt shift is required for an error reading.

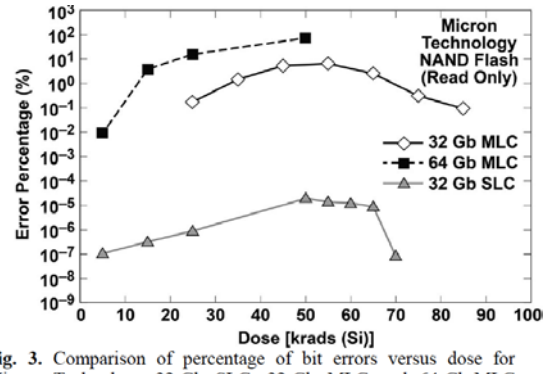

Fig. 3. Comparison of percentage of bit errors versus dose for Micron Technology 32-Gb SLC, 32-Gb MLC and 64-Gb-MLC NAND flash memories in Read Only mode.

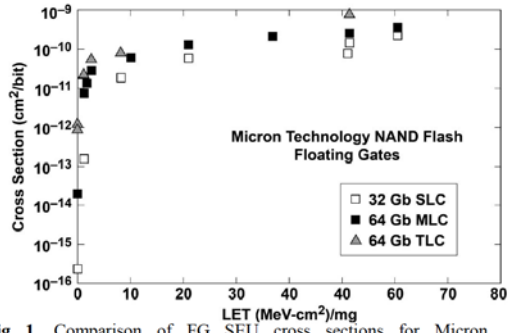

Fig. 1. Comparison of FG SEU cross sections for Micron Technology 64-Gb TLC, 64-Gb MLC and 32-Gb SLC NAND flash memories. The error bars are smaller than the size of the plotting symbols.

Figure 3. Total Ionizing Dose Induced Data Retention Error and Single Event Upset Cross Sections for TLC, MLC, and SLC NAND[7]

Another study of SLC and MLC NAND from the same manufacturer confirm data retention errors to be significantly higher for MLC.[9] Using 1% error as failure criteria, they found that MLC NAND fails for retention at a little over 20 krad(Si) while SLC NAND reaches 70 krad(Si). The choice of SLC versus MLC requires weighing error rate against data storage capacity and would be mission dependent. Low level bit error rates from the individual core cells can be correctable by implementing error correction code (ECC) in the readout. Functional failure, such as program and erase failures occurs at about 70 krad(Si) for both MLC and SLC NAND and are typically not reversible nor correctable.[9]

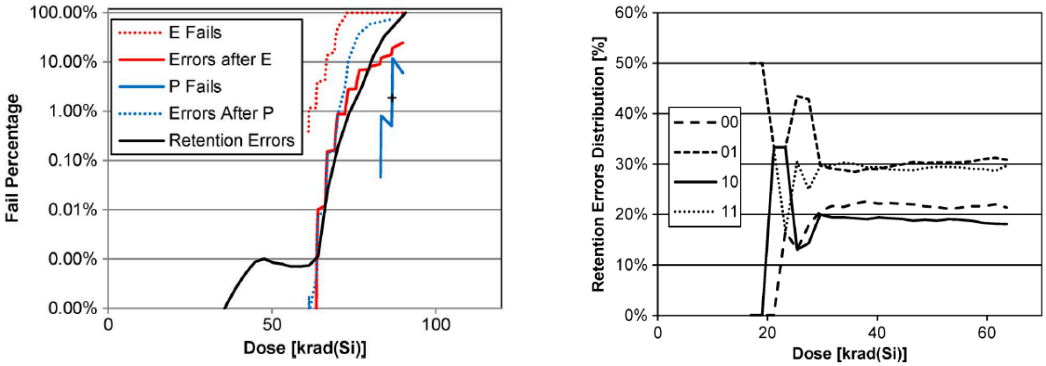

Figure 4. a) SLC Failure Type and MLC Pattern-based Failure as a Function of Total Ionizing Dose Under Low Duty Conditions (Mostly-Off)[9]

Interestingly, data pattern related retention failure (Figure 4) analysis showed that the "01" pattern was most susceptible to TID as the highest Vt state (see Figure 2) with the most amount of charge stored in the floating gate memory cell and the highest built-in field.[9] A third study using 16GB 32nm MLC NAND from another manufacturer demonstrated that the MLC part can be operated in SLC to gain additional TID robustness. Also, when SLC reference levels are chosen carefully, utilizing an understanding of the device physics, the TID tolerance of the memory core can be increased to almost 3x that of MLC levels beyond 200 krad(Si) (Figure 5).[10] But the authors also note that the periphery circuits may fail long before TID reaches 200 krad(Si).

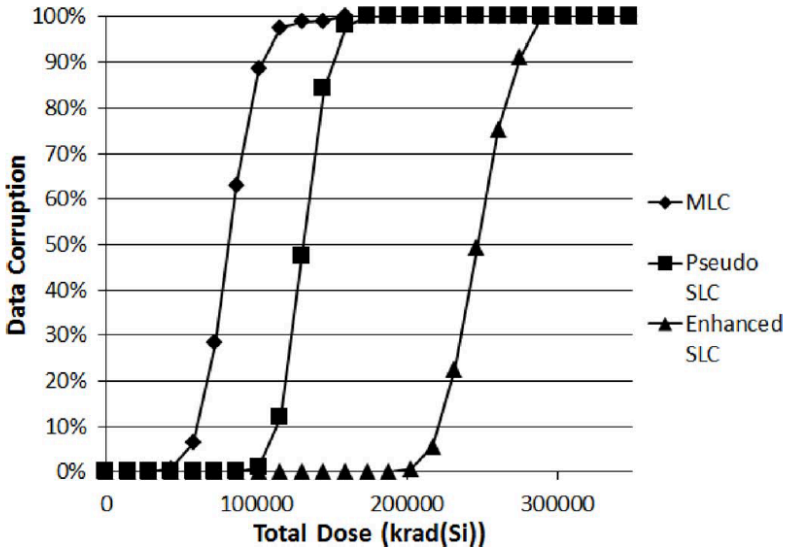

Figure 5. Data Retention Error for MLC NAND as Manufactured, Pseudo SLC (using R2 as V_{ref} see Figure 2) and enhanced SLC (using R1 as V_{ref} see Figure 2)[10]

Thus, NAND flash radiation results have consistently shown that MLC parts will have higher bit errors, which may be manageable by error correction, while SLC parts have more consistent TID tolerance. Also, both MLC and SLC NAND will be limited by the TID robustness of the periphery circuitry.

Reliability Impact on NAND Flash

The key reliability indicators specific to NAND flash are comprised of data retention, which is limited by the floating gate's ability to keep the injected charge for the rated lifetime, and program/erase cycling endurance. As memory array devices shrink, the margin for both data retention and endurance becomes reduced due to a smaller number of electrons injected to reach the same change in Vt. As seen in the radiation studies, MLC parts will have lower read margin throughout their entire lifetime, so error management is an important part of MLC NAND use.

The qualification for SMAP focused on the reducing the error rate of the population to reduce the ECC overhead required while still benefiting from the high storage density provided by the MLC architecture. Thus, the screening test utilized standard parametric testing for $I_{standby}$ at temperature, initial error rate at V_{cc} min and max, and initial bad blocks number. Parts were rejected if their initial error rates and initial bad blocks were high to avoid overwhelming the capabilities of the planned scheme.[11]

The qualification parts were subject to endurance cycling up to 5k at V_{cc} nominal, min and max and the results (Figure 6) show the change in bit error rates (BER) was manageable. In addition, the total BER do not nearly reach the proposed raw BER limit of 10^{-4} for the readout ECC. Combined TID and endurance effects were also tested by performing TID testing immediately after 5K endurance stress and showed no significant effect on bit error rate.[11]

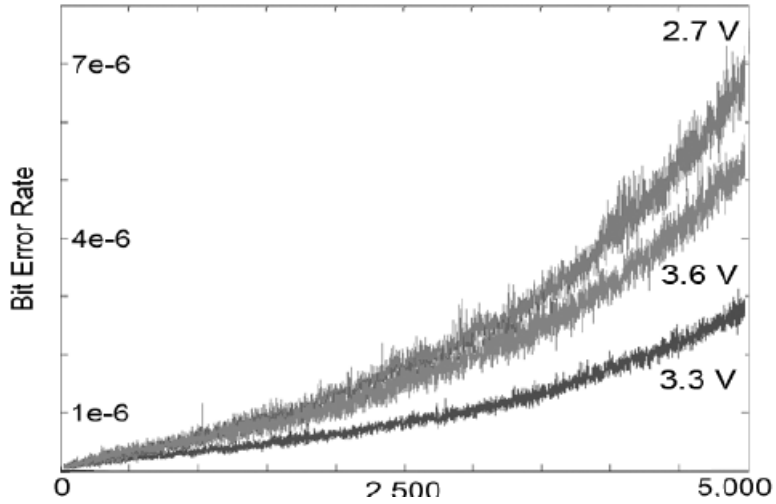

Figure 6. Bit Error rate for 32Gb MLC NAND as a Function of Endurance Stress and Vcc[11]

Overall, the SMAP MLC NAND qualification found that the BER to be quite stable and manageable and that there was little to no combined TID and endurance interactions.

VOLATILE DRAM MEMORY

On the working memory side, 25nm DDR3 DRAM is now mainstream and DDR4 is on the market (Figure 7). Each generation of DDR doubles transfer rate and theoretical bandwidth while reducing power consumption per bit by reducing operating voltage. Mobile oriented LPDDRx versions have seen rapid performance improvement in the past 5 years such that bandwidths are now comparable to standard DDR versions.[13]

Similar to NAND, 3D technology has been announced for DRAM as well, with a processor base controlling a stack of DRAM chips within a single package resulting in at least a 2 order of magnitude increase in bandwidth. There are two competing implementations: the Hybrid Memory Cube from Micron utilizing TSV to connect the processor to the DRAMs and the High Bandwidth Memory from an AMD-Hynix-UMC collaboration utilizing an interposer to connect between the processor and the DRAMs. The 3D DRAMs are designed to address the power consumption, noise and bandwidth limitations of the PCB board by utilizing tools such as 3D integration, system in package, multi-chip module, through silicon via, stacked silicon interconnect and wide-IO configurations.[12]

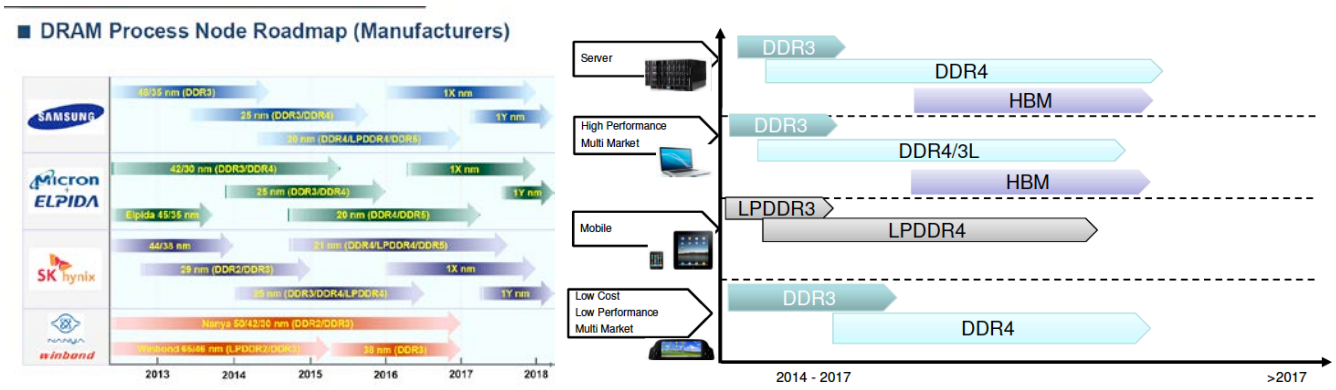

Figure 7. DRAM Technology Roadmap[10] and DRAM Application Roadmap[13]

Interestingly, the high aspect ratio, deep trench technology pioneered for DRAM is now bearing fruit in other 3D devices. Figure 8 left shows a 75:1 aspect ratio 70nm node deep trench DRAM cross section released by Infineon in 2004, when the deep trench process was only 25% of the DRAM market. Fast forward to 10 years later, aspect ratios of ~100:1 are now standard with Intel's 30nm eDRAM process (Figure 8 center) and the 3D NAND from Samsung (Figure 8 right). It is exciting to see solutions developed for one technology can surprisingly be used to enable other technologies.

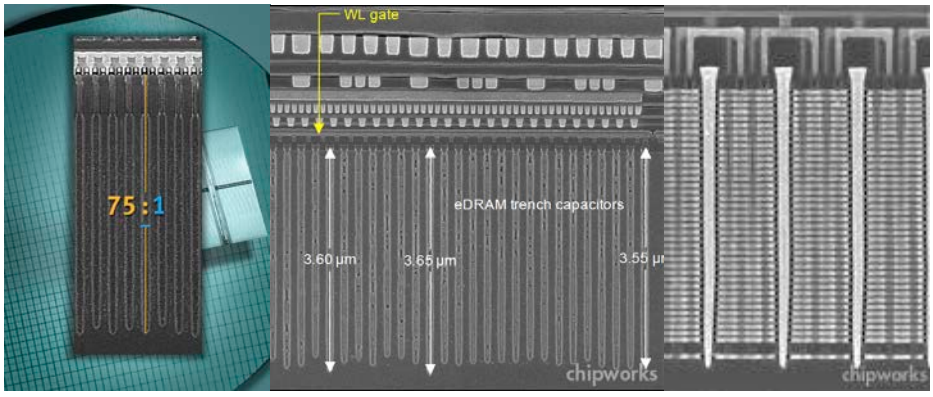

Figure 8. Infineon 70nm Node Trench Capacitor 2007,[14] Intel 30nm Node eDRAM Trench Capacitor 2014,[15] Samsung 2nd Generation 3D NAND 2014[16] (left to right)

DRAM Use in Space

SDRAM or DRAM is typically used as working scratchpad memory for a processor or as a data recorder for flight data or payload. SDRAM were also used in data storage since the early deep space mission Cassini, but NAND based solid state storage are more common now due to lower power consumption and nonvolatility. DRAM use as working memory has increased with high computation space technologies and higher performance processors. Currently the workhorse BAE Rad750 processor can be paired with DDR3 DRAM for a significant reduction in power, mass and volume as compared to rad hard SRAM especially in more moderate radiation environments.

Radiation Impact on DRAM

A 2010 presentation from NASA's Goddard Space Flight Center reviewed SDRAM testing and concluded that SDRAM is indeed quite TID hard for a commercial part with a consistent >50krad(Si) tolerance. Three characteristics were noted to be important. First, error burst can occur during intermittent events, such as solar radiation flares, which may overwhelm error correction (Figure 9). On-orbit results show >90% of errors can occur in a few events or a few "bad" days and cause over all error rate to jump a couple of orders of magnitude. Secondly, single event effects can cause lost of functionality or destructive failures, which must be managed. Finally, application specific testing is important to have meaningful results for mitigation planning within a manageable amount of critical testing time.[17]

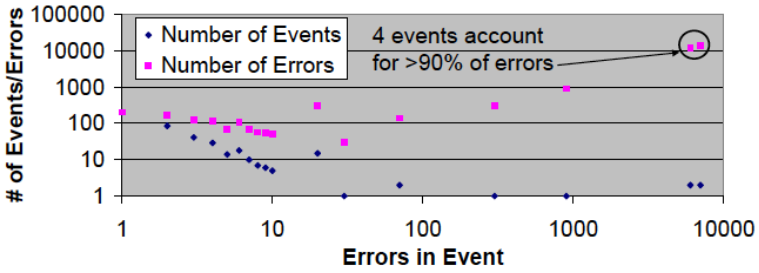

Figure 9. SDRAM On-Orbit Error Occurrence and Propagation [17]

Subsequent studies on DDR2 DRAM from Micron and Samsung showed that they are consistently hard to TID. Parametric failures occur at 150-300 krad(Si) and only for biased parts. Functional failures occur even later at 900 krad to 1Mrad(Si). Additional TID studies with pre-aged chips, having ~10 years of aging by temperature acceleration, show vey minor enhancement of TID damage with aging and no parametric or functional failure impact.[18]

A more recent study of 512Mb DDR3 DRAM (in 4 chip or 8 chip packages for a total of 2Gb or 4Gb) show that total ionizing dose tolerance can be as high as 400 krad but is very vendor dependent.[1] Figure 10 left top shows that in TID studies NAND flash can start to experience errors within a few krad of exposure especially when the data is in static storage mode. The vertical lines show functional failure, which occurs anywhere between 30-70krad. In comparison DDR3 DRAM seems to show significantly better TID hardness. The Samsung parts show no errors up to 200krad (Figure 10 right top) and Micron parts show errors can increase quickly after about 70krad (Figure 10 right bottom). DDR3 DRAM from Hynix (no figure) actually showed no errors up to 400krad, and all DRAM chips studied were functional after 400krad (Si) of gamma radiation.

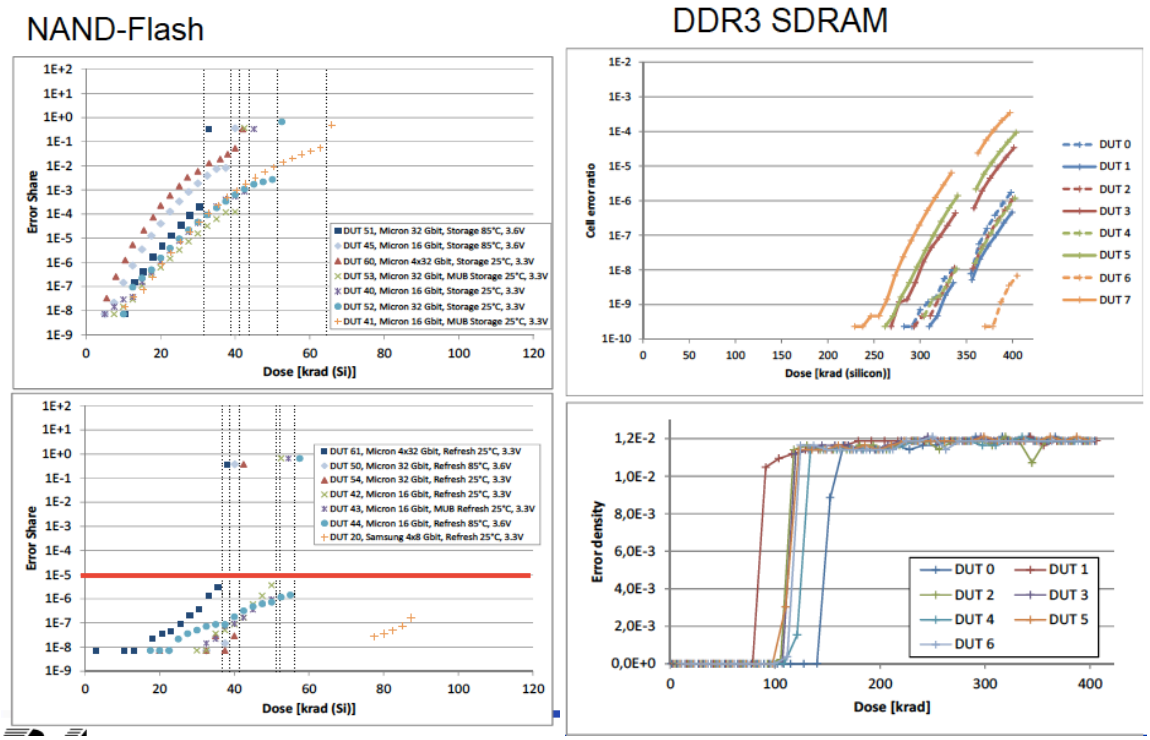

Figure 10. TIC Results: (left top) NAND Error Rate Static, (left bottom) NAND Error Rate Active Write, (right top) DDR3 DRAM Samsung, (right bottom) DDR3 Micron [1]

Reliability of DRAM

A separate reliability study was conducted for DDR3 DRAM from all three vendors: Micron, Samsung and Hynix in 2015.[19] Over 50 parts were first verified with I_{DD} testing, then data retention was characterized by adjusting refresh interval and operating temperature between 35°C and 75°C. Shmoo testing with the March X write/read steps examined input voltage versus operating frequency capabilities for the chips. The test dice performed very well The I_{DD} were all within nominal range or with minor differences. The Shmoo testing showed a 0.2V window for the Samsung and Micron devices and a >0.3V window for the Hynix devices. The data retention show the expected 2x change in retention time for every 10°C change that agrees with past literature.

All dice behaved within expected tolerance with the exception of one out of 17 Samsung dice which had a slightly higher than normal background number of bad bits at 35°C. This is again an expected result. Given the high production volumes, only 0.1%-1.0% of parts should have any detectable shift from nominal behavior.[19]

Figure 11. DDR3 Reliability (L) Shmoo plot for and (R) Retention Error vs. Refresh Period for a Hynix Die[19]

SUMMARY

More recent generations of commercial NAND and DRAM have been tested by various source and the radiation and reliability results support these parts to be suitable for some spacecraft applications requiring high density data storage or high rate processor memory. Data storage density of up to 128GB per package with MLC is available in NAND and DRAM densities of up to 4Gb are available with DDR3 data rates. Total ionizing dose radiation results shows that the NAND memory cells are more susceptible to radiation induced errors than the DRAM memory cell. NAND periphery circuitry is also more susceptible to radiation due to higher internal operating voltages. However, both exhibit enough radiation tolerance to be suitable for moderate missions which only require a few tens of krad(Si) of maximum exposure. MLC and TLC NAND have higher error rates and lower radiation margin than SLC and will require error correction support. For NAND and DDR3 DRAM, intrinsic reliability of these mass produced parts appear to be good and testing did not reveal significant failures due to the combined effects of aging and total ionizing dose.

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