Reliability Characterization of TaO_X-based Commercial ReRAM in Combination with Radiation

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***Abstract*— We present reliability data combined with total dose gamma radiation for one of the first commercially available resistive memory devices. These Tantalum Oxide (TaO_X)-based resistive memory chips demonstrate operation in dynamic program and erase testing up to ~130 Krad(Si) of ^{60}Co gamma dose. In static and unbiased conditions, the stored data in the memory cells were able to withstand up to 50Mrad(Si) of exposure. The access circuitry, though, seemed less robust to gamma radiation and was able to operate only up to a total dose of 3Mrad(Si). Post exposure reliability as indicated by endurance, cycling error rate, and data retention tests showed no detectable impact from the combination with prior gamma irradiation. Overall, the total dose radiation tolerance of the commercial TaOx-based resistive memory chip appears to be higher than flash memory chips and in agreement with prior tests conducted with single cell resistive memories.**

Keywords—ReRAM; resistive memory; radiation tolerance; data retention; flash memory; total ionizing dose

I. Introduction

Interest in resistive switching random access memory, or resistive memory (ReRAM), has grown significantly in the past decade such that it is now recognized as one of the most promising candidates of many emerging memory technologies [1][2]. ReRAM offers the promise of fast switching, high endurance, CMOS-compatibility, cost-effective integration, and scaling below 10nm. In addition, the inherent robustness of the cell and the possibility of supply-voltage level program and erase (set and reset) make this type of memory especially interesting for high reliability, low power and extreme environment applications. The low voltage program and erase offers a path to eliminate the charge pumps which are key, known-contributors to radiation induced failures [5][6] and chip power consumption [3][4] for flash memories. Low voltage program and erase also eliminates the need for high voltage, thick-oxide, row and column select transistors.

Tantalum oxide (TaO_x)-based ReRAM have been reported by many research and development sources to have excellent non-volatile memory benchmark behavior, such as cycling endurance and data retention. For example, cycling endurance of up to 10^{12} program and erase cycles has been reported [7]. Better than 10 year data retention at 85°C has been demonstrated with a retention activation energy of 1.1-1.23 eV reported [8], and the base cell itself has been known to operate at temperatures as high as 200°C [9].

TaOx-based ReRAM single cells have also demonstrated excellent total ionizing dose radiation tolerance with up to 2.5 Mrad(Si) ^{60}Co exposure under static testing conditions [10][11]. Of the two resistance states, the high resistance state is reported to be more sensitive to total dose. Other variables that impact radiation resistance include the device dimensions and the thickness of the oxide [12]. More recent work indicates that it may be possible to cause a TaOx based ReRAM to switch from a high resistance state to lower resistance state with a ^{60}Co gamma radiation exposure of ~ MRad(CaF_2), a 10KeV X-ray dose of ~3MRad(SiO2) [13], or with high dose rates of 20 MeV electrons in the 10^8 rad/s(Si) range [14]. These levels of total ionizing radiation dose tolerance are notably better than those typically reported for flash memories [15][16][17].

The encouraging radiation tolerance reported thus far for TaOx ReRAM suggests promise for its space applications, but the behavior under radiation is far from understood. The increased availability of commercial TaOx based ReRAM now offers an opportunity to study total ionization dose effects with ~500,000 of submicron sized, mass-produced ReRAM devices per chip. This type of study can produce more quantitative data to add to the body of knowledge that is primarily based on single cell research devices. In addition, studying a commercial chip also offers the opportunity to look at array effects as well as peripheral circuitry effects that are known to be important in understanding the radiation tolerance of complex memory chips.

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Furthermore, it is reasonable to assume that the write and read algorithms in this commercial chip are well optimized for key metrics such as endurance and data retention and may contain complex sequences of varying voltages, pulse widths, and feedback loops that are typical of commercial non-volatile memories. Therefore, our study results can offer a useful reference point of how a commercially optimized ReRAM product compares to research ReRAM single cells and commercial NAND products.

II. Experimental

A. Device

The Panasonic MN101L is an 8-bit microcontroller with 64kB of embedded tantalum oxide-based non-volatile ReRAM produced with an 180nm node CMOS baseline [18]. The basic construction of this tantalum oxide-based ReRAM has been previously reported [8] and its reliability shown to be similar or better than standard flash NAND in terms of endurance, retention and operation temperature [19]. The 64kB of ReRAM is comprised of 62kB of memory rated for 10^3 program cycles and a small group of 2kB of memory designated for data area and rated separately for 10^5 program cycles.

The memory cell has a physical dimension of approximately 400nm per side. Transmission electron microscopic and energy dispersive X-ray spectroscopic analysis confirm that the top electrode is comprised of ~30nm of Iridium, connected to a $Ta_2O_{5-\delta}/TaO_x$ memory element measuring ~30nm total thickness. The bottom electrode is Tantalum Nitride [19].

Previous tests have shown that pre-stressing with endurance stress well beyond the datasheet limit may be needed to ensure measurable error rates in other tests given the size of the array. For example, it was found that even after 5000 write cycles (5x data sheet limit for most of the chip capacity), the resulting error rate was difficult to measure with accelerated data retention test at 150°C due to very low? error rate. Therefore, the chips used in this experiment all were subject to at least 20K cycles of program endurance stress prior to radiation testing.

B. Testing Conditions

All bits in the 64 kB resistive memory embedded in the microcontrollers are programmed with data and read using the Panasonic AM13L-STK2 evaluation board. The high resistance state (HRS) has a designation of logic “0” while the low resistance state (LRS) is designated as logic “1.” The test code and evaluation boards have been previously used in endurance testing and accelerated data retention tests and resulted in error rates and activation energies consistent with literature [19]. The errors reported here are as output by the chip.

Radiation exposure testing with a ^{60}Co (1.332 and 1.173MeV gamma) radiation source was conducted at NASA’s Jet Propulsion Laboratory Total Ionizing Dose laboratory. All tests and irradiation were performed at room temperature unless otherwise specified. The dose rates were confirmed with air ion chamber measurement.

Three different tests were conducted to ascertain the impact of gamma radiation on the ReRAM chips: dynamic test, static test, and post irradiation reliability.

III. Results and Discussions

A. Dynamic Test Results

Dynamic testing was conducted by exposing two ReRAM chips at a dose rate of 38rad (Si)/sec. The chips were powered and set to continuously program cycling with repeating “10” pattern on all bits during the irradiation. The test pattern is read after each program, and the program pattern is reversed with each subsequent programming to ensure that all bits are subjected to programming stress at each cycle. Each programming cycle took ~ 2seconds during which ~76rad(Si) of gamma radiation is received. The other components of the evaluation board are shielded by lead during test but may still have experienced up to 10% of the total radiation dose as unintentional exposure.

DUT8 stopped executing program cycling after receiving ~ 225krad(Si) of gamma ray exposure. The last program cycle for DUT8 saw only multi-bit errors concentrated in 13 words of 16 bits. The bits were read as all “1”s where there should have been alternating “01”s in almost all cases. The error signature and the concentration of errors in very few words suggest that the CMOS peripheral circuitry failed during read. Memory cell failures would tend to appear as single bit flips in random addresses with no correlation to word sizes.

The sensitivity of the CMOS peripheral circuit seen here is consistent with a previous study by

Chen et al. who also found the CMOS elements for this commercial ReRAM chip to be much more susceptible to heavy ion and pulsed-laser induced bit upsets than the memory array [21]. The most sensitive circuits reported by Chen et al. to pulsed-laser stress were the sense amplifier circuits used in the read operation.

DUT8 was able to recover its function after power cycling, but did not show any single bit errors for study. So, we chose a chip with more baseline single bit errors, created by 50,000 pre-irradiation endurance cycling stress, for the second test. DUT11 exhibited a good number of single bit errors during program cycling before, during and after irradiation as shown in Figure 1. The single bit error occurance was more frequent during irradiation than for either the pre or post irradition tests. Error ocurrence during irradiation was especially high after ~115Krad(Si) of gamma radiation dose. The chip stopped writing and reading after ~130Krad(Si) dose.

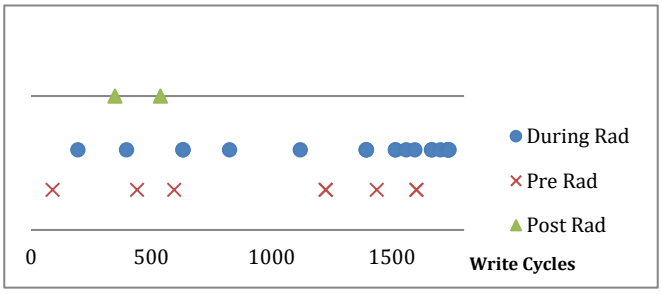

Figure 1. Single Bit Dynamic Errors

The failure signature suggests failures in the write circuits this time. At the fourth to last

0 20 40 60 80 100 120 140 Krad(Si) dose

programming cycle, 72 words showed a data pattern that is consistent with missed or failed programming. At the last program cycle, 96 words showed the same failure signature and read as if the programming was missed or failed. The chip stopped operating at the write portion of the next cycle. The entire failure pattern suggests that DUT11 failed in its write circuitry while DUT8 most likely failed during read. In both cases, the ultimate limitor was the periphery circuitry.

We also note that the type of single bit errors measured during irradiation exhibited different weighting of the 0's read as 1's (HRS➔LRS bit flips) type versus 1's read as 0's (LRS➔HRS bit flips) as compared to without irradiation. Of the single bit errors measured during irradiation, DUT8 showed 99% of error are the HRS➔LRS type while DUT 11 showed 86% of errors are the HRS➔LRS type. By comparison, we found only 62%-78% of the errors are of the HRS➔LRS type for typical program cycling errors without irradiation for both chips. Therefore, there appears to be a greater prevalence for HRS➔LRS bit flips during gamma radiation exposure.

The higher prevalence for HRS➔LRS bit flips during TID is in agreement with prior reports showing HRS to be more susceptible to TID radiation than LRS [12][13]. It is possible that ionizing radiation can form oxygen vacancies in the TaOx to affect some bridging of pre-existing partial conduction filaments thus generating new conduction paths. The mechanism for the generation of oxygen vacancies has been suggested to be due to current generation and localized heating from electron-hole pair generation in the built-in electric field of the oxygen vacancies and anions in the device [10]. Holes generated by ionizing radiation have also been proposed as the cause of O^{-2} anion formation, which interferes with the high resistive state [20]. These are both possible mechanisms that are consistent with existing percolation models for the set/reset and switching of ReRAM indicating that charge or ion movement is important in the set/reset process [22].

B. *Static Test Results*

A first static irradiation test was conducted with two chips (DUT5 and DUT7) preprogrammed with a "10" pattern and exposed at a dose rate of 38 rad (Si)/sec. The leads were floating and the chips were power off. After irradiation to predetermined doses, the chips were read to determine data retention. DUT 5 saw zero read error when the pattern was read after an exposure of 225krad(Si). DUT 7, a chip with significantly higher endurance stress prior to irradiation (see Table 1), saw a single bit flipped from HRS "0" to LRS "1" at 375krad(Si) of exposure.

Lead shielding was used to protect other chips on the board during irradiation, but these other components still failed sooner than the ReRAM chip in gamma radiation. As a result, a new fixture

Die # and test type (static or dynamic)	Total Ionizing Dose, rad(Si)	Prog. cycles before TID test	Prog. cycles before retention	Pre irradiation error rate	Post irradiation error rate
DUT 4	0	*	360000	2.29E-08	*
DUT 5 (s)	2.25E+05			1.31E-08	*
	1.97E+06	20000	50000	*	2.02E-09
DUT 7 (s)	3.75E+05	360000	380000	7.26E-08	3.94E-08
DUT 8 (d)	2.25E+05	20000		2.72E-09	1.71E-09
DUT 8 (s)	1.97E+06	42884	50000	1.71E-09	3.21E-09
DUT 11(d)	1.30E+05	50000	70000	6.27E-09	2.52E-09
DUT 12	0	*	50000	5.04E-09	*
DUT 31 (s)	5.30E+07	20000	*	4.44E-09	6.05E-09
DUT 36 (s)	6.00E+06	20000	*	5.14E-09	1.26E-08

*not applicable or not available

Table 1. Devices Tested and Error Rates

was developed to removably plug the memory chip into the evaluation board and ensure that static irradiation can be conducted on the chips without affecting? the evaluation board.

A second set of static irradiation tests were conducted on 9 ReRAM chips at a higher dose rate of 242 rad/s (Si). The chips were irradiated with power off and die leads grounded or floating. All 9 chips were subject to 20,000 program endurance stress cycles before the irradiation. Irradiation was conducted during two runs with reading but no refresh between runs. The first run consisted of 4 sets of chips exposed to doses of 0, 30krad, 300krad, and 3Mrad(Si) correspondingly. Each set was comprised of 2-3 chips. No errors were found post irradiation so the chips were subjected to a second run where 3 chips each received an additional 3Mrad or 50Mrad doses for a total static exposure range of 30krad to 53Mrad(Si). Post irradiation readings showed that both the stored data in memory and the CMOS chip circuitry remained without error after total gamma exposures of 30krad(Si) to 6Mrad(Si). No difference was observed in the radiation response between leads grounded and leads floating configurations, although previous work with single cells have shown terminals floating may be more susceptible to total ionizing dose [20].

There were three chips subjected to doses >50 (Si) dose and after exposure, 2 out of 3 chips were unreadable through the evaluation board. The remainder chip, DUT31, accumulated a total of 53Mrad(Si) of gamma radiation through 2 runs, and showed zero bit errors (bit flips) post irradiation.

The gamma radiation tolerance for these ReRAM chips appears to be even higher than prior results such as those by McLain et al. for ^{60}Co source irradiation effects on single cell TaOx-based ReRAM [13]. They reported that a "switching threshold" dose of ~1Mrad(Si) can cause resistance switch from HRS to LRS for cells grounded during ^{60}Co irradiation. We found the commercial chip may be able to resist bit flips at doses as high as 53Mrad(Si). This apparent resistance to bit flips can be attributed to additional process and algorithm development and also may suggest presence of internal error correction.

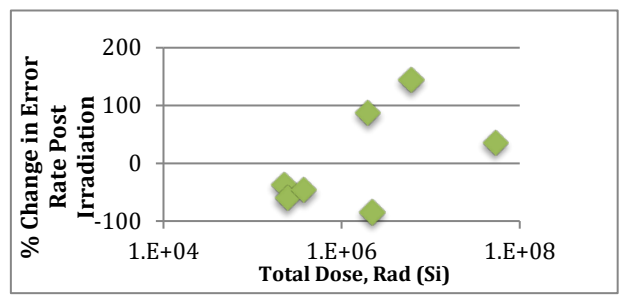

Figure 2. Post-irradiation Error Rate Change

C. *Post-irradiation Reliability*

Post-irradiation reliability testing was conducted to identify combined impact of gamma radiation on endurance and retention performation. Endurance testing was conducted for 6 irradiated samples with doses up to 53Mrad(Si) and pre-endurance stress cycle as indicated in Table 1. The post-irradiation endurance cycling test showed typical error rates in the 10^{-8} to 10^{-9} range (Table 1) and can be either higher or lower than pre-irradiation error rates at lower gamma doses (Figure 2). In general, post irradiation error rate see to increase with dose rate, but the effect is very weak and variations. No strong

combined impact from the radiation exposure was detected in the error rates during endurance testing. This finding is similar to those of McLain et al. who found that gamma radiation induced bit flips to present no permanent damage in TaOx ReRAM single devices [13].

Gamma radiation impact to data retention capabilities was studied with four irradiated chips with up to 2.2Mrad(Si) of total exposure (DUTs 5, 7, 8, &11), along with two control chips (DUTs 4 & 12). The two control chips were chosen to cover the initial endurance stress range of the irradiated chips (see Table 1). Previous studies have shown endurance stress to be an important factor in determining data retention.

The 6 chips were each programmed with a complete array of "01" pattern then subjected to an accelerated data retention test at 150°C for up to 500+ hours. The chips were removed from heat at regular intervals and the data read 10x without rewrite at room temperature before the chips were returned to the oven.

The resulting data retention performance is shown in Figure 3 as a plot of the read error rate versus total time at 150°C. We found no statistically significant difference between data retention error rates for the control versus the irradiated DUTs.

No residual impact from the gamma irradiation, up to 2.2Mrad(Si) of exposure, was detected in the accelerated data retention test results.

The data retention bit errors (bit flips) measured were almost exclusively of the LRS➔HRS type. This type of retention error is consistent with existing percolation models for conduction through filaments of oxygen vacancies [24]. The filament can be broken by diffusion of oxygen vacancies that has the same activation energy range as those previously reported in data retention tests for these TaOx ReRAMs [19][23]. Gamma radiation does not seem to impact ReRAM data retention after disturbed or flipped bits? are re-programmed, just as it does not seem to impact dynamic error rates within the range studied.

IV. Conclusion

An initial total ionizing dose characterization of a commercial TaO_X-based ReRAM chip, with ~500,000 accessible bit cells per die, was conducted. The ReRAM chip shows more than 50Mrad(Si) of ^{60}Co radiation tolerance during static storage. Dynamic active operation is demonstrated with some increase in error rate up to 130krad(Si). Both static storage and dynamic operations with gamma radiation appear to be limited by the periphery circuitry and not the memory cells.

The 50Mrad(Si) of static radiation tolerance is significantly better than commercial flash based nonvolatile memory. The data here can be recognized as initial evidence that the absence of charge pumps and high voltage column and row select transistors can indeed lead to a more radiation tolerant memory product based on ReRAM.

Overall, the ReRAM chip appears to be quite robust to ^{60}Co total ionizing dose. Statically and dynamically exposed chips show no evidence of post-exposure combined impact in dynamic operational error rate or in accelerated data retention. The ReRAM data retention errors are dominated by LRS to HRS errors that were previously identified by activation energy with oxygen vacancy diffusion [19], while ionizing radiation can cause HRS to LRS errors during dynamic operation attributed to oxygen vacancy generation.

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