



# **2.5/3D Daisy Chain Reliability Evaluation**

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## Objectives and Products

The objective of this task is to evaluate thermal cycle behavior of advanced 2.5/3D electronics — commercial-off-the-shelf (COTS) — packages of different configurations assembled onto printed circuit boards (PCBs). Three key approaches were considered for evaluation. The first approach focused on the through-mold via (TMV™) technology at assembly level. The second approach focused on evaluation of 2.5D (also known as, System in Package (SiP)) in fine pitch ball grid array (FPGA). The third approach focused on evaluation of through-silicone-via (TSV) technologies. This report presents the test results for TMV™ and SiP packaging technologies and reliability, and it also provides lessons learned on quality assurance methods.

Specifically, the report presents the test matrix for various 3D TMV™ packaging assembly configurations and reliability characterizations performed under two accelerated thermal cycling (ATC) and accelerated thermal shock cycling (ATSC) conditions. The ATC and ATSC were performed in the range of  $-55^{\circ}\text{C}$  to  $125^{\circ}\text{C}$  and  $-100^{\circ}\text{C}$  to  $125^{\circ}\text{C}$ , respectively. The report also includes assembly of a SiP— a 60-mm fine-pitch ball-grid array (FPGA) interposer with an IC at the center and six chip-scale package (CSP) daisy chains at the periphery—with package assembly characterizations. After assembly, the daisy chains were subjected to ATCs in the range of  $-40^{\circ}\text{C}$  to  $125^{\circ}\text{C}$  for reliability evaluation. Finally, for both TMV™ and SiP packaging configurations, characterizations results by X-ray, optical imaging, and daisy-chain resistance evaluations were also presented.

**Key Words:** Ball grid array, BGA, through-mold via (TMV™), 3D stack, fine pitch BGA, FPBGA, solder joint reliability, thermal cycle, thermal shock cycle, SiP, system in package

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## 1.0 2.5/3D PACKAGING TRENDS

Stack packaging—more than Moore’s Law—has now been widely implemented for use to increase the capabilities of commercial electronics because of increasing cost and limitation of die fabrication with finer features [1–3]. Moore’s Law, stating that the number of transistors on a given chip will double every two years (or even shorter, 18 months), has been substantiated by package implementations throughout the past several decades. The exponential growth for die density has allowed computers and electronic communication devices to become cheaper and more powerful simultaneously. However, the die density growth has slowed significantly. Recently, Intel’s chief technologist stated that “Moore’s Law is about integration for lower cost-per-function, and it continues — but we don’t get to pick the technology that enables it anymore.” This is alluding to new materials, devices, and packaging methods.

In more recent years, the increase in package density has further helped this miniaturization trend by using area arrays for interconnection rather than conventional packaging such as quad flat package (QFP) with peripheral leads [4–8]. A package with an array of solder bumps is commonly referred to as ball-grid array (BGA) technology. If the package dimension is nearly that of the integrated circuit (IC) itself, then the technology is called chip-scale package (CSP). A wafer-level package (WLP) uses wafers with added protective coating, and subsequent singulation provides dense components with standard packaging attributes such as ease of testing and handling.

Combination of these packages and integrated circuits (ICs) inside a single package is called system in package (SiP) whereas system on chip (SoC) integrates functional chips onto the same die. SiP has been around since the 1980s in the form of multi-chip modules. Rather than put chips on a printed circuit board, they can be combined into the same package to lower cost or to shorten distances that electrical signals have to travel. Connections historically have been through wire bonds; however, now connections are in the form of flip-chip die or other FPGA packages.

While SiP saw limited adoption in its earliest forms, much work has been done on improving this concept recently with 2.5D and 3D ICs, as well as package-on-package and flip-chips. As stated by Rao Tummala and his co-authors [9], “Heterogeneous integration is necessary to continue the growth of electronics post Moore’s Law.” Electronic packaging integration enables better and denser electronics by device-level integrations in 2D, 2.5D, and 3D using current approaches in organic laminates, Si interposers, and wafer fan-out and embedding as well next generation using glass packaging. There are several key drivers for these changes:

Figure 1 illustrates 2.5/3D stack packaging trends from those that are in the development stage to those that are now mainstream. The 2.5D covers segmented die with passive TSV interposer within package or active interposer with packages, also known as system in a package (SiP). The 3D packaging consists of stacking of packaged devices called package-on-package (PoP), including through-mold via (TMV™), and stacking of die within a package called package-in-package (PiP) or stacked wire-bonded die (primarily memory) [10–11]. The PoP and PiP technologies are used today using conventional stacking or other unique technologies such as TMV™ and through-silicon via (TSV) as well as through-edge-interconnection processes for device stacking within packages [12–15].

In general, commercial off-the-shelf (COTS) conventional or 3D packages using plastic-encapsulated materials (PEMs) have two key limitations:

1. Due to the major differences in design and construction, COTS packages have a smaller operating temperature range and are typically more frail and susceptible to moisture absorption compared to high-performance devices; therefore, the standard test practices used to ensure that high-performance devices are robust and highly reliable often cannot be applied to PEM packages.
2. Users of 3D COTS packages have little visibility into commercial manufacturers’ proprietary design, materials, die traceability, and production processes and procedures, whereas controls are in place for the high-reliability systems.

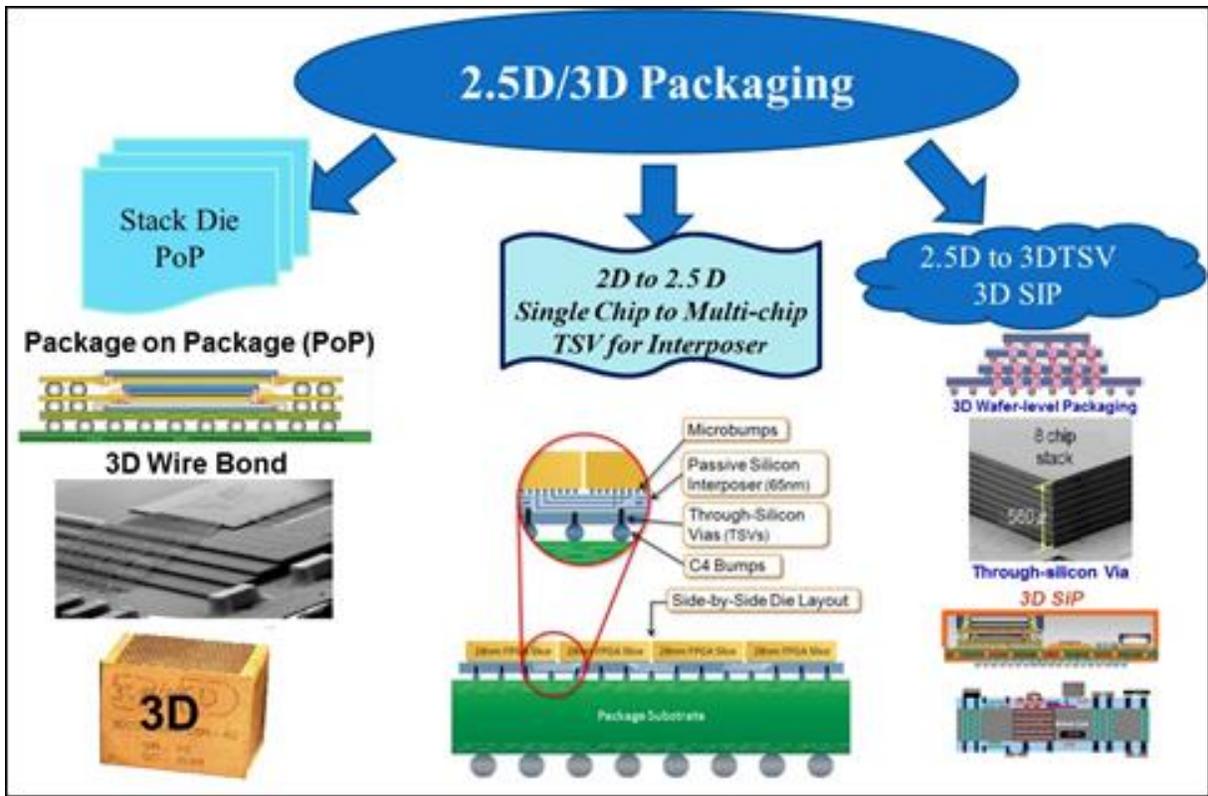


Figure 1. 2.5/3D stack packaging technology roadmap with maturity status.

(C4 is controlled collapsible chip connector.)

A literature survey indicates that most prominent failures for COTS 3D packages and assemblies are due to warpages (individual or system) for plastic packages. For the stack ceramic package and TMV™, failures due to via are of concern. In addition, both plastic and ceramic stack packages are required to meet minimum shock and vibration requirements per Mil-STD-883. Separation of stack layers, if not adhesively bonded together, during shock is another failure mechanism that needs to be considered. In addition, very limited techniques are available to ensure quality and reliability of 2.5/3D stack packaging and assemblies.

Figure 2 presents the two experimental methods —TMV™ and SiP— presented in this report, which first presents evaluation performed on TMV™ stack packaging-assembly reliability, followed by the second approach that is focused on evaluation of SiP assembly reliability on a fine-pitch ball-grid array (FPBGA). The first section presents test matrix design, 3D TMV™ package daisy-chain patterns, detailed design of the PCB, test vehicle (TV) design, and detailed information with representative images of assemblies. It also includes the three approaches of 3D stack assembly— pre-stacking package or stacking during PCB assembly with using either flux/solder or solder/solder. The interim thermal cycle test results to as many as 200 cycles (–55°C /125°C) or thermal shock cycles (–100°C /125°C) were also presented. The second section presents assembly, characterization, and reliability test results for SiP assembly configuration with a centrally located (ICs surrounded by eight chip-scale packages (CSPs). The thermal cycle test results performed to 200 cycles (–40°C /125°C) were also presented.

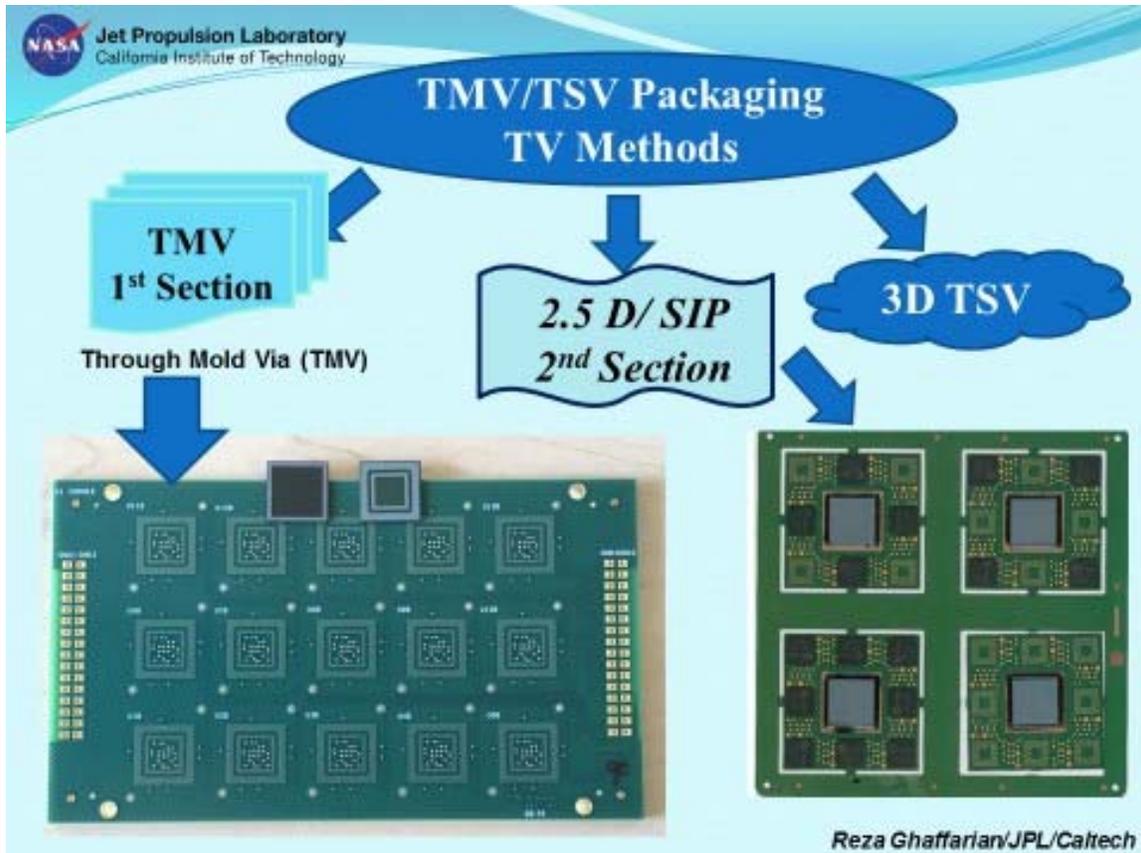


Figure 2. Two test vehicles for thermal cycling: (1) 3D TMV™ packages (on the left) and (2) SiP on a fine-pitch ball-grid array (FPBGA) interposer on the right.

## 2.0 3D TMV™ TEST METHODS

### 2.1 Test Matrix

To determine assembly reliability of 3D TMV™ stack packaging technologies, packages with daisy chain patterns are required for detecting solder joint failure by electrical daisy-chain failure. Industry has designed the stack package with a daisy-chain pattern to match those of PCBs for drop test evaluation, but it is also used for thermal cycle reliability characterization. Figure 3 shows the board design with daisy-chain pattern, and how traces are routed to the edge of the board for daisy chain monitoring. The design facilitates the 3D TMV™ solder-joint reliability characterization since most package styles from a manufacturer do not come in daisy-chain form. This was the most effective approach to meet the task objectives with limited funds to design a unique costly test vehicle for evaluation. The daisy-chain resistive loops were monitored during thermal cycling during cycling or at intervals to allow detection of an open loop due to solder-joint opens at either package level (bottom or top) of 3D TMV™ assemblies.

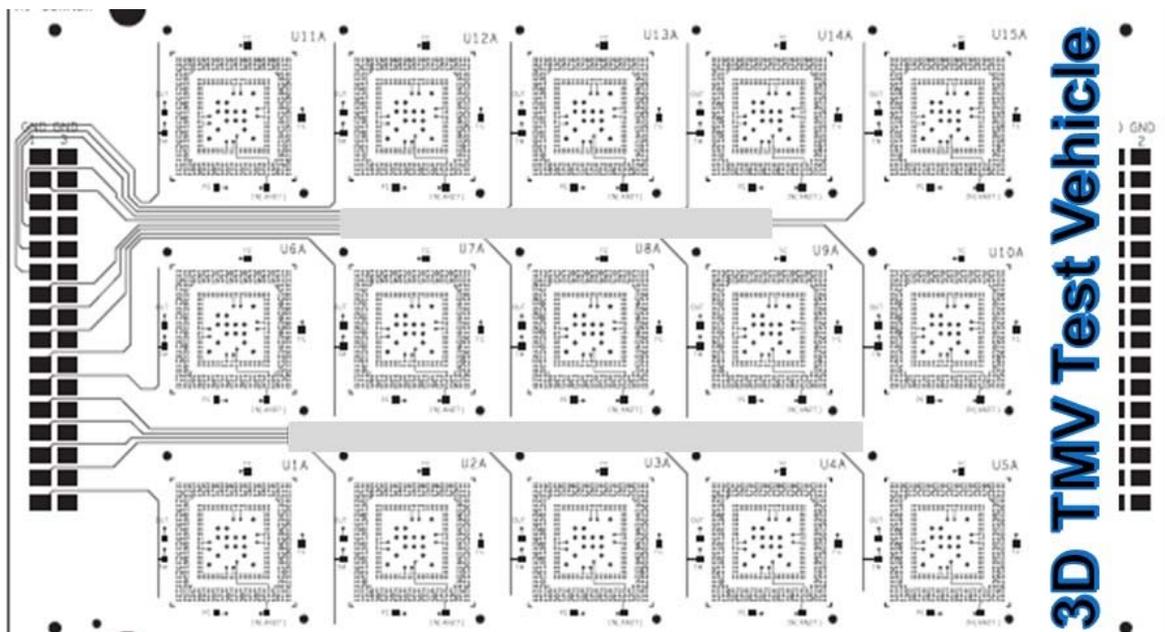


Figure 3. The 3D TMV™ daisy-chain patterns.

A design of experiment (DOE) technique was used to cover four methods of packaging stack assemblies and their effect on the stack packaging assembly reliability. The four methods are

1. The top package was only fluxed and placed onto the lower package, which was placed on tin-lead (SnPb) solder paste. Then, both were reflowed with 15 TMV™ packages (see Figure 4).
2. Solder paste was placed onto the bottom package pads prior to placement of the top package, which was placed on SnPb solder paste of the PCB pad patterns. Then, the TMV™ stacks were reflowed.
3. Pre-stack package as a unit with SnPb solder and then assemble the stack package onto PCB with SnPb solder paste. Then, the pre-stack reflowed with 9 TMV packages (see Figure 5).
4. The top 14 mm package had 200 lead-free tin-silver-copper (95% Sn, 1% Ag, and 0.5% Cu), SAC105) balls with 0.5-mm pitch. The lower through mold via 14 mm package had 620 lead-free SAC125 balls with 0.4-mm pitch.

The pre-stack approach is possibly the most applicable approach for high-reliability applications even though this approach is the most costly and time consuming. Reliability is another key aspect that should be considered in the overall final selection of the 3D TMV™ selection for an application. The PCB material was FR-4 glass-reinforced epoxy laminate material with 93-mil (2.4-mm) thickness with microvia in pad and electroless nickel immersion gold (ENEPIG) surface finish.



Figure 4. Fifteen 3D TMV™ daisy-chain packages assembled with SnPb solder either at the package or PCB level.

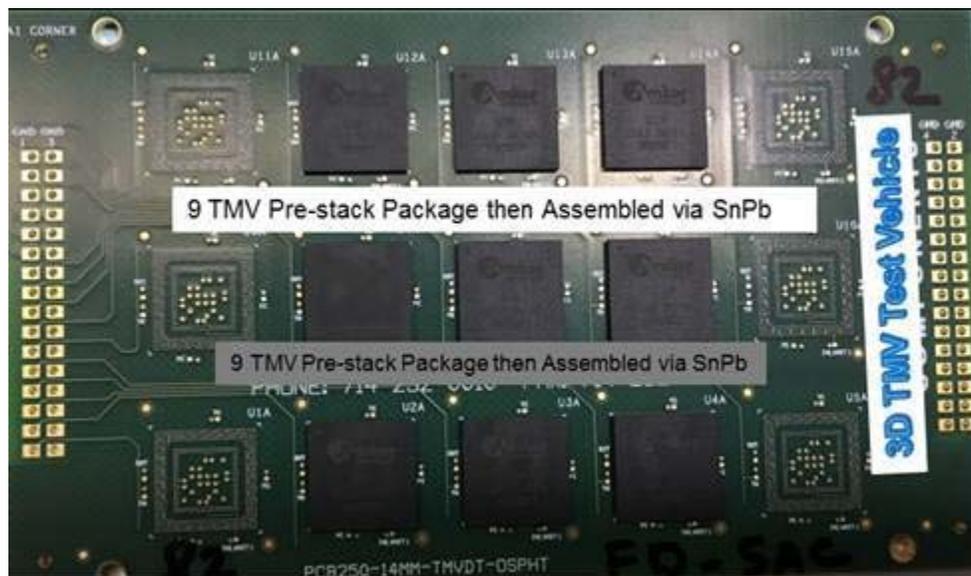
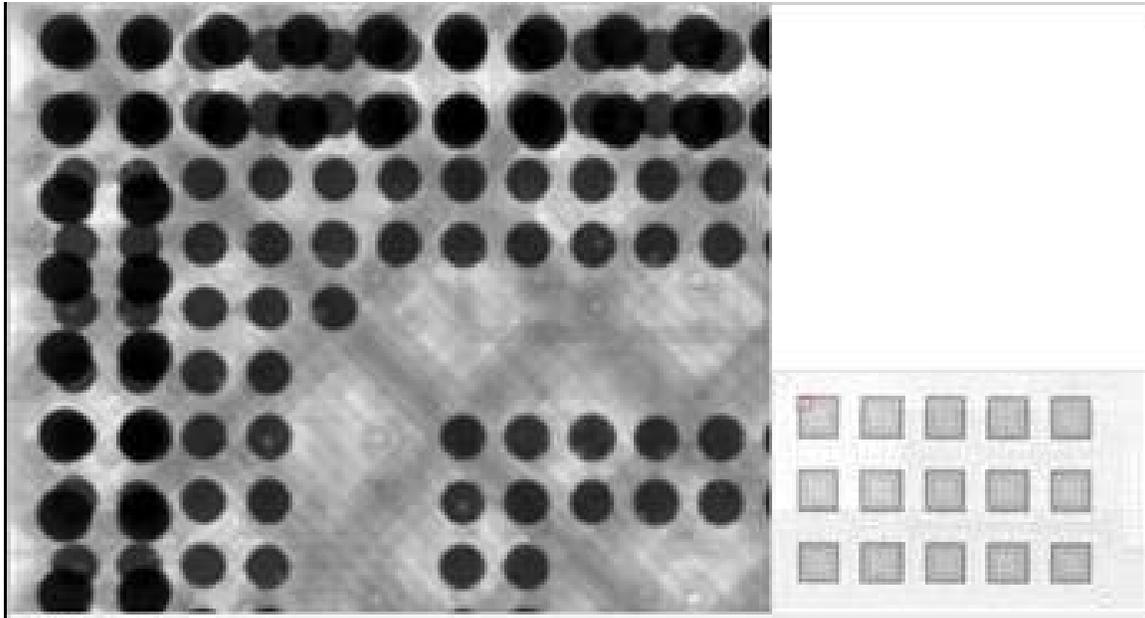


Figure 5. Nine 3D TMV daisy-chain packages pre-stacked and then assembled onto PCB with SnPb solder.

## 2.2 TMV™ under Thermal Cycles

After successful assembly of a large number of 3D TMV™ test vehicles, they were subjected to two different thermal cycling profiles: accelerated thermal cycle (ATC) or accelerated thermal shock cycles (ATSC). The ATC profile was in the range of  $-55^{\circ}\text{C}$  to  $125^{\circ}\text{C}$  using a single chamber for cycling, and the ATSC profile was in the range of  $-100^{\circ}\text{C}$  to  $125^{\circ}\text{C}$  using a single chamber with direct liquid-nitrogen exposure built for highly accelerated life testing. In addition to daisy-chain resistance evaluation monitoring, X-ray and optical images were performed and presented for the as-assembled and after-thermal-cycles test vehicles. Figures 6 and 7 present representative X-ray and optical images, respectively, after thermal cycling.



**Figure 6. X-ray image of corner of 3D TMV™ package showing packages configuration that is peripherally populated and shows a limited number of voids.**

Optical inspection (Figure 7) was difficult to perform on the test vehicles, and even though such inspections partially revealed the condition of solder joints at the bottom package, it was difficult to determine the condition of solder joints at the top of the package. After thermal cycling, individual packages were cut out for optical and scanning electron microscopy (SEM) evaluations. Figure 8 shows representative optical and SEM evaluation of a cut-out package after cycles. For this package, both bottom and top packages were assembled with SnPb solder paste.

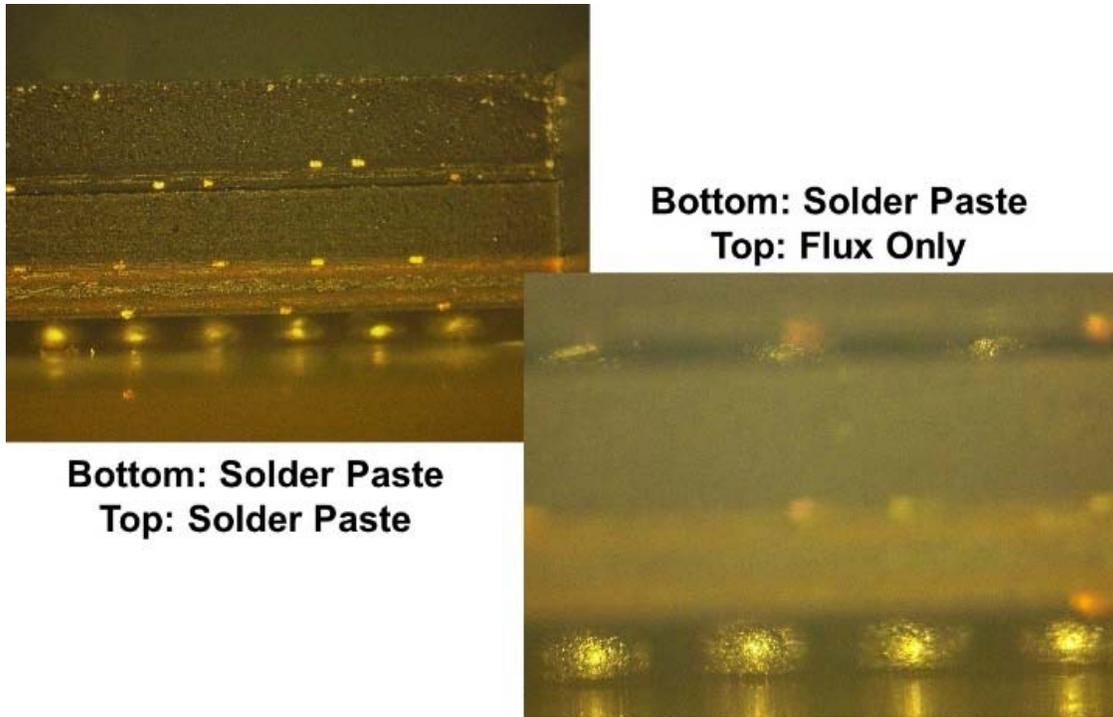


Figure 7. Optical photomicrographs of two 3D TMV™ daisy-chain packages, one with using solder paste on both top and bottom and the other using solder paste only on the bottom of the FPBGA.

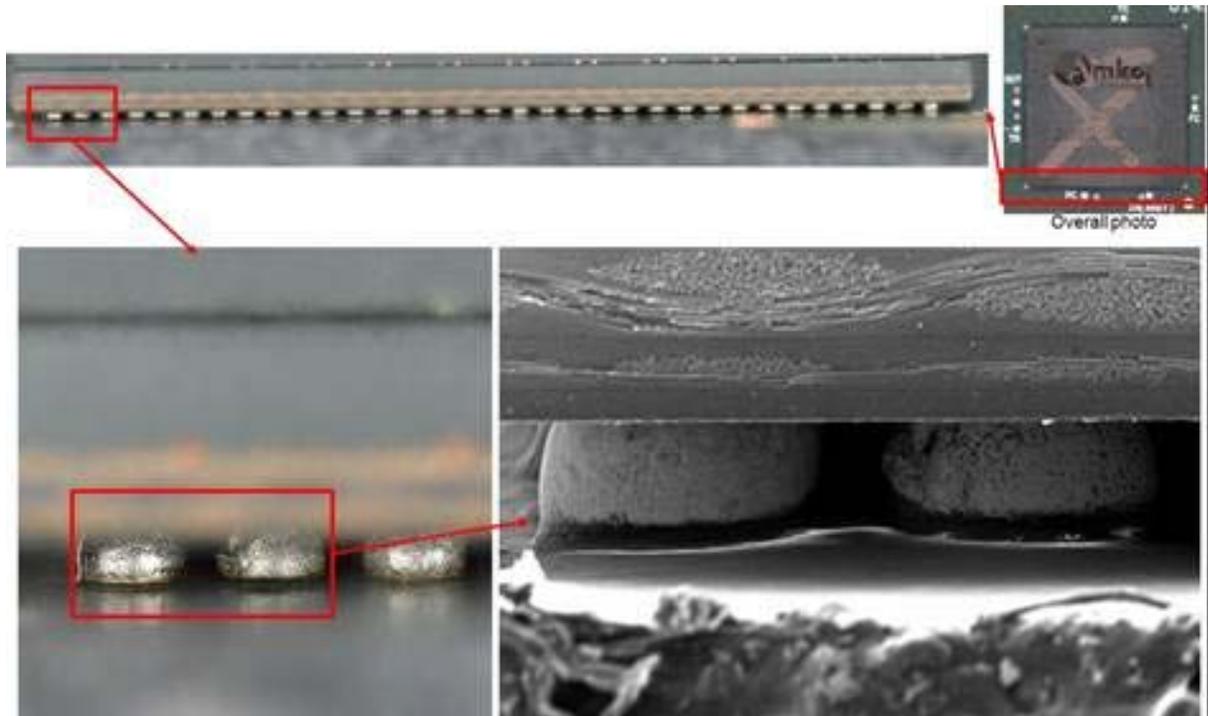


Figure 8. Optical images (lower left and top left, corresponding SEM image (lower right), and overall image (top right) of a 3D TMV™ package assembled with SnPb solder paste at both the bottom and top sites.

### 3.0 System-in-Package Evaluation

#### 3.1 Introduction

In the second experimental approach, system-in-package (SiP) test vehicles (TVs) were configured with centrally located integrated circuits (ICs) surrounded by chip scale packages (CSPs). As shown in Figure 9, the TV design allowed for as many as eight chip-scale packages (CSPs) to be attached around the perimeter of each SiP interposer.

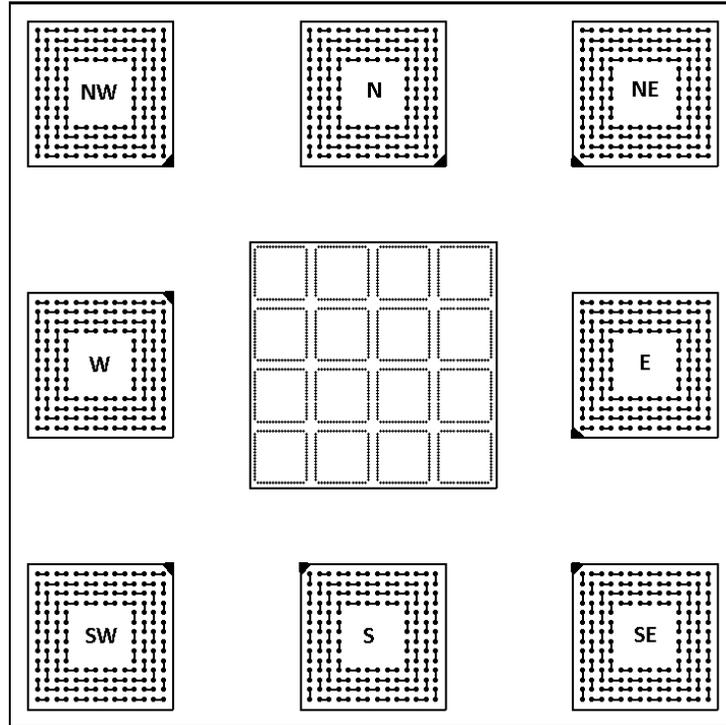


Figure 9. Drawing showing top view of SiP substrate with eight CSP memory placements and centrally located IC placement. (Directional reference designators are shown.).

The ICs and CSPs of the SiP were assembled onto a fine-pitch ball-grid array (FPBGA) interposer for subsequent assembly in a hybrid configuration (Figure 10). The CSPs with SnPb represent high-reliability applications, and SAC305 solder balls represent applications fabricated in compliance with the European Union Restriction of Hazardous Substances (RoHS, Directive 2002/95/EC) were each assembled onto an interposer partially or fully covering its CSP site. Mixed package assembly becomes a challenging task, and the assemblies were characterized to determine if their quality was acceptable. They were characterized for solder-joint quality by X-ray and for warpage level by Shadow Moiré analysis. Those assemblies that were considered to have acceptable quality and warpage were then subjected to thermal cycling for solder-joint reliability evaluation. Thermal cycling was performed between  $-40^{\circ}\text{C}$  and  $125^{\circ}\text{C}$  with 15-minute dwells at the temperature extremes. Transition rates between the temperature extremes were less than  $10^{\circ}\text{C}$  per minute resulting in a total cycle time of 74 minutes. Evaluation results from assembly to solder-joint characterizations are presented in the following sections.

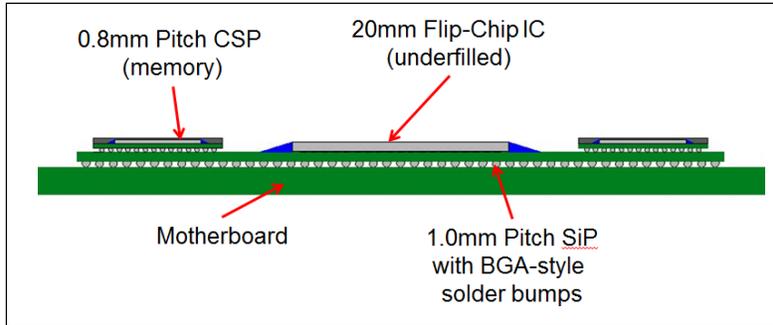


Figure 10. Drawing showing cross-sectional view of SiP test vehicle.

### 3.2 SiP Test Vehicles

Figure 11 shows a SiP interposer with the IC assembled at the center and the CSP pattern surrounding the IC before the CSPs are assembled.

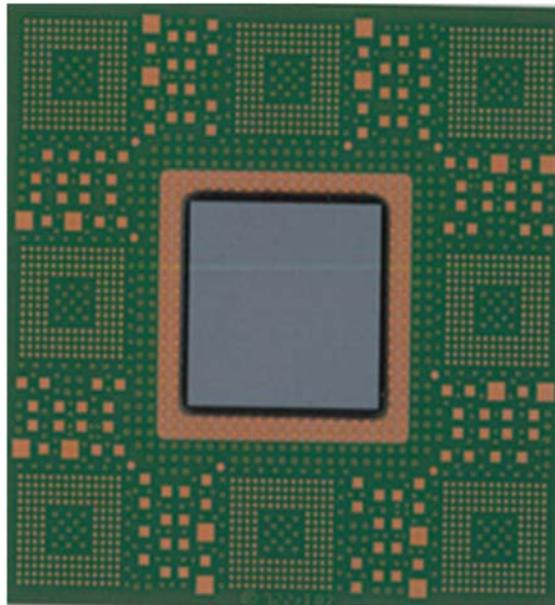


Figure 11. Top view of SiP substrate with flip-chip IC.

The interposer constructed using daisy-chain pattern to complement the IC and CSP daisy-chain patterns. The CSP simulates a memory package and had 160 solder balls ChipArray® ball-grid array (CABGA 160), 12 × 12 mm, with SAC305 balls as shown in Figure 12.

The interposer FBGA of the SiP body was designed and assembled by the package supplier. The FPBGA package was populated with 3364 area array balls with 1.0-mm pitch. The interposer had an area of 60 × 60 mm<sup>2</sup> with 0.9-mm thickness utilizing blind and buried via structures providing signal conduction between the layers (see Figure 13).

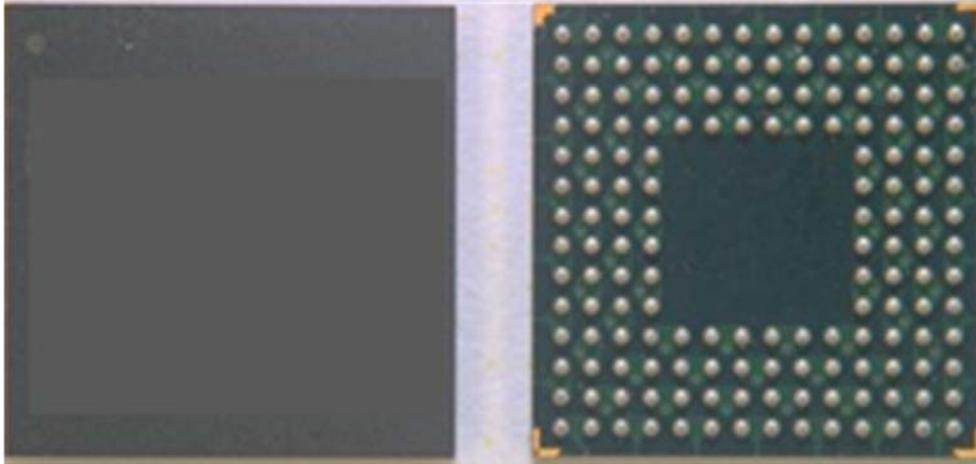


Figure 12 Top and bottom view of a ChipArray® ball-grid array (CABGA) with 160 solder balls.

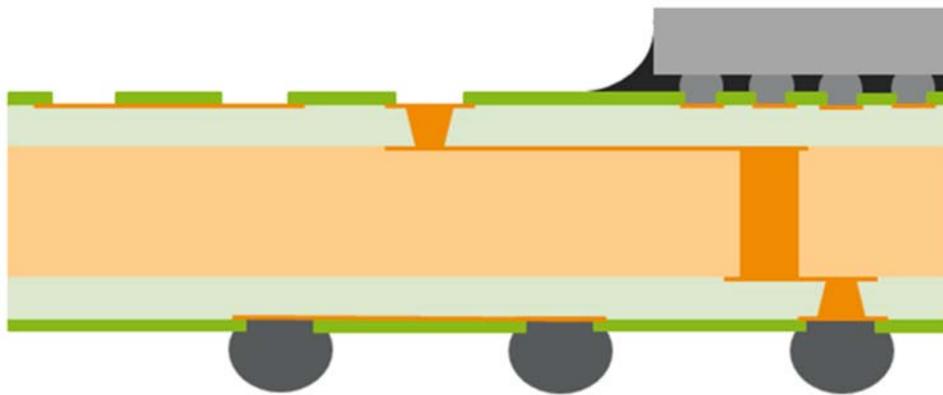
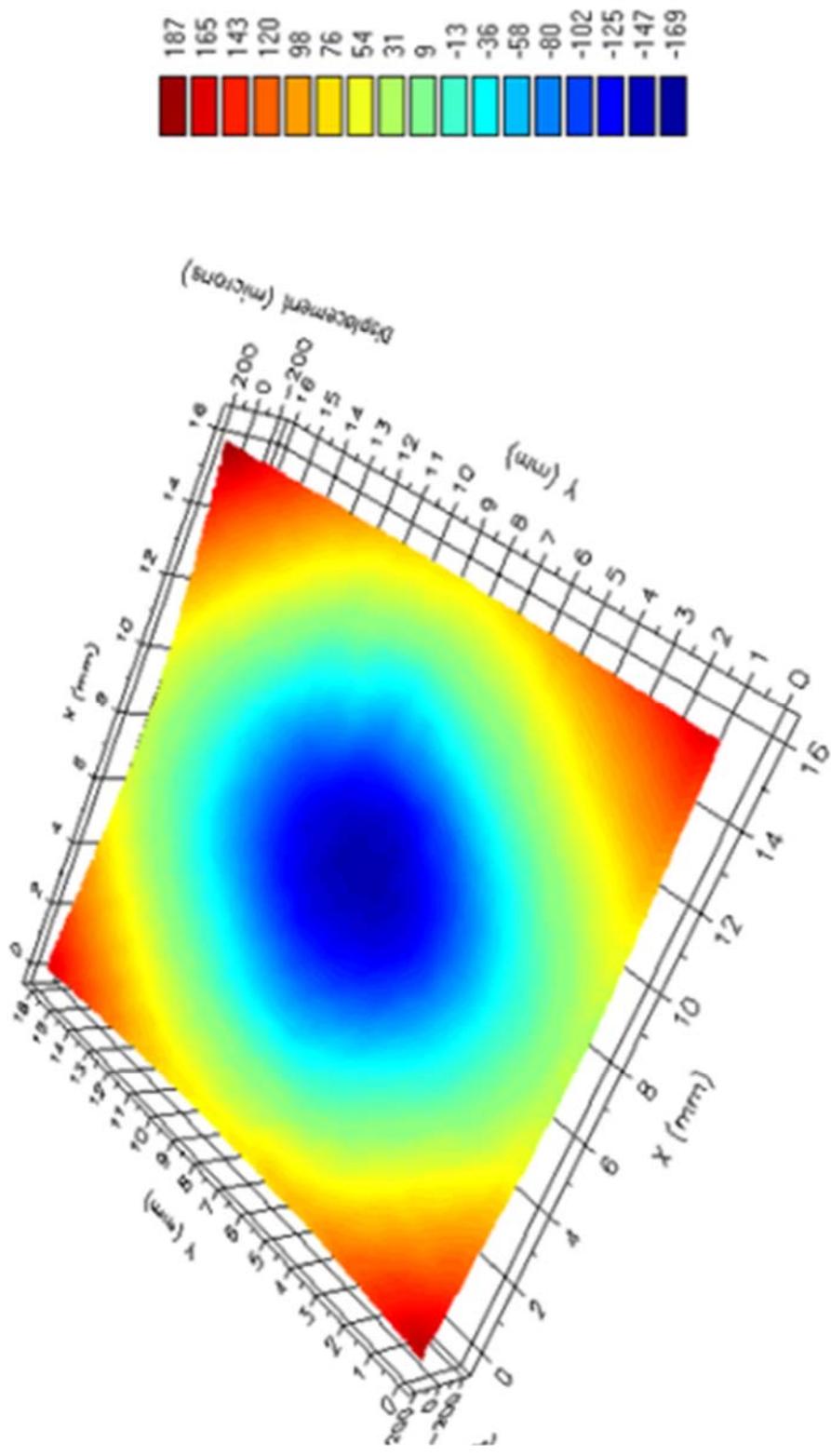


Figure 13. Drawing showing partial cross section of SiP BGA with IC and BGA solder bumps attached.

### 3.3 Interposer Warpage Characterization

Shadow Moiré analysis was performed during the reflow cycle to determine warpage deformation behavior of the SiP interposer with temperature. The SiP-interposer deformation was measured at temperature intervals during ramp up at 25°C (room temperature, RT), 100°C, 150°C, 215°C, and 245°C. During ramp down it was measured at 215°C, 150°C, 100°C and 25°C. Analysis evaluated the free-body deformation across the FBGA bump side and for each component. The temperatures were selected to coincide with milestone temperatures experienced during typical lead-free reflow processes, including peak reflow temperature (245°C) and the expected solder solidification range of 215°C to 150°C. Figure 14 shows a typical Shadow Moiré color-coded warpage configuration for a bare SiP interposer.



Coplanarity = 348 microns

Figure 14. Representative Shadow Moiré contour plot at 25°C for a non-populated SiP FBGA interpose. Image is produced “ball side up” and indicates that the center of the package would be raised above the board surface. (Units in the key are microns, 0.001 mm.)

### 3.4 Assembly and Inspection Processes

The basic process flow used to construct and evaluate the test assemblies was:

1. Print solder paste over the interposer
2. Place the SiP and the interposer CSP (with and without dip flux, as needed)
3. Dip flux and place the CSP on the SiP as required
4. Perform reflow soldering
5. Perform X-ray inspection
6. Perform the daisy-chain verification test

Reflow was performed using a convection reflow oven with 10 heating and 3 cooling zones. All assemblies were inspected by X-ray to characterize quality of the solder joints prior to environmental exposures. The X-ray inspection was primarily focused on characterizing voids in the solder joints and identifying solder bridging, if any. Both CSP and FBGA solder joints were inspected. Of 80 SiP assemblies, only two were found to have workmanship defects. One defect was attributed to a placement error during the pick and place process, which resulted in the SiP being placed one row off in the y-direction. The other defect was due to solder bridging. The solder-bridge defect occurred in a SiP assembled with SnPb solder. The X-ray images showed that six solder-joint pairs located at the center of the device had bridged (Figure 15).

The reason for the bridges is unknown, but bridging at the center of a package often occurs due to the deflection profile of the device resulting either in a convex (corner ball up) or concave (corner balls down) that in both cases results in increased loading, leading to excess solder ball stretching or collapse and possible bridging. This is especially prominent for the concave condition. Based on the Shadow Moiré results, these defects most likely occurred while the samples were near the peak reflow temperature, when the parts demonstrated concave warpage of 120 to 140 microns (0.12 to 0.14 mm) at the center of the FBGA interposer.

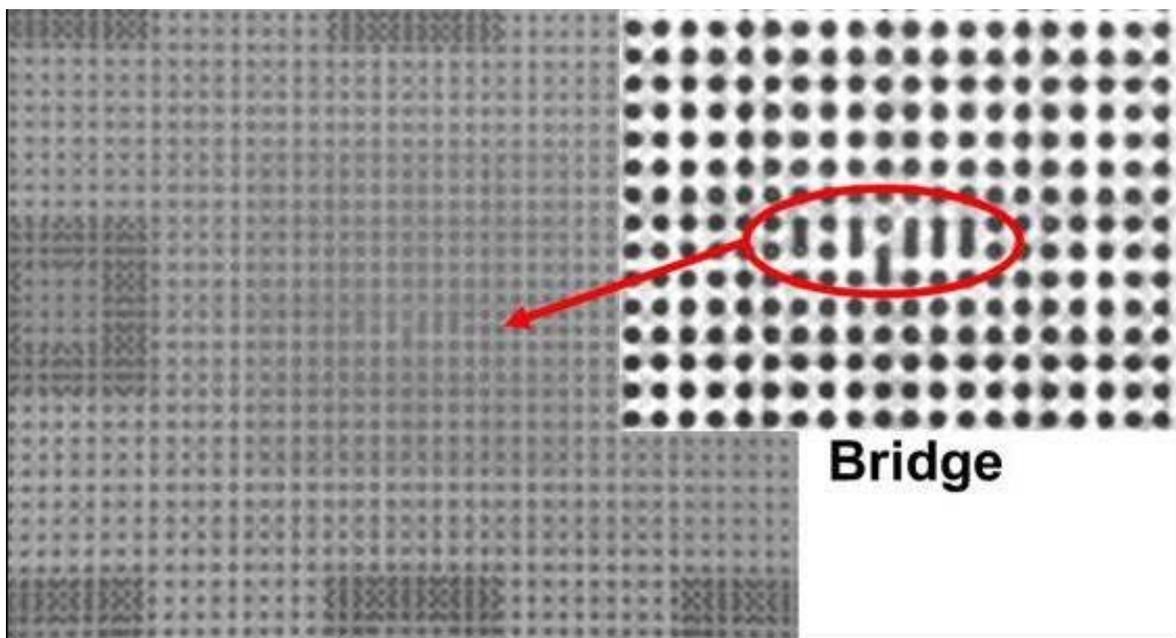


Figure 15. Solder bridging at the center of device in the SiP interposer.

The other goal of the X-ray inspection was to characterize solder-joint void levels. In most cases, the number and/or size of voids observed in the CSP or SiP FBGA solder joints were negligible. However, the SnPb test cell did produce large and numerous voids in the SiP FBGA. Interestingly, the voids were primarily located near the center of the package as shown in Figure 16.

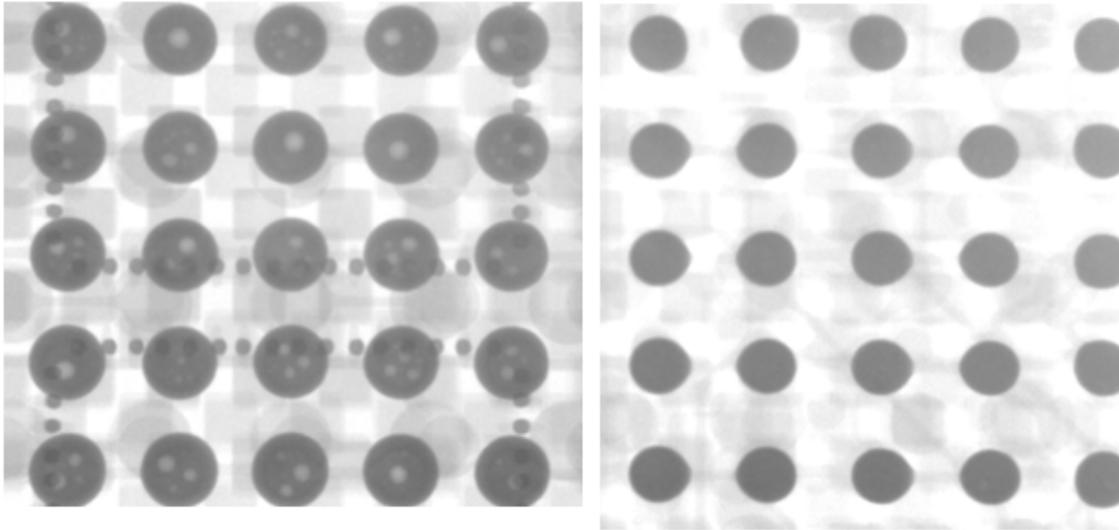


Figure 16. Comparison of voids near center of SnPb SiP (left image) and perimeter of SiP (right image).

### 3.5 Thermal Cycle Test Results

The SiP assemblies with acceptable daisy-chain continuity levels were subjected to accelerated thermal cycle testing in order to evaluate solder-joint reliability. During thermal cycling, an event detector was used to detect resistance spikes, exceeding 500 ohms and lasting in an excess of 200 nanoseconds. Accelerated thermal cycling was performed between  $-40^{\circ}\text{C}$  and  $125^{\circ}\text{C}$  with 15-minute dwells at the temperature extremes with a total cycle of 74 minutes. Figure 17 shows a typical warpage analysis performed on a SnPb solder SiP assembly after thermal cycling. This figure shows that SiP curling up at the corners, imposing peeling stresses on the corner solder joints.

A large number of variables were considered in the DOE design including evaluation of bare FBGA and FBGA balls either with SAC305 or SnPb solders, FBGA fully/partially populated with CSPs and flip chip (FC) die, and CSPs with and without underfills on a SiP. Failure analyses indicate that the SiP FBGA solder joint life was significantly impacted by these variables. The Weibull failure characteristic life ranged from about 500 to 2000 thermal cycles. However, the first cycles-to-failures were lower and were about 300 to 1500 cycles.

SiP FPBGA with underfilled CSPs showed the lowest cycles-to-failures indicating the importance of underfill on the SiP reliability. This test cell was a SAC305 CSP assembly in which the eight CSPs were underfilled. For this case, the Weibull characteristic lifetime of the population was determined to be 512 thermal cycles with the first failure detected at 325 cycles. Cycling of this test cell was stopped after only 800 cycles since 7 out of 8 CSPs had already failed.

An increase in cycles-to failures was also observed when CSPs were not underfilled. The characteristic lifetime increased to 1339 cycles with the first failure at 455 cycles. The possible reasons for such changes in reliability are discussed in the following section.

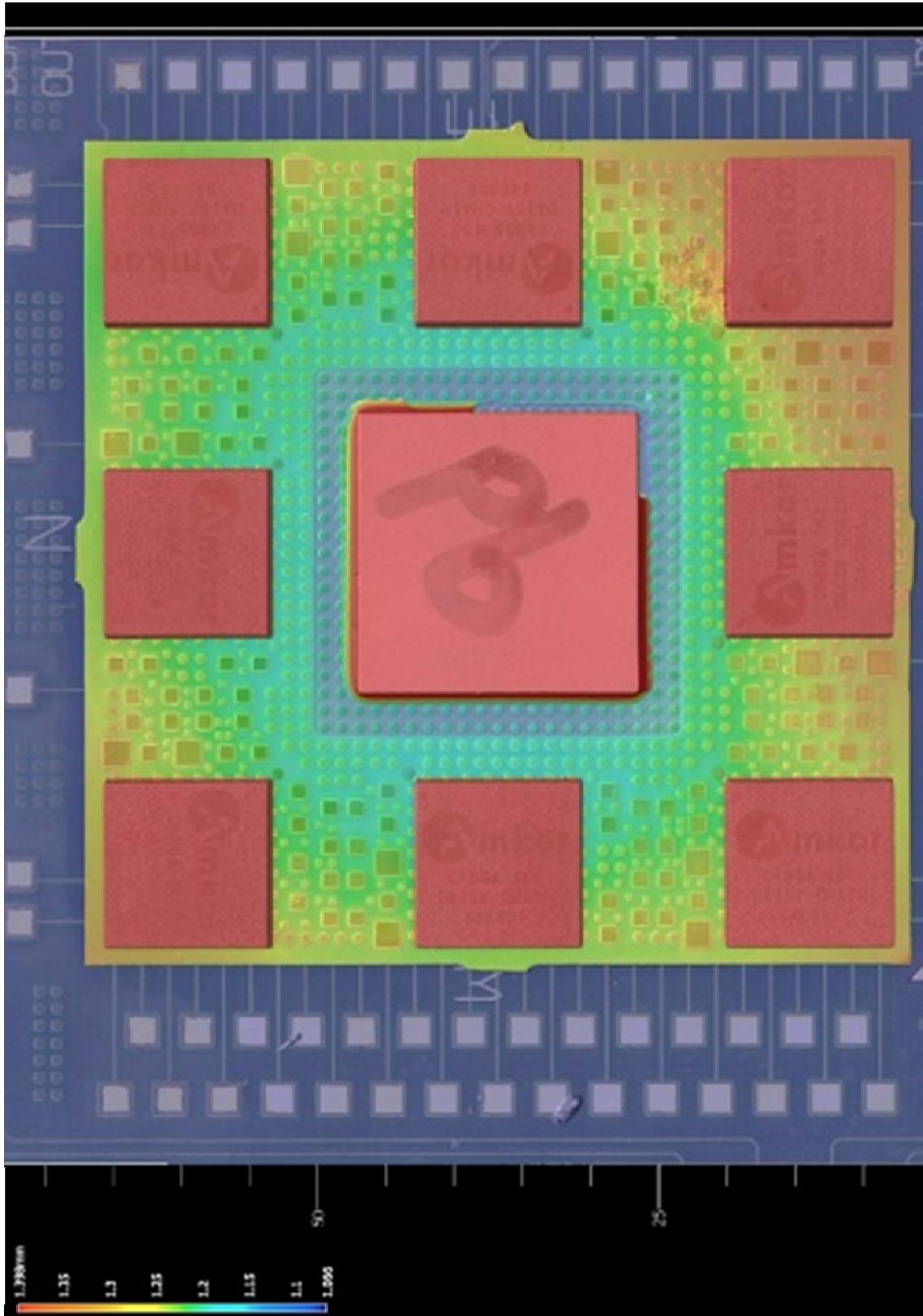


Figure 17. Visual representation of SiP warpage SiP after thermal cycling with corner having the highest values.  
 (Units for the values shown in the upper left are in millimeters.)

## 4.0 CONCLUSIONS

This report presented a comprehensive test matrix developed to assemble and evaluate reliability under thermal cycle and shock cycle conditions for a large number of advanced 3D TMV™ and SiP package assemblies using two different assembly configurations. The fine-pitch ball-grid array (FBGA) packages had various sizes and pitches covering the current demands for the fine-point ball-grid array (FPBGA) and memory technologies. We successfully assembled a large number of these packages onto PCBs and then characterized for quality assurance (QA) by X-ray and optical images and then for solder-joint reliability by performing thermal cycling.

The X-ray images revealed the key workmanship anomalies including the levels of the voids in solder balls and shorts. The use of daisy-chain patterns enabled detecting opens after assembly and during thermal cycling using an event detector continuously or at intervals when removed for inspection and resistance continuity verification. Three thermal cycle/shock profiles were used. An ATC (ramp rate of  $<10^{\circ}\text{C}/\text{min}$ ) in the range of  $-55^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$  for 3D TMV™ and an ATC in the range of  $-40^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$  for SiPs. The 3D TMV™ assemblies were also subjected to ATSC in the range of  $-100^{\circ}\text{C}$  to  $125^{\circ}\text{C}$  with a higher than  $20^{\circ}\text{C}/\text{min}$  ramp rate. IPC 9701 defines profiles with ramp rates of higher than  $20^{\circ}\text{C}/\text{min}$  as “thermal shock” cycle [16].

The findings and failure analyses test results after thermal cycle/shock cycles are summarized in the following four items.

1. For an ATC of  $-55^{\circ}/125^{\circ}\text{C}$ , the three 3D TMV™ stack configuration assemblies— built with SnPb solder at package and PCB levels, flux dip at package level and SnPb solder at PCB level, and pre-stack package and solder at PCB—did not show failures after 200 ATC determined by daisy-chain resistance measurement.
2. For an ATSC of  $-100^{\circ}/125^{\circ}\text{C}$ , the three 3D TMV™ stack configuration assemblies— built with SnPb solder at package and PCB levels, flux dip at package level and SnPb solder at PCB level, and pre-stack package and solder at PCB—did not show failures after 200 ATSC determined by daisy-chain resistance measurement.
3. For an ATC of  $-40^{\circ}/125^{\circ}\text{C}$ , the SiP assemblies with either SnPb or SAC305 solder balls did not show failures after 200 ATC determined by daisy-chain resistance measurement.
4. Possible reasons for early failures of SiP assemblies with underfilled CSPs were presented. Key parameters that play roles in early failures are postulated to be: (1) the global coefficient of thermal expansion (CTE) mismatches between FPBGA and PCB, (2) local stiffness due to CSP on FPBGA, and (3) higher warpage at the FPBGA corner locations.

Further qualification testing is being performed by thermal cycling and characterizations to determine failure mechanisms and the reliability limitations of these advanced 2.5/3D electronic packaging technologies. The qualification guidelines presented in this report—based on the test results for two key advance packaging configuration and assemblies (3D TMV™ stack with three configuration and SiP with CSP and IC on a large FPBGA—will facilitate the use of newly advanced electronic packaging technologies by NASA projects. It allows the projects the use of newly available and very dense FPBGA and memory area-array packages with known reliability and mitigation risks, allowing greater processing and memory power in a smaller board footprint and lower system weight.

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## 6.0 ACRONYMS AND ABBREVIATIONS

2.5D	multiple chips in a stacked configuration
3D	multiple chips in three dimensional configuration
ATC	acceleration thermal cycle
ATSC	accelerated thermal shock cycle
BGA	ball-grid array
C4	controlled collapsible chip connector
CABGA	ChipArray® ball-grid array
COTS	commercial-off-the-shelf
CSP	chip scale (size) package
CTE	coefficient of thermal expansion
DOE	design of experiment
ENEPIG	electroless nickel electroless palladium immersion gold
FC	flip chip
FCBGA	flip-chip ball grid array
FPBGA	fine-pitch ball-grid array
FR-4	glass-reinforced epoxy laminate material
IC	Integrated circuit
I/O	input/output
JPL	Jet Propulsion Laboratory
NASA	National Aeronautics and Space Administration
NEPP	NASA Electronic Parts and Packaging
PBGA	plastic ball grid array
PCB	printed circuit board
PEM	plastic encapsulated materials
PiP	package in package
PoP	package on package
PWB	printed wiring board
QA	quality assurance
QFP	quad flat pack
RoHS	Restriction of Hazardous Substances (European Union Directive 2002/95/EC)
RT	room temperature

SAC	tin silver copper
SEM	scanning electron microscopy
SiP	system in package
TC	thermal cycle
TMV	through mold via
TSV	through silicon via
TV	test vehicle
WLP	wafer-level package