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# Virtex-5 CN Package Daisy Chain Evaluation Test Report

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## 1.0 INTRODUCTION

Modern space field programmable gate array (FPGA) devices, such as Xilinx Virtex 4 (V4) and 5 (V5), with their increased functional density and operational frequency, have received a lot of attention from the space community. These parts are packaged in non-hermetic ceramic flip chip forms, with column grid array (CGA) board-level interconnection (Table 1). Figure 1 illustrates the evolution of the Xilinx V5 packages.

Table 1. Comparison of different versions of Virtex 5 packages

| | CF Package (Before 2012) | CF Package (2012 to 2014) | CN Package |
|---|---|---|---|
| Heat spreader | SiC (32x25x2mm)<br>Electrically non-conductive | SiC (38.5x38.5x2mm)<br>Electrically non-conductive | Al-SiC (44.1x44.1x0.85mm)<br>Electrically conductive |
| Heat spreader corner pillars | None | None | 4 pillars at each corner |
| Thermal interface material between the die and the heat spreader | Electrically conductive<br>IBM proprietary | Electrically conductive<br>IBM proprietary | Electrically non-conductive<br>Kyocera proprietary |
| Flip chip solder bump material | 95Pb5Sn | 95Pb5Sn | Sn63Pb37 |
| Underfill material | IBM proprietary | IBM proprietary | Kyocera proprietary |
| Solder column | IBM CLASP (Pb90Sn10) | IBM CLASP (Pb90Sn10) | Six Sigma (80Pb10Sn) |
| Weight | 50g | 54.57g | 49g |

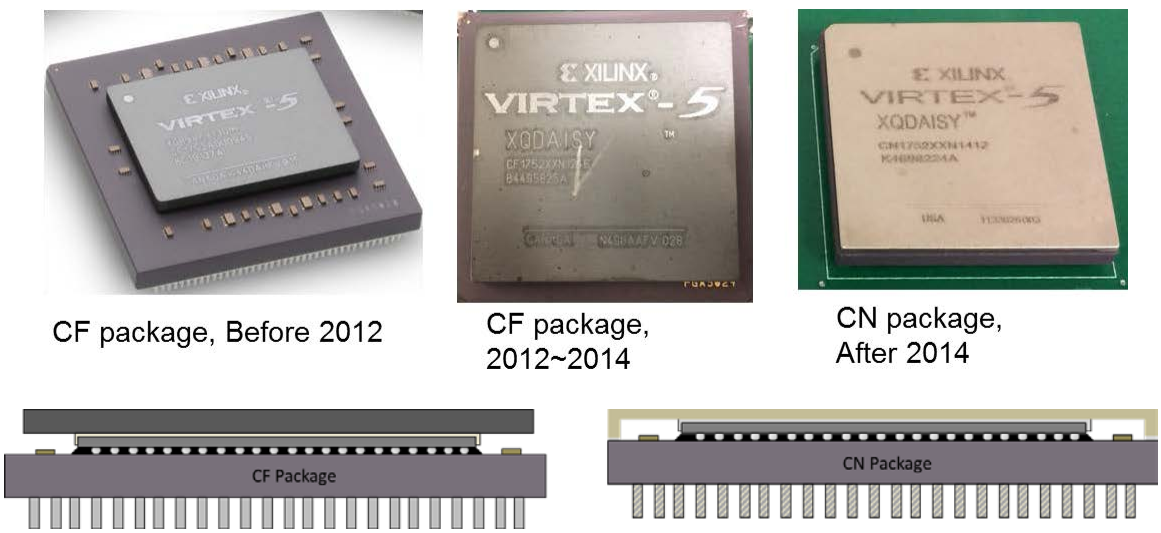


Figure 1. Xilinx V5 package styles have changed slightly over time.

The CF package was packaged at IBM's Bromont facility. The first design change, in 2012, was to increase the size of the heat spreader to cover the capacitors around the die. The major package design change happened in 2014, when IBM shut down the Bromont facility and Xilinx selected Kyocera as the packaging service provider. Since most of the packaging materials in the CF package were IBM proprietary, the package design went through major changes, including the board-level interconnect. The CGA solder columns were changed from IBM CLASP columns to Six Sigma columns. The IBM CLASP columns are composed of 90Pb10Sn and are attached to the package with Pd-doped Sn63 solder. The Six Sigma columns are made of 80Pb10Sn with a copper spiral around the column and are attached to the package with Sn63 solder.

The comparative reliability of IBM CLASP columns and Six Sigma columns has often been a subject of debate. Microsemi reliability test results claim that Six Sigma columns showed about 30% greater temperature cycling life than the CLASP columns [1]. The current task mainly focused on generating statistical data of the CN packages' board-level temperature cycling reliability.

## 2.0 TEST DETAILS

In designing the test matrix, JPL's approach was to use existing Xilinx test data as the baseline and generate the comparative data (Table 2). Xilinx performed their tests at temperatures ranging from 0°C to 100°C, with a 10-minute dwell time and 5-minute ramp time [2]. In the current study, the ramp time was set to 10 minutes as an alternative to Xilinx's 5 minutes, due to the unavailability of equipment capable of achieving such a temperature profile. The current task also performed -55°C /100°C (-55/100) temperature cycling, known as NASA handbook cycling, to generate reliability data under conditions familiar to NASA. The dwell time for the -55/100 test was 10 minutes and the ramp time was 47 minutes. The 0°C /100°C (0/100) temperature cycling was done in a Tenney LN2 chamber; -55/100 temperature cycling was done in a Thermotron S-8C Freon chamber.

Since the purpose of 0/100 temperature cycling was to generate reliability data comparable to Xilinx's data on CF packages, originally it was preferred to match their board construction. This was challenging because Xilinx board construction is proprietary information and thus insufficient to construct an exact match. Instead, the printed circuit boards were configured similar to the boards for the flight application, so the reliability data could be relevant to actual applications. For example, the board had 18 layers and the same metal thickness as boards frequently used for flight applications (e.g., board thickness affects temperature cycling life [3] ).

Table 2. Comparison of test conditions: Xilinx vs. JPL

| | Existing Xilinx Data | JPL Condition 1 | JPL Condition 2 |
|---|---|---|---|
| Board | 8 layer FR4 | 18 layer PI and FR4 | 18 layer PI and FR4 |
| Pad opening | 0.7mm | 0.7mm | 0.7mm |
| Board finish | HASL | HASL | HASL |
| Temperature cycle range | 0 to 100°C | 0 to 100°C | -55 to 100°C |
| Dwell time | 10 min | 10 min | 10 min |
| Ramp time | 5 min | 10 min | 47 min |

For the test matrix (Table 3), 8 parts were assigned for each temperature cycling condition; 4 of the 8 parts were assembled on FR4 boards (IPC/26) and the remaining 4 were assembled on polyimide boards (IPC/41). Although the board resin material used would only have a small effect on the temperature cycling life of solder columns, FR4 boards were built to best reflect the Xilinx conditions and also to reflect a worst case condition. Two parts were assigned to investigate the capacitor solder joint reliability and 2 parts were temperature cycled in a dual-zone chamber with a 20°C/min ramp rate to generate solder column reliability data under a high ramp rate condition.

The test board had 7 daisy chains (Figure 2), located at columns at each of the 4 corners, the outer 2 rows, the next 3 rows, and all internal rows (Figure 3). The resistance of each daisy chain was continuously monitored.

Table 3. Test matrix

| Part S/N | Test Details | Board SN | Board Material |
|---|---|---|---|
| 01 | Temp cycling to inspect BME capacitor solder joints | SN009 | PI |
| 02 | Part level reflow / SMT process optimization / capacitor solder joint evaluation | SN001 | |
| 03 | 0 to 100°C TC (10C/min ramp, 10 min dwell) | SN101 | FR4 |
| 04 | | | |
| 05 | | SN102 | |
| 06 | | | |
| 07 | -55 to 100°C TC (~3.3C/min ramp, 10 min dwell) | SN103 | |
| 08 | | | |
| 09 | | SN104 | |
| 10 | | | |
| 11 | 0 to 100°C TC (10C/min ramp, 10 min dwell) | SN002 | PI |
| 12 | | | |
| 13 | | SN003 | |
| 14 | | | |
| 15 | -55 to 100°C TC (~3.3C/min ramp, 10 min dwell) | SN004 | |
| 16 | | | |
| 17 | | SN005 | |
| 18 | | | |
| 19 | Dual-zone chamber cycling (-55 to 100C, 10 min dwell) | SN006 | |
| 20 | | | |

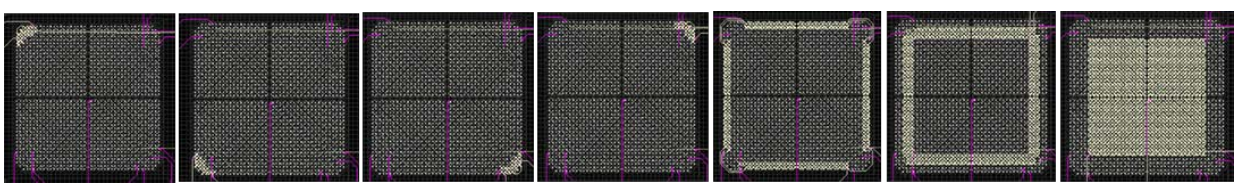

Figure 2. Daisy chain design.

Figure 3. The assembled test board.

The heat spreader of one of the parts was removed to investigate the solder joints of the BME capacitors. Figure 4 shows an SEM image of solder joints at one of the capacitors after the removal of the heat spreader, without temperature cycling.

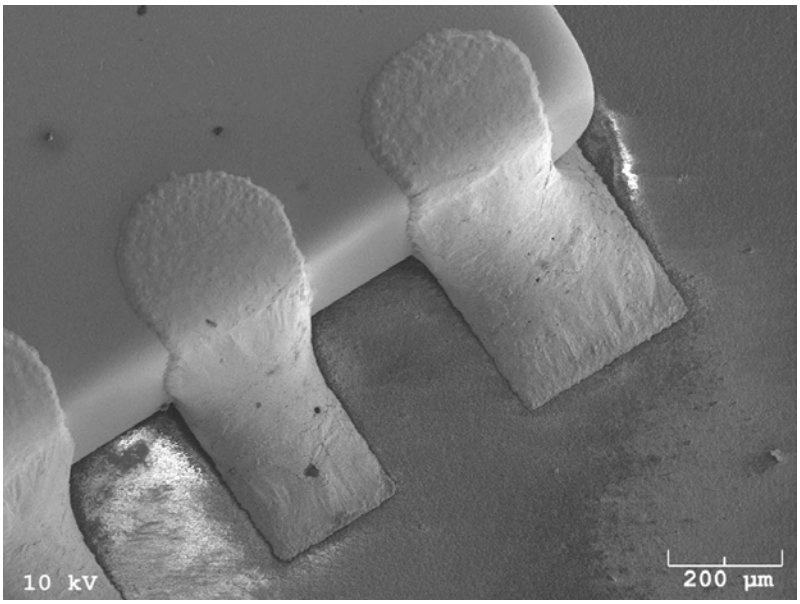


Figure 4. Solder joints of a decoupling BME capacitor before temperature cycling.

## 3.0 RESULTS

During the temperature cycling tests, both ambient temperature and the resistances of daisy chains were continuously monitored. Figure 5 shows the measured ambient temperatures of the chambers during temperature cycling. Figure 6 shows the resistances of daisy chains during the temperature cycling.

At the conclusion of testing, 0/100 cycling had completed 6586 cycles, -55/100 temperature cycling had completed 1705 cycles, and -55/100 dual-zone chamber temperature cycling had completed 3389. No part failed during the 0/100 temperature cycling. One part failed during the -55/100 temperature cycling, at 1236 cycles at the innermost daisy chain. One of part failed at 2097 cycled during dual-zone -55/100 thermal cycling, at the second innermost daisy chain. Since the corner columns with a large distance to neutral point (DNP) generally fail first, these failure modes were unexpected. Potential causes included a workmanship issue, a part defect, or a board via failure. As shown in Figure 7, the failed parts exhibited discontinuity only within a certain range of temperatures. The test boards had probing pads on the back side, each of them connected to a solder column land pad, so any failed solder column could be located by electrically probing the back-side pads. However, this approach did not work because the backside probing pads could only be probed outside the chamber at room temperature and the two failed parts exhibited continuity at room temperature for the duration of testing. A thorough failure analysis would be necessary to identify the mode and cause of failure. Table 4 summarizes the overall test results and Figure 7 illustrates how the resistance of the failed innermost daisy chain changed.

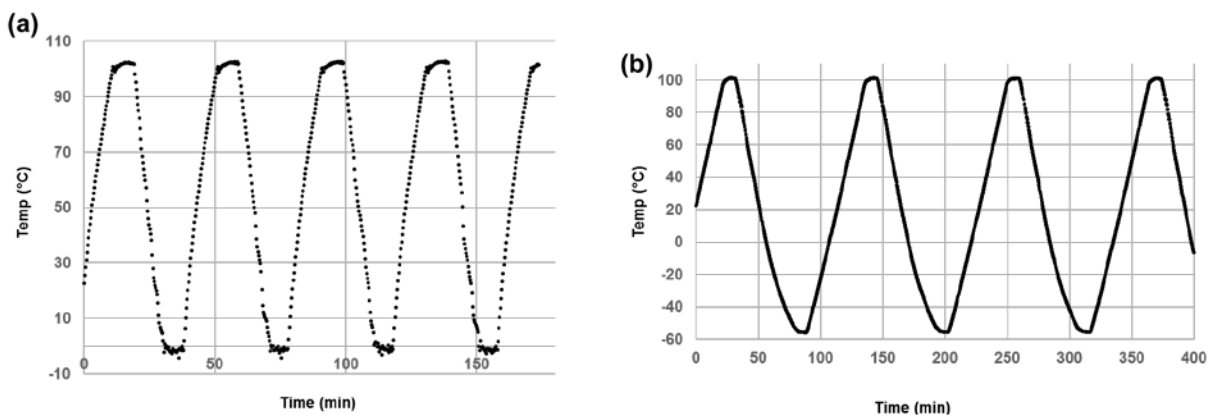


Figure 5. Ambient temperature profiles of (a) 0/100 and (b) -55/100 temperature cycling.

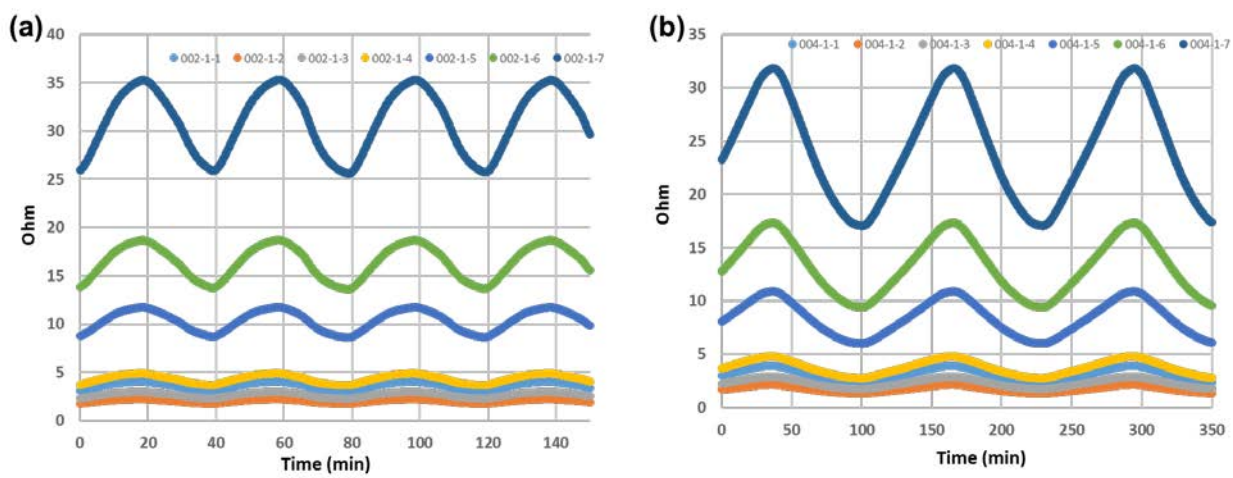


Figure 6. Resistances of daisy chains during (a) 0/100 and (b) -55/100 temperature cycling.

Table 4. Summary of temperature cycling test results

| Part S/N | Board Material | Test Details | Board SN | Number of cycles done | Results |
|---|---|---|---|---|---|
| 03 | FR4 Board | 0 to 100°C TC (10°C/min ramp, 10 min dwell) | SN101 | 6586 | No failure |
| 04 | | | | 6586 | No failure |
| 05 | | | SN102 | 6586 | No failure |
| 06 | | | | 6586 | No failure |
| 07 | | -55 to 100°C TC (~3.3°C/min ramp, 10 min dwell) | SN103 | 1705 | No failure |
| 08 | | | | 1705 | No failure |
| 09 | | | SN104 | 1705 | No failure |
| 10 | | | | 1705 | No failure |
| 11 | PI Board | 0 to 100°C TC (10°C/min ramp, 10 min dwell) | SN002 | 6586 | No failure |
| 12 | | | | 6586 | No failure |
| 13 | | | SN003 | 6586 | No failure |
| 14 | | | | 6586 | No failure |
| 15 | | -55 to 100°C TC (~3.3°C/min ramp, 10 min dwell) | SN004 | 1705 | No failure |
| 16 | | | | 1705 | No failure |
| 17 | | | SN005 | 1705 | The innermost daisy chain failed at 1236 cycles. |
| 18 | | | | 1705 | No failure 1705 cycles |
| 19 | | Dual-zone chamber cycling (-55 to 100°C, 10 min dwell) | SN006 | 3389 | No failure 3389 cycles |
| 20 | | | | 3389 | The second innermost daisy chain failed at 2097 cycles. |

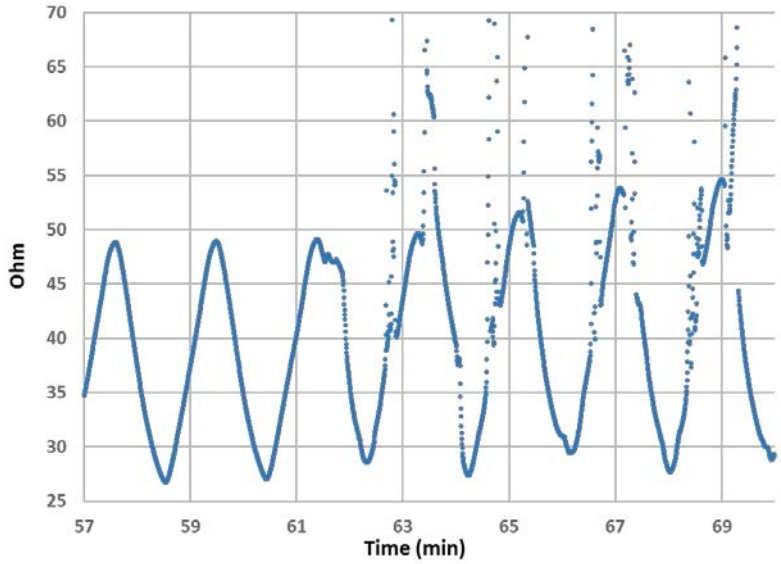


Figure 7. Resistance change of the first failed daisy chain during -55/100 temperature cycling.

Solder columns were also visually inspected. Figure 8 shows optical microscope images of solder columns before and after the temperature cycling tests. The initially shiny surface of the solder columns and fillet

became dull and gray due to fatigue. Microcracks can also be observed on solder columns that went through temperature cycling tests.

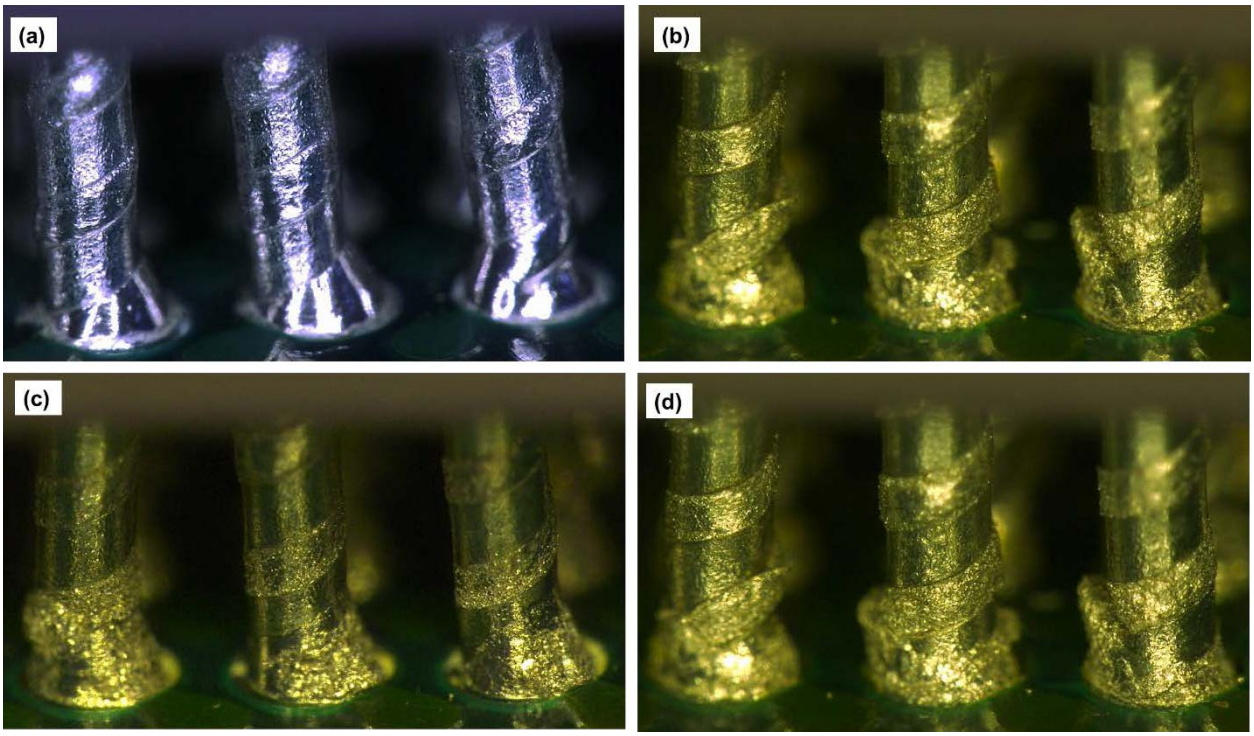


Figure 8. Optical microscope images of solder columns: (a) before temperature cycling; (b) after 1705 cycles at -55/100°C temperature cycling in a single-zone chamber; (c) after 6586 cycles at 0/100°C temperature cycling in a single-zone chamber; and (d) after 3389 cycles of -55/100°C temperature cycling in a dual-zone chamber with a high ramp rate.

Figure 9. Shows optical microscope images of solder joints at the decoupling capacitors. The solder joints became dull due to fatigue. The inspected capacitor solder joints did not have cracks. However, only two V5s were inspected for capacitor solder joints and whether all capacitor solder joints survived temperature cycling is inconclusive.

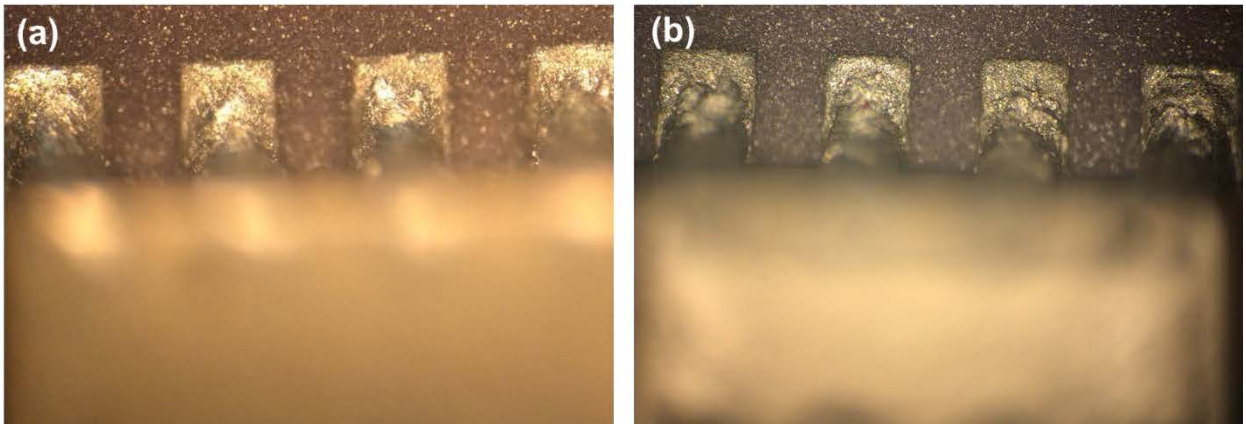


Figure 9. Solder joints of a decoupling BME capacitor (a) after 6586 cycles of 0/100 temperature cycling and (b) after 1705 cycles of -55/100 temperature cycling.

## 4.0 DISCUSSION

The resistances of all daisy chains were continuously monitored during temperature cycling. Per IPC-9701A, a 20% increase in resistance was the criteria for failure. Figure 10 shows the resistances of the corner daisy chains at the beginning of the test and after 6500 cycles of 0/100 temperature cycling. Even after 6586 cycles, there is no obvious resistance increase, indicating no solder column failures. Figure 11 shows resistances of the corner daisy chains of a part measured during -55/100 temperature cycling. During -55/100 temperature cycling, one part failed at the 1236 cycle. However, this failure took place within the innermost daisy chain, which suggests the failure was likely due to a part defect or via failure. Other parts did not show any increase in resistance, as measured up to 1705 cycles. One of the two parts temperature-cycled from -55 to +100°C in a dual-zone chamber showed a failure at 2097 cycles, but this failure also happened within an internal daisy chain. In other words, no obvious solder fatigue failure took place during any test.

The Weibull cumulative distribution function (CDF) is given as,

$$f(t) = 1 - \exp(-(t/\eta)^{\beta}) \qquad (1)$$

Where f(t) is probability, t is the time of failure, η is characteristic life, and β is shape factor. If the failure at 1236 cycles during -55/100 temperature cycling was a normal solder fatigue failure, the β has to be smaller than 2.4 (which is unreasonably low) to have the first failure at 1236 cycles and not to have the second failure up to 1705 cycles.

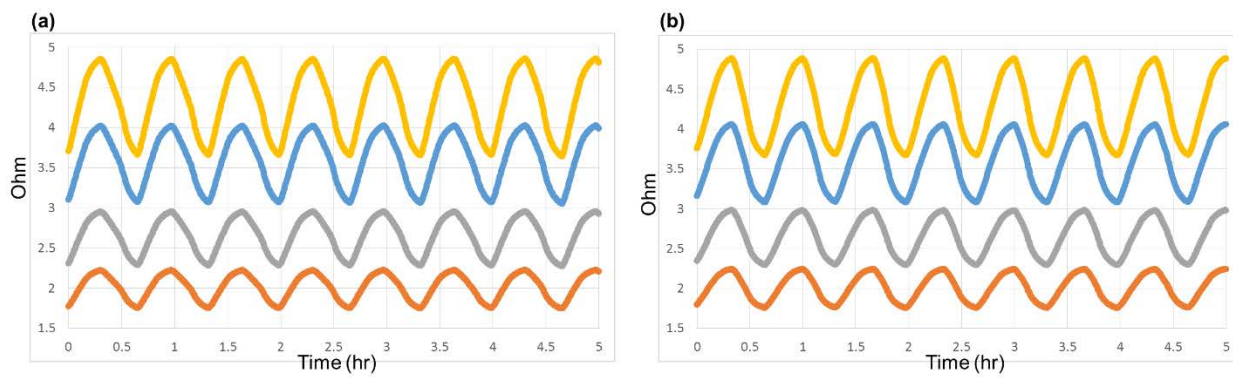


Figure 10. Resistances of 4 corner daisy chains of a part, measured during 0/100 temperature cycling: (a) at the beginning of the test, and (b) after 6300 cycles.

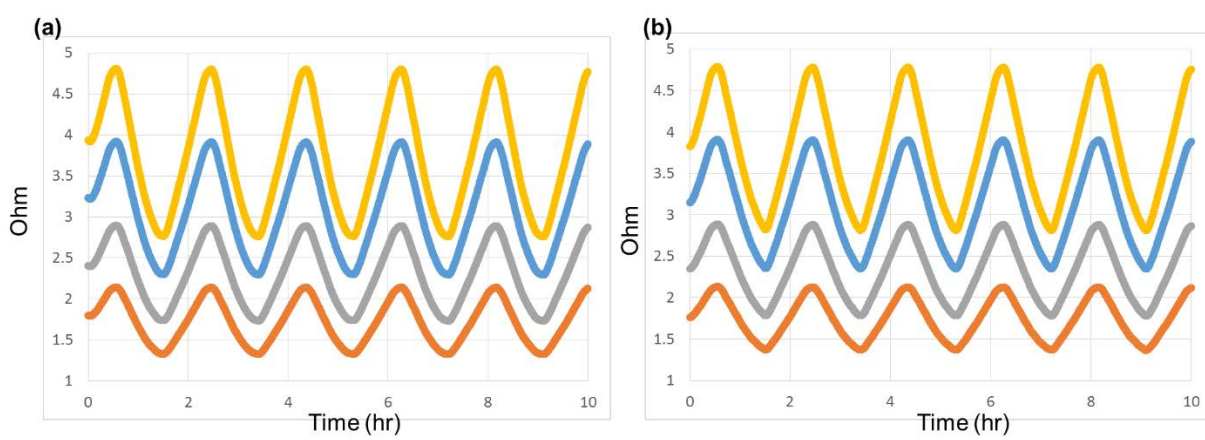


Figure 11. Resistances of 4 corner daisy chains of a part, measured during -55/100 temperature cycling: (a) at the beginning of the test, and (b) after 1600 cycles.

Compared to the already existing industry data, the solder columns exhibited unusually long temperature cycling life in the current test. An early study performed at Xilinx showed that the IBM CLASP columns of CF1752 packages had about 4700 cycles of characteristic life. As explained previously, Xilinx test conditions were different from the test conditions used in the current task. The most commonly used fatigue equation for Ceramic Column Grid Array (CCGA) is the modified Coffin-Manson equation by Norris and Landzberg [4], later further modified by Teng [5]. Although the equation was initially based on data of flip chip solder bumps without underfill and Ceramic Ball Grid Array (CBGA) balls, it is frequently used to calculate the acceleration factor of CCGAs for rough estimation. The fatigue equation is given below.

$$AF = \left(\frac{\Delta T_L \times DNP_L}{\Delta T_F \times DNP_F}\right)^{1.9} \times \left(\frac{f_F}{f_L}\right)^{1/3} \times e^{1414\left(\frac{1}{T_F} - \frac{1}{T_L}\right)} \qquad (2)$$

where $\Delta T_L$ and $\Delta T_F$ are the temperature ranges of temperature cycling during the laboratory test and the field operation, respectively.$DNP_L$ and $DNP_F$ are distance from neutral point of the part used at the laboratory and field. $f_L$ and $f_F$ are frequencies of temperature cycling at the laboratory and field; and $T_L$ and $T_F$ are the highest temperatures measured during the temperature cycling at both the laboratory and field. This equation is only useful for rough estimation, as it uses constant exponents regardless of test conditions and does not consider many variables, such as board thickness. Regardless, it would be worthwhile to see how Xilinx conditions could be translated to JPL conditions for the equation. Per equation (2), one Xilinx 0/100 cycle is equivalent to 0.28 JPL -55/100 cycles and 0.91 JPL 0/100 cycles. In other words, the CF1752 CLASP columns, which had about 4700 cycles of characteristic life, would show about 1300 cycles of characteristic life during the -55/100 JPL cycles and about 4300 cycles of characteristic life during the 0/100 JPL cycles. The Weibull plot from Microsemi's datasheet shows that Six Sigma columns had about 33% longer fatigue life than CLASP columns [1]. If we assume that the both types of columns have the same exponent and apply the 33% fatigue life difference to the current case, the estimated characteristic life of CN package columns is approximately 5700 cycles for the 0/100 JPL condition and approximately 1700 cycles for the -55/100 JPL condition. These anticipated characteristic life durations, although rough estimations, are far shorter compared to the current test results. In addition, Microsemi's CG1152 package with Six Sigma columns showed the first failure among 6 samples at 1212 cycles and about 1600 cycles of characteristic life during -55/105 temperature cycling [1]. JPL's -55/100 profile is only slightly less severe than Microsemi's -55/105 cycling profile, and Xilinx CN1752's package diagonal length is about 10mm larger than Microsemi's CG1152. In theory, CN1752 should have exhibited shorter, or at least comparable, temperature cycling life during the -55/100 test than what CG1152 exhibited during its -55/105 test.

Table 5. Temperature cycling conditions used by JPL, Xilinx, and Microsemi.

| Test | Delta T (°C) | Cycle Frequency (cyc/day) | Max Temperature (°C) | Ramp Time (min) | Dwell Time (min) |
|---|---|---|---|---|---|
| Xilinx condition | 100 | 48 | 100 | 5 | 10 |
| JPL condition (0/100) | 100 | 36 | 100 | 10 | 10 |
| Microsemi condition | 160 | 11.61 | 105 | 32 | 30 |
| JPL condition (-55/100) | 155 | 12.63 | 100 | 47 | 10 |

The discussion above shows that the temperature cycling life that the solder columns exhibited during the current test was unusually long compared to the existing data, and it is difficult to explain the difference with the fatigue equation. The unusually long fatigue life could be due to JPL's better controlled inspection, handling and attachment process of the parts. JPL's board had much larger number of layers (18 layers) than Xilinx's (8 layers) and Microsemi's (10 layers) boards, which rules out board thickness as the cause of the long fatigue life (the temperature cycling life of solder joints decreases as the board thickness increases [3]). It is also possible that JPL's conditions were more benign than industry's, although at a

glance the conditions look similar. JPL's -55/100 temperature cycling condition seems similar to Microsemi's -55/105 condition (see Table 5); the delta T and maximum temperature is almost within the error range of most temperature cycling tests, since the actual temperature of solder joints can be slightly different than the ambient, or of the surface of the board, or of the package where the temperature is measured. JPL's 0/100 test condition and the Xilinx 0/100 test condition have identical temperature ranges. The only difference between the JPL and industry conditions is the cycle frequency. These differences are not large enough to cause such difference in fatigue life, if the fatigue equation (1) holds true. Since the frequency term of the fatigue equation is inversely proportional to the duration of a cycle, the number of cycles to fail will decrease as duration per cycle increases. The duration per cycle is the sum of ramp time and dwell time, and JPL's condition had longer ramp time and shorter dwell time than industry's. For the same duration per cycle, having shorter ramp time and longer dwell time would be more severe than the opposite case, since short ramp time would induce greater strain rate and longer dwell time would induce more creep effect to solder joints at the peak temperature [6, 7, 8]. The differences in ramp rate and dwell time could have contributed to the long solder fatigue life in the current test. However, the individual effects of the ramp rate and dwell time on solder fatigue life over different temperature ranges are not well understood, as there is insufficient literature or data studies dedicated to this topic.

Although there was no obvious solder fatigue failure to determine the number of cycles with a 1% chance of failure, the fact that no solder joint failed until the end of the tests still allows us to make conservative estimations by assuming that one of the samples was at the brink of failure at the end of testing and would have failed if it had gone through one additional cycle. The estimated conservative number of cycles with a 1% chance of failure was about 3900 cycles for 0/100 temperature cycling and about 1000 cycles for -55/100 temperature cycling, when a reasonably conservative value of shape factor was used (~5).

## 5.0 RECOMMENDATIONS

Since there are not enough failed parts to produce statistical data, the probability of failure at a given number of cycles cannot be determined yet. All 8 parts survived up to 6586 cycles of 0/100 temperature cycling. During -55/100 temperature cycling, all 8 parts survived up to 1705 cycles, except for one part that failed at 1236 cycles, most likely due to a part defect, workmanship issue, or board via failure. This test proves the robustness of the board level interconnect of Virtex 5 CN packages, if they are attached to boards with JPL-level well-controlled inspection, handling, and attachment processes. It must be noted that the current result is not applicable to the cases where a V5 is attached to a heat transfer device or has corner support. In actual applications, V5s, as high-power FPGA, are frequently attached to a heat transfer device, such as heat pipes or heat straps. In such cases, the board-level reliability of a V5 has to be assessed case-by-case, since the reliability is affected by many parameters, such as the geometry of heat transfer device, corner support configuration, and properties and thickness of the thermal interface material.

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