

A Compact Two-stage 120 W GaN High Power Amplifier for SweepSAR Radar Systems

Tushar Thrivikraman, Stephen Horst, Douglas Price,
James Hoffman, and Louise Veilleux
Radar Science and Engineering
Jet Propulsion Laboratory
California Institute of Technology
4800 Oak Grove Drive, Pasadena, CA 91109
818-393-8628
Tushar.Thrivikraman@jpl.nasa.gov

Abstract—This work presents the design and measured results of a fully integrated switched power two-stage GaN HEMT high-power amplifier (HPA) achieving 60% power-added efficiency at over 120 W output power. This high-efficiency GaN HEMT HPA is an enabling technology for L-band SweepSAR interferometric instruments that enable frequent repeat intervals and high-resolution imagery. The L-band HPA was designed using space-qualified state-of-the-art GaN HEMT technology. The amplifier exhibits over 34 dB of power gain at 51 dBm of output power across an 80 MHz bandwidth. The HPA is divided into two stages, an 8 W driver stage and 120 W output stage. The amplifier is designed for pulsed operation, with a high-speed DC drain switch operating at the pulsed-repetition interval and settles within 200 ns. In addition to the electrical design, a thermally optimized package was designed, that allows for direct thermal radiation to maintain low-junction temperatures for the GaN parts maximizing long-term reliability. Lastly, real radar waveforms are characterized and analysis of amplitude and phase stability over temperature demonstrate ultra-stable operation over temperature using integrated bias compensation circuitry allowing less than 0.2 dB amplitude variation and 2° phase variation over a 70°C range.

Details of the SweepSAR concept are can be found in [2], [3], and [4]. The large swath and the limited SNR of the receiver requires the transmitter to have a high peak power. For the proposed L-band SweepSAR mission, 24×100 W transmitters are required. Given this high peak power, an extremely efficient compact TRM is required to allow this mission to be feasible. Gallium Nitride (GaN) High Electron mobility transistors (HEMTs) technology has been shown to provide high-power and high-efficiency making it the perfect candidate for this next generation radar system [5].

Due to the large commercial interest in GaN, there is plenty of literature targeting telecommunication applications. However, due to the specific requirements for space-flight operation (radiation and thermal environments), special care must be taken in the design of a transmitter able to meet the needs of a repeat-pass interferometry system. The resolutions of these systems are limited by amplitude and phase stability. This is complicated by the SweepSAR concept where individual per-channel errors cannot be corrected due to on-board digital beamforming. One of the largest sources of performance drift within the TRM are thermal effects on amplifier and component performance. The TRM is designed with internal calibration loops as described in [6] to achieve on the order of 0.1 dB amplitude and 0.1° phase knowledge, however, by designing both electrically and mechanically for stable thermal operation, the calibration can be minimized allowing more time to gather science data.

Typically, in most systems, the HPA is most sensitive to thermal drifts due to the non-linear large signal operation, therefore, a key focus on the TRM design for the proposed L-band SweepSAR mission was to create a thermal stable HPA, optimizing both the electrical performance and packaging design. Electrically the HPA was stabilized by (1) operating the device at or near saturation by creating a compressed two-stage design and (2) a temperature compensated gate bias circuitry. Mechanically, (1) HPA packaging was optimized to provide an efficient path to the thermal radiator and (2) optimize thermal radiator area to maintain temperature. Section 2 will describe the detailed electrical design of the 8 W and 120 W stages. Section 3 will present the packaging design. Section 4 and Section 5 presents the measured results of the HPA over temperature and an analysis of the amplitude and phase stability.

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1. INTRODUCTION

Next generation Synthetic Aperture Radar (SAR) remote sensing platforms utilize new concepts such as the SweepSAR technique that provide increased swath size, high resolution, rapid global coverage, as well as sub-cm interferometry and polarimetry. An L-band SweepSAR mission would use multiple transmit/receive (T/R) channels and digital beamforming to achieving simultaneously high resolution and large swath [1]. One of the key challenges in implementing the SweepSAR concept is the development of space-qualified efficient T/R modules (TRMs) that provide the amplitude and phase stability necessary for repeat pass interferometry.

2. HPA ELECTRICAL DESIGN

GaN HEMT's offer many performance improvements for HPA design and can be attributed to a confluence of optimal material characteristics. GaN's high-breakdown voltage allows large drain voltages (>20 V) to be used, leading to high output impedance per watt of RF power. In addition, the high-electron mobility allows for increased power density per unit of gate periphery. Smaller gate geometry reduces capacitances per watt of output power. These two characteristics (high-breakdown voltage and electron mobility) couple resulting in easier matching and lower loss matching circuits, improving amplifier efficiency. The excellent thermal conductivity of both GaN and Silicon Carbide (SiC) substrates allows for reduced channel to case thermal resistance, simplifying thermal design. Table 1 highlight some of the critical properties of modern microwave semiconductor materials quantifying GaN's performance advantages [7]. In addition, GaN has been shown to be radiation tolerant to high fluences, making it an optimal choice for space-borne HPAs [8].

The two-stage HPA was designed using Sumitomo Electric Device Innovations (SEDI) space-qualified GaN HEMT technology. To achieve over 100 W output power out of the TRM, 120 W was required to be generated at the HPA to overcome front-end losses and driven by an 8 W GaN device. The 8 W GaN HEMT was unmatched in a compact MK-style package. To improve efficiency at high-output power, the 120 W was in an IV-package style, which combined two die with internal pre-matching networks and power combining.

The devices were optimized for power and efficiency through matching networks fabricated on a 50 mil Rogers TMM10i substrate. The networks were designed and characterized on a active load-pull system as presented in [9]. The transmitter was designed to operate with a maximum duty cycle of 12%, therefore to improve efficiency and reduce the contribution of noise during the receive window, both 8 and 120 W parts were DC switched. Due to the very large swath in the SweepSAR concept, the receivers have valid data 100% of the time, therefore the DC switching time between transmit and receive events needs to be minimized to less than 500 ns.

Matching network design—Three RF matching network boards (input, interstage, and output) were designed using SEDI reference designs, load-pull data, as well as RF design simulation tools. The first step was to migrate the existing SEDI reference designs in AD1000 ($\epsilon_r = 10.2$) to the TMM10i ($\epsilon_r = 9.8$) substrate. The SEDI reference designs contained four total matching network boards, an input / output for both of the 8 and 120 W parts. To reduce the total area, the output board of the 8 W part was combined with the input board of the 120 W part to form a single interstage matching board of the combined HPA. In addition, the SEDI reference designs contained additional tuning line lengths to accommodate frequency and performance tuning, these were removed to further reduce size. For the SEDI reference design, the test fixture length is 4.25 in for the 8 W and 3.25 in for the 120 W, totaling 7.5 in, while the JPL design is only 5.6 in long (Figure 1).

The simulated performance of these matching networks were compared against harmonic load-pull measurements to verify matching network performance. Active harmonic load-pull allows wide-band signals to be characterized under large-signal conditions, helping to optimize amplifier design [10]. Finally, in order to meet the fast DC drain switching time, the drain switching power MOSFETs were included on the

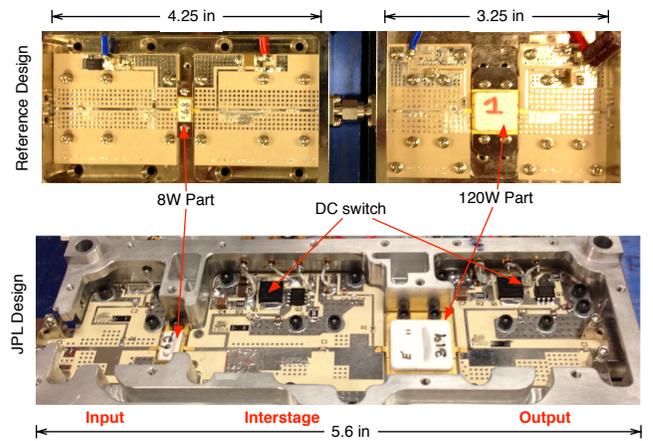


Figure 1. SEDI Reference design and JPL design comparison. (not to scale)

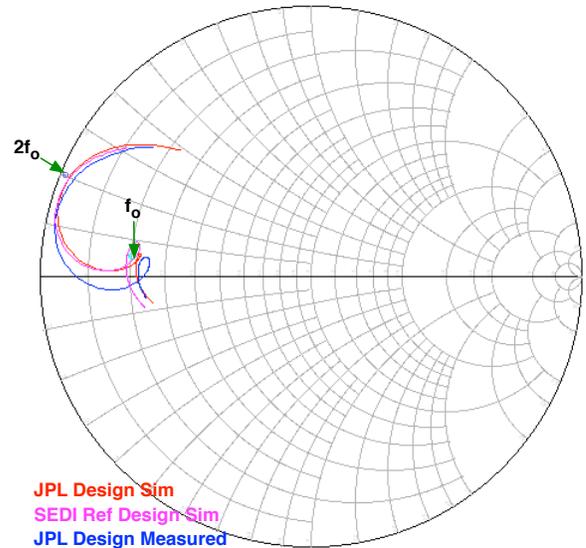


Figure 2. Impedance presented to 120 W part from output match terminated in 50Ω for JPL design (both simulated and measured) and the SEDI reference design.

interstage board on the 8 W drain bias line and the output board on the 120 W drain bias line.

Figure 2 plots the impedance presented to the 120 W device with the output terminated in 50Ω . Both designs, the critical RF matching elements were simulated using momentum EM simulator within Agilent's Advanced Design System (ADS) software. The JPL design and the SEDI reference design are in close agreement. In addition, the load-pull optimized impedances for the fundamental (1.25 GHz) and second harmonic (2.5 GHz) are also shown and to be in agreement with the matching network impedances.

The overall design was verified by implementing the SEDI provided models within ADS and simulating the full two-stage amplifier with the designed matching networks. The saturated output power was simulated to be above 50 dBm with the PAE greater than 65%. In addition, the power gain was simulated to be approximately 35 dB, reducing required drive power. Both second and third harmonics were simulated to be greater than 40 dBc.

Material	Mobility, $\mu, cm^2/V \cdot s$	Dielectric Constant, ϵ	Bandgap, E_g, eV	Breakdown, $E_b, 10^6 V/cm$	Conductivity, $k, W/cm \cdot C$
GaN	1500	9.5	3.4	2	1.3
4H-SiC	260	10	3.2	3.5	3.7
Si	1300	11.9	1.12	0.3	1.3
GaAs	5000	12.5	1.42	0.4	0.55

Table 1. Characteristics of Microwave Semiconductor Material

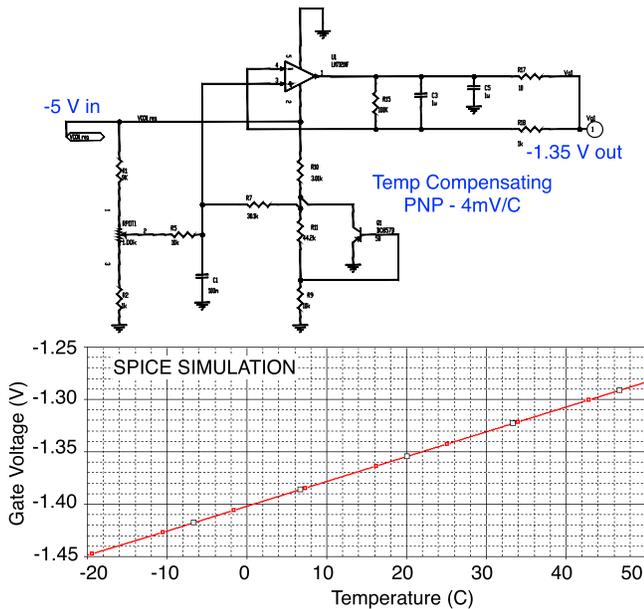


Figure 3. Gate bias circuitry for each of the GaN devices in the two stage amplifier.

DC board design—The final part of the electrical design of the HPA is the DC bias board. The bias board contained three major blocks: 1. gate bias generation, 2. drain switching circuit, and 3. gate dropout protection.

In order to properly bias GaN HEMT device gate voltage, the bias source must be able to drive both positive and negative currents as the device enters RF power saturation. In addition, in order to present stable operation over temperature, the gate voltage should be adjusted to compensate for performance shifts. An opamp circuit was used to regulate the voltage to the appropriate bias, approximately -1.35 V yielding 25 mA quiescent drain current for the 8 W device and 250 mA for the 120 W device. Figure 3 shows the opamp temperature compensating bias circuit and the SPICE simulation of the circuit over temperature.

The second critical part of the DC bias board is the high-speed drain switch. This circuit operates at PRF rates (3 kHz), switches 50 V signals at high current, and must have a switching time of less than 500 ns. Figure 4 shows the circuit schematic, the high-power FETs are on the RF matching network boards to reduce parasitics, which serves to limit transient voltages and currents during switching. A schmitt trigger inverter latches the enable signal to a MOSFET driver pair. The driver signals are AC coupled to the gate of the switching FETs. A zener diode in shunt with the gate of the switching FETs clamps the voltage to turn on the FET. To simplify the circuit design, an n-type device is used as the

bottom device to shunt the drain line to ground, while a p-type device is used to pull the device up to 50 V. Measurement of this circuit demonstrate switching speeds less than 200 ns. In addition, the switching circuitry topology acts as a duty cycle limiter, preventing it's use in CW mode.

The final DC circuit is the gate dropout protection switch. GaN HEMT devices are depletion mode, and require a negative gate voltage to turn them off. If the gate voltage is not applied with the drain voltage present, a large amount of current will flow in the device, potentially causing it to fail. This circuit monitors the input -5 V voltage (which supplies the gate bias) and ensures that if the voltage drops below -1 V, the drain voltage will shutoff preventing damage to the device, and will not propagate a failure in the TRM.

3. HPA MECHANICAL DESIGN

In addition to the electrical design, special care was taken in the mechanical design of the HPA chassis. The chassis was designed to have a DC cavity and an RF cavity to provide isolation between the two circuits with feedthroughs providing connections between two cavities. The 50 V supplied by the Energy Storage System (ESS) is delivered by a twisted shielded pair directly into the DC cavity where ground is connected to the HPA chassis. The regulated $+5$, -5 V, and the Tx enable are supplied by the digital interface board through another set of feedthroughs. The RF cavity and cover were designed to minimize the cavity's volume to prevent feedback and cavity resonances. In addition, EMI shielding was used on the cover to form a tight RF seal around the RF and DC cavities.

The requirement for passive thermal management relies on efficient use of thermal radiators to dissipate the waste heat generated by the electronics [11]. For the TRM, the back-surface of the chassis serves as the thermal radiator to space. In order to simplify fabrication, assembly, and test, the TRM was separated into four major components, Front-end Module (FEM), HPA, ESS and TRM main chassis. Figure 5 shows both the radiator side and the cavity side, with the HPA chassis colored in green. The HPA chassis has an extra lip that extends past the chassis housing area to increase the radiator area.

For the HPA chassis, in order to maintain low junction temperatures, the GaN parts were mounted directly to the back-surface of the radiator, therefore only 0.183 in of aluminum separates the GaN part (heat source) from radiator, thus minimizing the thermal resistance. Given nominal operating conditions, the HPA dissipates approximately 7 W of average DC power and the HPA-only radiator area is 5.9×5.7 in². The whole TRM area is 5.9×17 in² and nominally dissipates 11 W of DC power (excluding the HPA). Figure 6 shows the entire radiator surface with dimensions, the red box indicates the HPA chassis radiator area.

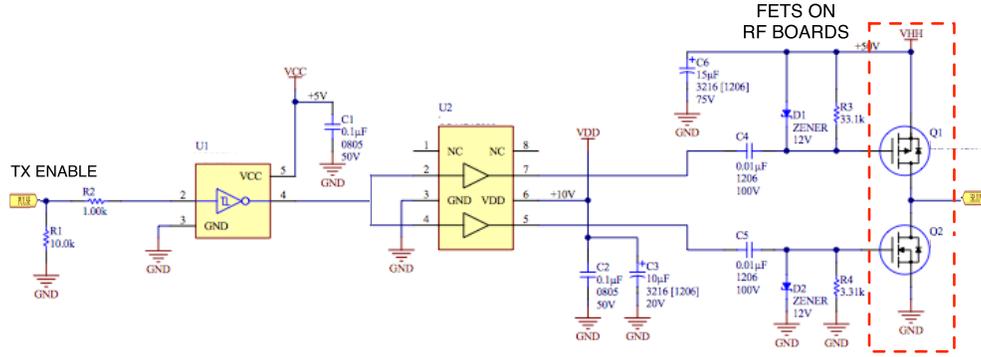


Figure 4. High-speed Drain switch for GaN devices. Switching FETs are located on RF matching boards, reducing parasitics and improving switching speeds while decreasing voltage and current transients.

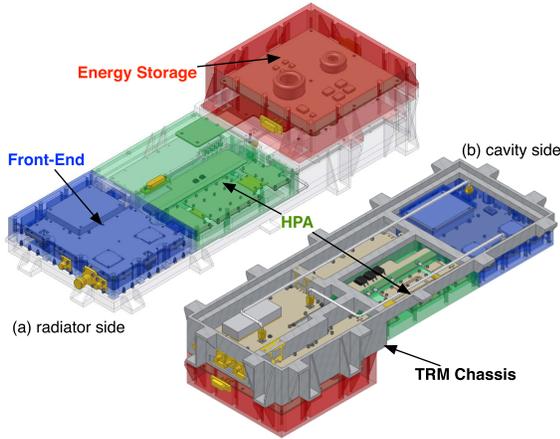


Figure 5. TRM Mechanical design showing both the (a) radiator and (b) cavity sides. The four major TRM components, Front-end Module (FEM), HPA, Energy storage system (ESS), and TRM chassis are also highlighted.

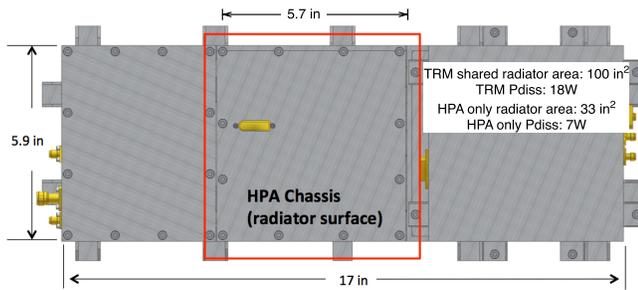


Figure 6. View of TRM from radiator surface showing radiator dimensions for the TRM and the HPA chassis.

A simple analysis was performed to determine the radiator temperature given the power dissipation of the TRM. Equation. 1 was used to calculate the radiator temperature where Q_{diss} waste heat generated by the electronics, S_{sun} is the solar constant (1350 W/m^2), α_s is solar absorptance (0.15), f is the solar view factor (0.2), A is the radiator area, σ is the Stefan-Boltzmann constant, ϵ is the emissivity (0.8), and T_{space} is the temperature of deep space (4K).

$$T_{radiator} = \sqrt[4]{\frac{Q_{diss} + S_{sun} \cdot \alpha_s \cdot f \cdot A}{\sigma \cdot (1 - f) \cdot \epsilon \cdot A} + T_{space}^4} \quad (1)$$

Using this equation, nominal operating powers, radiator sizes, and view factor assumptions, Fig 7 shows the temperature contours as a function of dissipated power and radiator area. For the HPA only, the radiator temperature is above the allowable flight temperature (40°C), while the TRM only temperature is 30°C . Therefore, conduction from the HPA to the TRM chassis radiator is necessary to distribute the heat out of the the HPA chassis. For the case of both the TRM and HPA shared radiator area, the total temperature will approximately be 35°C . This equation assumes a simplified worst-case model for the solar view factor, full thermal orbital analysis has been performed and shows that the TRMs temperatures are below this calculation, however, it is still useful to understand the necessary radiator area sharing between the various sub-assemblies in the TRM.

4. MEASURED RESULTS

During the HPA assembly process, the various components were tested and verified at different stages to ensure proper operation and performance. Figure 8 highlights the test procedure used to assemble and test the HPA. First step after RF board assembly was to perform S-parameters tests to compare and tune in order to match simulation results (Figure 2). The next step is to integrate the three RF boards and GaN onto a test fixture blocks to measure RF large-signal performance using the active-load pull system. The third step is to integrate these boards into the HPA chassis and remeasure large-signal performance to characterize any cavity related effects. In parallel, the DC board was assembled and tested. Once the RF and DC boards were separately tested, the final step is to integrate all of the boards the chassis and fully characterize the HPA over thermal ambient conditions.

Power performance in ambient conditions

To verify the initial performance of the HPA, the RF boards were tested in the chassis using the mixed-signal active load-pull system as described in [9]. The load-impedance was varied around 50Ω , measuring the output power and efficiency. Figure 9 plots the power (red) and PAE (blue) contours on a smith chart at 3 dB gain compression operating at 1.25 GHz (band center). The contours are lines of constant

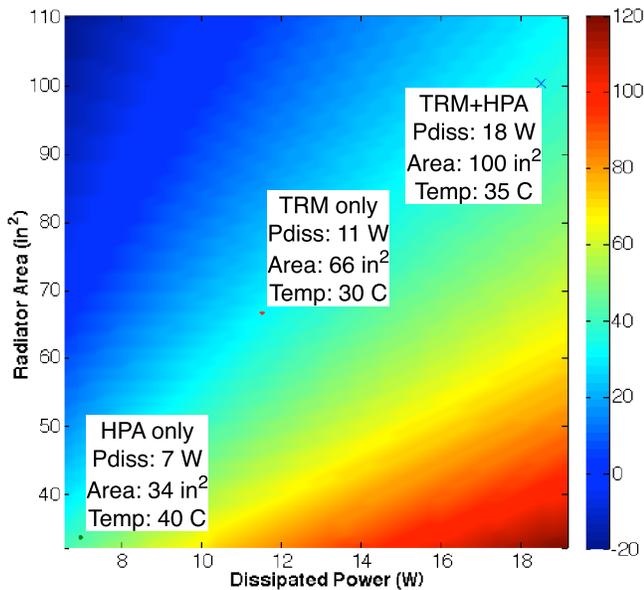


Figure 7. Radiator Temperature as a function of dissipated power and radiator area. HPA only, TRM only, and shared TRM + HPA conditions are highlighted on plot showing the need for thermal sharing between TRM and HPA chassis.

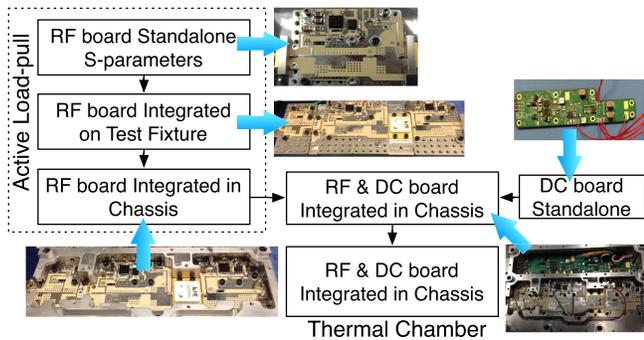


Figure 8. Assembly and test procedure for GaN HPA module assembly. The procedure characterizes individual RF and DC boards and then integrates them into a test fixture, and finally the chassis.

power (or PAE) across those given impedances. For instance, 50Ω is between the 51.2 and 51.4 dBm power contours and 60 to 61 % PAE contours, demonstrating the device appears to be well power matched while achieving optimal efficiency. Also, the flatness of the power contours will result in the HPA power and PAE varying a small amount, less than 1.6 dB for 1.5:1 mismatched load conditions.

In addition to power contours, the swept power response was measured on the load-pull system. Figure 10 plots the output power and PAE as a function of input power for both simulation and measurement. The simulation and measurement track very closely, with only a 10% difference in PAE, this is mostly attributable to losses and parasitics that tend to be difficult to model within the simulation.

Once the DC and RF boards were integrated into the HPA chassis, both pulsed CW and chirped large-signal waveforms (40 MHz) were characterized on the integrated HPA assembly. The DC-to-RF timing was optimized to account for

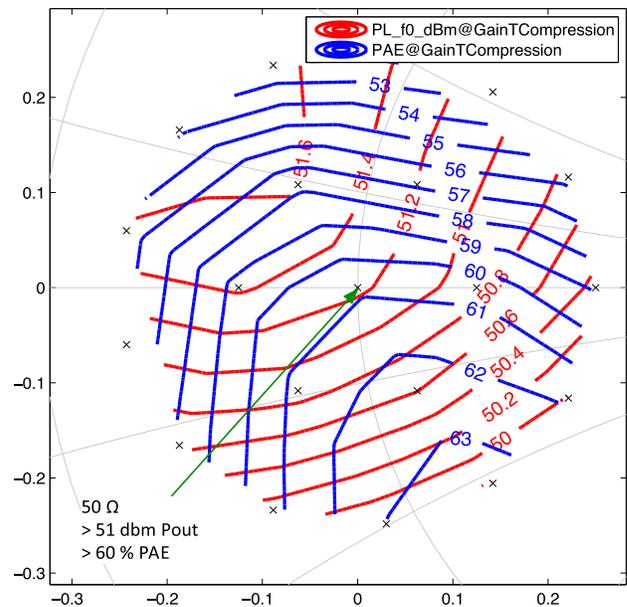


Figure 9. Power and PAE contours of HPA output at 1.25 GHz in 3 dB gain compression.

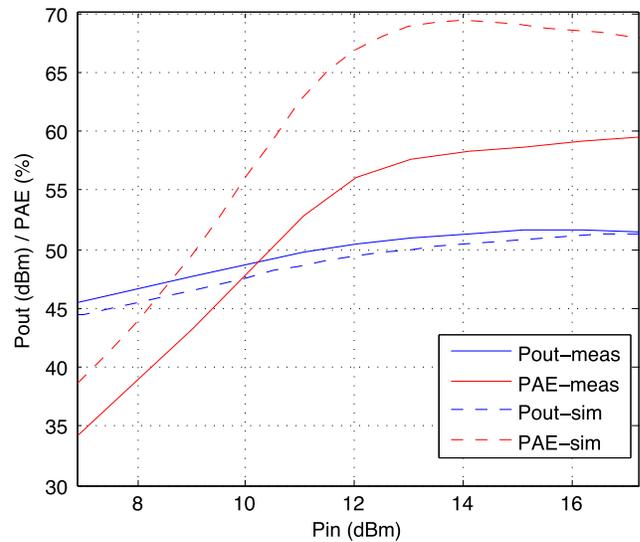


Figure 10. Measured and simulated output power and PAE as a function of input power at 1.25 GHz for the HPA.

system delays and to ensure that the DC drain switch applied bias to the GaN devices before the RF pulse was triggered and removed the bias just after the RF pulse finished. The timing was controlled through a master pulse generator that allows for coherent individual pulses of varying delay and width to synchronously trigger the equipment and HPA.

Performance over temperature

The tests were conducted in thermal ambient environments using the setup shown in Figure 11. All measurements were automated with measurements repeating over set intervals to capture trends during temperature ramp and soaking. The RF power was calibrated to the input and output of the HPA assembly with the front-end module used as the load

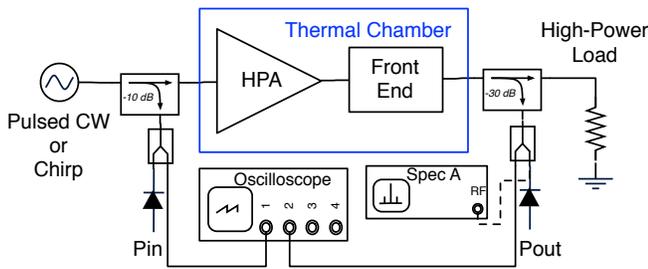


Figure 11. Measurement setup for testing the HPA in pulsed CW or chirp configurations. Both scalar power measurements were taken as well as input and output waveforms were digitized to perform amplitude and phase measurements.

and deembedded from the measured results. A digitizing oscilloscope was used to capture input and output waveforms to extract amplitude and phase variation. For the pulsed CW measurements, input power was swept at each frequency to determine optimal gain compression point with the measurement repeating approximately every 60 seconds. In addition to measuring the output power, the spectral content was measured using a spectrum analyzer to determine the power levels at the harmonics. The pulsed chirp measurement setup was similar to the pulsed CW setup except a fixed power level was used and data was recorded every 30 seconds.

The thermal ambient temperature profile is shown in Figure 12, which plots the chamber temperature (in blue) and the GaN device package temperature in green. The temperature rise of the GaN part above the chamber temperature is approximately 5°C . Given the channel to case thermal resistance of $0.85^{\circ}\text{C}/\text{w}$, and an DC power of approximately 16 W, the channel temperature is approximately 14°C above case temperature. For worst case qualification temperature of 60°C , the maximum channel temperature should be no more than 80°C , which is well under the maximum derated channel temperature of 125°C .

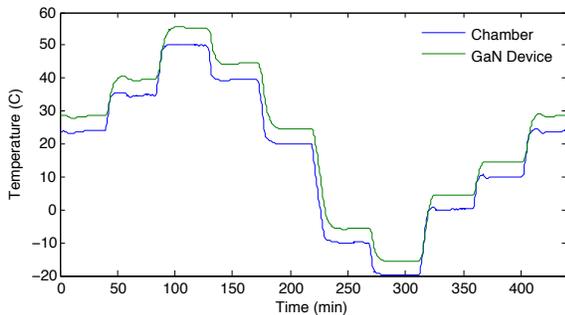


Figure 12. Temperature profile used to characterize the HPA module. The GaN device package was measured to have a 5°C rise over chamber temperature.

Figure 13 plots the output power and PAE over temperature from 50°C to -20°C of the pulsed CW waveform for three different frequencies. The chirp length was $50\ \mu\text{s}$ with a 2 kHz pulse repetition frequency (PRF) with the input power set to 16.5 dBm. The output power variation per tone is less than 0.2 dB, while the variation across the frequency range is $\pm 0.5\ \text{dB}$. The PAE is measured to be approximately 60% over temperature for all frequencies. The rise and fall time of the RF waveform was measured to be less than 10 ns, with a settling time of 200 ns.

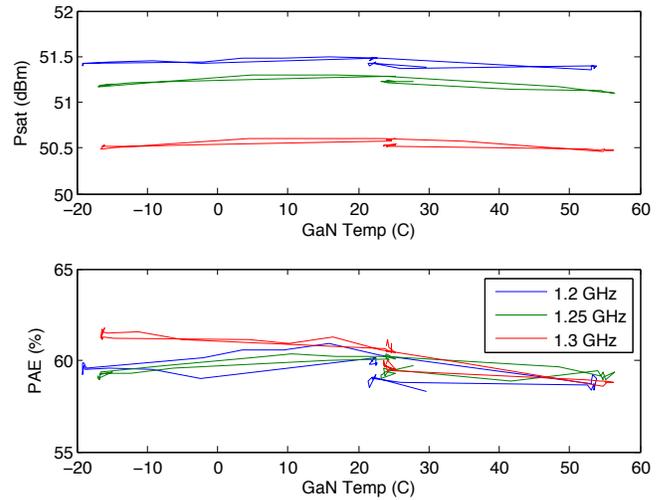


Figure 13. Saturated power and power-added efficiency over a base-plate temperature of (-20°C to $+50^{\circ}\text{C}$). Measurement was performed at three different pulsed CW frequencies. The variation over temperature is less than 0.2 dB while the frequency variation is less than $\pm 0.5\ \text{dB}$.

The stability over temperature of the HPA is derived from both compressed operation as well as gate bias tuning to compensate for the performance changes over temperature. Under compressed operation, output power does not respond to variations in input power. Figure 14 plots the slope of the output power versus input power. At low input powers, the slope is one, meaning that a 1 dB change in input power corresponds to a 1 dB change in output power. However, at 3 dB compression, the slope is nearly zero over a 2-3 dB change in input power. Therefore, the HPA is insensitive to gain variations in pre-amplifier stages improving output power stability.

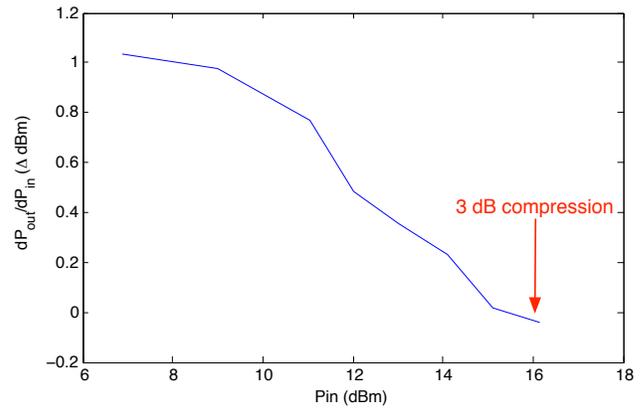


Figure 14. Slope of output to input power as a function of input power, highlighting under compression output power is insensitive to input power.

While compressed operation allows the HPA to be immune to gain variation in the preceding stages, in order to stabilize the gain of the HPA itself, temperature compensation circuitry is necessary to account for bias shifts in the device. As mentioned in section 2, the gate bias circuitry included temperature compensation to allow the gate voltage to track changes in temperature. By adjusting the gate voltage over temperature, the average drain current was measured to vary less than 10 mA ($< 2\%$), which in turn stabilizes the gain and output power of the HPA.

Harmonic and time domain performance

A key advantage of using GaN HEMT technology is ability to maintain high peak output power at high efficiency at harmonic terminated amplifier modes. By using the active harmonic load-pull system, matching networks can be designed to reject harmonics at the output, which eliminates the need for an output filter to control out of band spectra. Figure 15 plots the measured output spectrum of the TRM (including the front-end module) with the NTIA spectral mask [12] plotted in red. Taking the antenna rejection (show in green at the harmonics) into account, the TRM output meets the spectral mask for the second and third harmonic frequencies. There is a slight violation around 200 MHz, which is due to the video feedthrough from the DC switching. This leakage can be reduced by not switching the 8 W part or staggering the 8 W and 100 W turn on times, which will be investigated in future designs of the DC board, but should have little effect on the RF performance. The DC switching time may increase, but still can be maintained within the turn on time requirement.

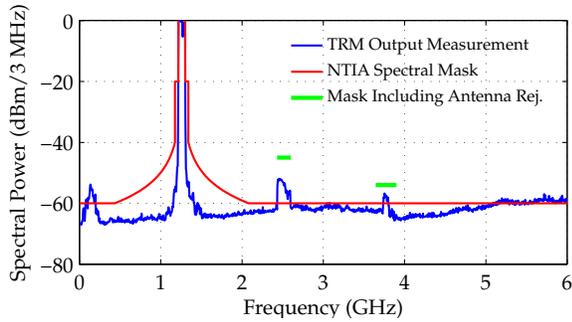


Figure 15. TRM output spectrum with overlay of NTIA spectral mask

To accurately characterize the HPA, the effects of the power regulator (ESS) should be taken into account. The ESS is a switched supply DC-DC converter that scales the proposed spacecraft bus voltage of 70 V to the voltages required by the TRM, including the pulsed current 50 V DC supplying the HPA. The ESS was developed at JPL and achieves very high-conversion efficiencies (approaching 90%). As the HPA is pulsed, the energy from the capacitor banks are drained leading to a potential droop on the 50 V HPA supply. Longer transmit pulses could cause a larger droop resulting in a significant impact on variation of the signal over the pulse. Increasing the size of the capacitor bank as well as minimizing the parasitic inductance between the ESS and HPA will help minimize the droop. Figure 16 is a screenshot from the high-speed oscilloscope capturing the RF input and output waveforms, an FFT of the output waveform, the ESS current as well as the 50 V pulsed drain of the 120 W GaN HEMT device. The input signal is a 40 μ s, 40 MHz linear ‘up’ chirp. The voltage droop at the GaN device was measured to be approximately 2.4 V, this combines with the frequency response of the HPA to have a total droop of just over 1.1 dB.

To isolate the effects of the ESS from the HPA frequency response, a CW pulse and ‘down’ chirp were measured as shown in Figure 17. The CW pulse at the center of the band shows a total droop of approximately 1 dB, which can be attributed to the droop in the ESS voltage. The 40 MHz ‘down’ chirp acts to cancel the power droop due to the ESS since the HPA’s output power is higher at lower frequencies, which translates into an overall power droop of less than 0.3 dB.

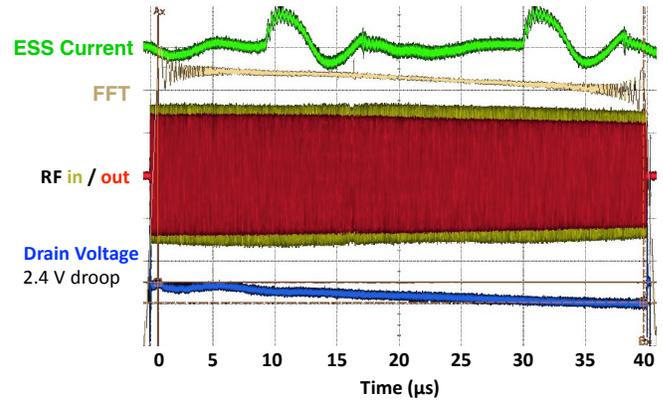


Figure 16. Oscilloscope screenshot of RF input and output waveforms of a 40 μ s 40 MHz linear ‘up’ chirp along with the pulse DC voltage, ESS current, and FFT of the output waveform.

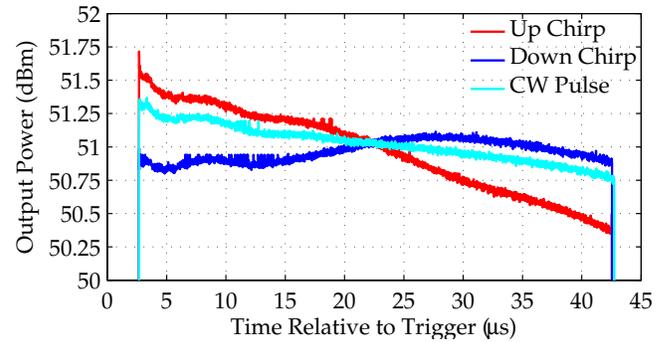


Figure 17. Output power of CW pulse, up, and down chirps that demonstrates the effects of ESS voltage droop as well as combined HPA frequency response. By optimizing the transmitted waveform by using a down chirp, the variation in the pulse magnitude can be reduced to less than 0.3 dB.

Comparison to state-of-the-art

This work was compared to other state-of-the-art amplifiers in Table 4. This amplifier has the highest gain, while still maintaining high-efficiency and output power. In order to compare the overall performance in a relevant TRM environment, the efficiency of the driver stages should be also taken into account. Assuming linear driver stages of 12% efficiency, the overall transmit efficiency can be calculated. With the high-gain of the amplifier reported in this work, the change in efficiency is negligible, however, with other lower gain HPAs, the overall transmit efficiency is reduced. The improvement is due to the need for only lower power driver amplifiers, thus consuming less DC power as well as reducing the overall number of gain stages needed before the HPA.

	P_{out}	G	f_c	PAE	Transmit Efficiency
	dBm	dB	GHz	%	%
this work	51	34.5	1.25	58	58
[13]	47.6	15	1.191	68	58
[14]	51.5	12.5	1.25	60	49
[15]	51.7	15	2.1	54	48
[16]	50	10.5	3.8	64	46

Table 2. Comparison of GaN HPAs targeting space applications.

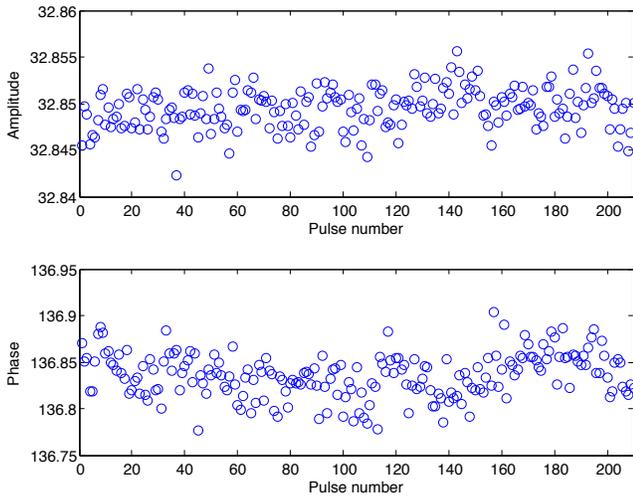


Figure 18. Extracted amplitude and phase at the peak of the compressed chirp for 210 consecutive pulses of a 40 μ s, 40 MHz linear ‘up’ - chirp at room temperature.

5. PULSED AMPLITUDE AND PHASE ANALYSIS

For the 40 μ s, 40 MHz linear chirp waveform pulsed at a PRF of 2 KHz, 210 consecutive pulses (approximately 100 ms of data, limited by memory depth of oscilloscope) of the input and output waveforms were digitized at 10 GSPS using a high-speed oscilloscope across temperature. Each data acquisition was performed in 30 second intervals. The waveforms were processed using a matched filtering algorithm extracting the amplitude and phase at the peak of the compressed chirp signal over temperature using a methodology discussed in [17].

Analyzing the 200 consecutive pulses, approximately 0.01 dB amplitude and 0.1 $^\circ$ phase variations were demonstrated at room temperature (Figure 18). The variations in the amplitude and phase over the 210 consecutive pulses do not appear strongly correlated and likely the results of random noise.

To analyze the amplitude and phase change over temperature, the mean of the 210 pulses were computed at each data acquisition across the thermal cycle. Figure 19 shows a very stable 0.2 dB change in amplitude and 2 $^\circ$ change in phase from -20 $^\circ$ C to +50 $^\circ$ C temperature range. The blue circle data points show areas where the chamber has achieved thermal stability during a ‘soak’ cycle, while the green dashed line are areas of temperature ramp, which was set to 3 $^\circ$ C/min.

The amplitude variation correlates with the measured change in output power as expected, however, analyzing the phase during the thermal ‘soak’, a large change in phase is measured for a fixed chamber temperature. This unexpected behavior appears to be due to thermal gradients in the HPA as it achieves thermal equilibrium. This effect is demonstrated in Figure 20, which plots the temperature difference between the GaN device package and the chamber temperature as well as the compressed chirp phase over time for the full temperature cycle. There is a slight thermal lag between the temperature of the GaN device and the chamber as evidenced by the spikes in the temperature difference. These temperature spikes appear to be correlated to spikes in the phase of the output waveform. Typically in space, the instruments will

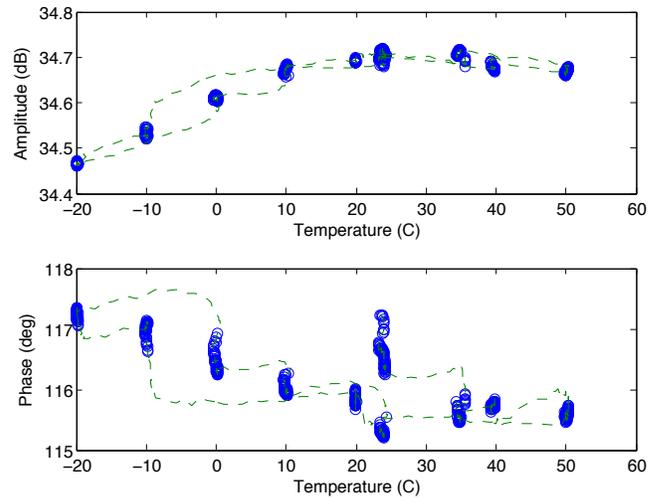


Figure 19. Amplitude and phase of a compressed 40 MHz chirp across temperature, showing less than 0.2 dB variation in amplitude with less than 2 $^\circ$ change in phase.

experience ramp rates of much less than (3 $^\circ$ C/min) so the thermal gradients in the HPA will be smaller, reducing any phase variations.

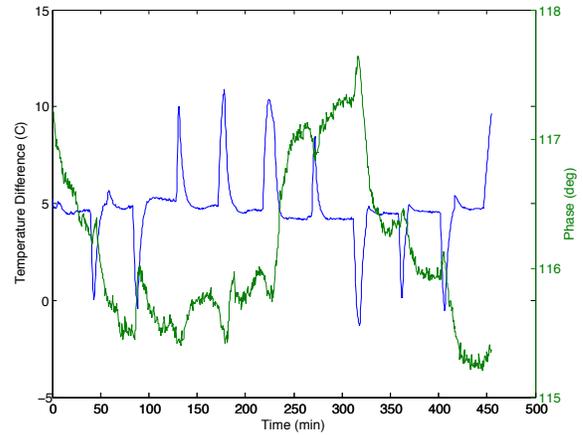


Figure 20. Temperature difference of GaN device package and temperature chamber overlaying phase of compressed chirp as a function of time during the thermal cycle. The spikes in temperature represent the thermal lag between the HPA and the chamber reaching equilibrium and correlate to phase variations of the compressed chirp.

Key metrics to determine the quality of SAR images are the integrated and peak sidelobe level ratios (ISLR and PSLR) after compressing the waveform. These ratios help quantify any distortions of the chirp signal that deviate from the ideal impulse response. A low ISLR and PSLR could be caused by changes in group delay, non-linear phase response, as well as large amplitude variations. For this analysis, the ISLR and PSLR were calculated as discussed in [18] are presented in Figure 21. Both the mean ISLR and PSLR (over the 210 pulses) is above 33 dB and 25 dB respectively over temperature, which indicates that the HPA has minor impacts to the quality of the chirp signal. In addition, the flat response of these metrics indicate that the compressed waveform is relatively insensitive to temperature variations, which can greatly ease calibration requirements.

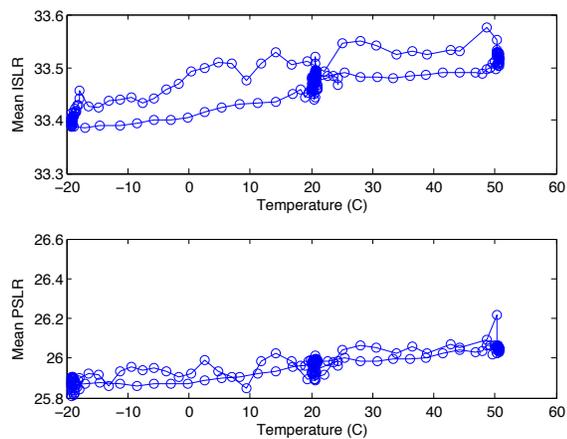


Figure 21. Integrated and peak sidelobe level ratio for compressed chirp at output of the HPA as a function of temperature.

6. SUMMARY

This work presents the design and measured results of a two-stage GaN HEMT based HPA for use in an interferometric L-band SweepSAR mission. GaN HEMT devices are a mission enabling technology, offering high peak output power and efficiencies. The output power of the HPA was over 51 dBm at 60% PAE with over 34 dB of power gain. This design focused on a thermally stable design, ensuring high-quality science data as demonstrated by less than a 0.2 dB change in output power over 70°C temperature range. Electrically, the design was stabilized through compressed operation in addition to bias compensation circuitry. Also, the mechanical design was optimized to make efficient use of thermal radiators to dissipate waste heat.

The HPA was characterized using a realistic radar waveform of a wideband chirp over temperature. This signal was analyzed to extract the amplitude and phase of the compressed chirp using a matched filtering algorithm. This analysis demonstrates that with these expected radar signals, less than 2° phase change should allow very stable operational and ensure accurate interferometric signal processing, helping to fulfill the science goals of this proposed mission.

ACKNOWLEDGMENT

This work is supported by the NASA Earth Radar Mission task at the Jet Propulsion Laboratory, California Institute of Technology, under a contract with the National Aeronautics and Space Administration.

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BIOGRAPHY



Tushar Thrivikraman is an RF engineer at the Jet Propulsion Lab at the California Institute of Technology in the Radar Science and Engineering section where he has focused on the development of RF hardware for air- and spaceborne SAR systems. He received his PhD in Electrical and Computer Engineering from the Georgia Institute of Technology in 2010. His research under Dr. John

Cressler in the SiGe Devices and Circuits Research Group at Georgia Tech focused on SiGe BiCMOS radar front-ends for extreme environment applications.



Stephen Horst Stephen Horst received a B.S.E.E. degree from The Ohio State University in 2004, and an M.S.E.E. and Ph.D. from the Georgia Institute of Technology in 2006 and 2011 respectively. His Ph.D. dissertation involved radiation-hardening-by-design on SiGe mixed-signal integrated circuits. He has co-authored over 25 papers in peer-reviewed venues, and a book chapter in

Extreme Environment Electronics. He is currently a member of the Radar Science and Engineering section at the Jet Propulsion Laboratory developing T/R modules for future SweepSAR missions.



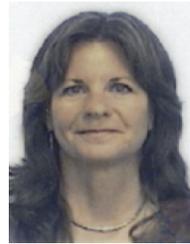
Douglas Price Douglas Price is the RF radar electronics group supervisor in the radar science and engineering section at the Jet Propulsion Laboratory. He has over 29 years of experience in the design, fabrication, assembly and testing of RF/Microwave/Millimeter wave telecom and radar electronics hardware and currently the cognizant engineer of the L-band SweepSAR RF electronics

subsystem. He received his MSEE from the University of Southern California in 2003.



James Hoffman is a Senior Engineer in the Radar Technology Development Group at JPL. He received his BSEE from the University of Buffalo, followed by MSEE and PhD from Georgia Tech in planetary remote sensing. He has worked in the design of instruments for remote sensing applications for more than 10 years. In previous technology

development tasks, he successfully developed a new low power digital chirp generator, which has been integrated into several radar flight instruments. He has experience designing radar systems for both technology development and space flight hardware development, and is currently the RF lead for the proposed DESDynI radar instrument.



Louise Veilleux Louise Veilleux received a B.S.E.E from University of Maine, Orono in 1979, and a M.S.E.E from MIT in 1982. She has been with JPL for more than 25 years in the Radar Science and Engineering Section. She developed radar flight hardware for SIR-B, SIR-C, and SRTM SARs, was involved in the formulation and development of NScat, SeaWinds, and Aquarius Scatterometers, as well as the SMAP (and precursor HYDROS) and SWOT (and precursor WSOA) Earth-observing radars

currently under development.