

# SMAP's Radar OBP Algorithm Development

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**Abstract** – An approach for algorithm specifications and development is described for SMAP's radar onboard processor with multi-stage demodulation and decimation bandpass digital filter. Point target simulation is used to verify and validate the filter design with the usual radar performance parameters. Preliminary FPGA implementation is also discussed.

## I. INTRODUCTION

Soil Moisture Active-Passive (SMAP) mission is the successor of the HYDROS mission concept [1] shown in Fig.1. The scientific objectives of the project are to provide frequent and global maps of the Earth's surface soil moisture and surface freeze/thaw state every 2-3 days, for weather and climate prediction, water, energy and carbon cycle studies, natural hazards monitoring, and national security applications. The mission requirements and system design were described in [2] and the radiometer/radar instrument design was illustrated in [3]. To obtain adequate spatial resolution while proving wide swath measurement for global 3-day refresh time, SMAP employs a conical rotating reflector antenna as shown in Fig. 2.

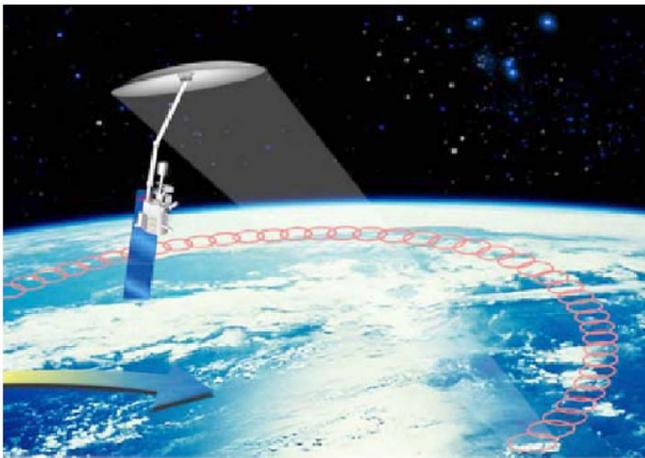


Fig. 1: Artist drawing of HYDROS mission in orbit.

While the radiometer resolution is determined by the real antenna footprint, the radar resolution comprises of two modes: (a) "low-res" which is similar to radiometer resolution and (b) "high-res" which employs range-Doppler discrimination [3]. This paper will describe the algorithm for the radar onboard processor (OBP) which is supposed to turn raw data into low-res and high-res data ready to be down-linked for further ground processing into low-res and high-res radar products.

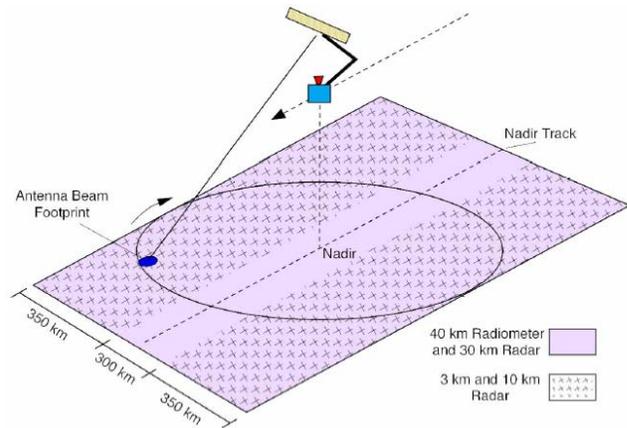


Fig 2: Conical scanning reflector configuration showing radiometer swath, and high- and low-resolution radar swaths.

## II. ALGORITHM DESCRIPTIONS

Fig. 3 displays the frequency characteristics of the digital offset-video (real) signal sampled by the ADC at 60 MHz. Each of the physical receiver channels (H-pol and V-pol receivers) contains three 1 MHz subbands corresponding to the co-pol, noise, and x-pol signals. The OBP is equivalent to a demodulation decimating bandpass channelizer (DDBC) which moves each of the subbands to baseband, filters it out to remove out-of-band interference, and decimates it to yield a complex (I/Q) output data rate of 1.2 MHz.

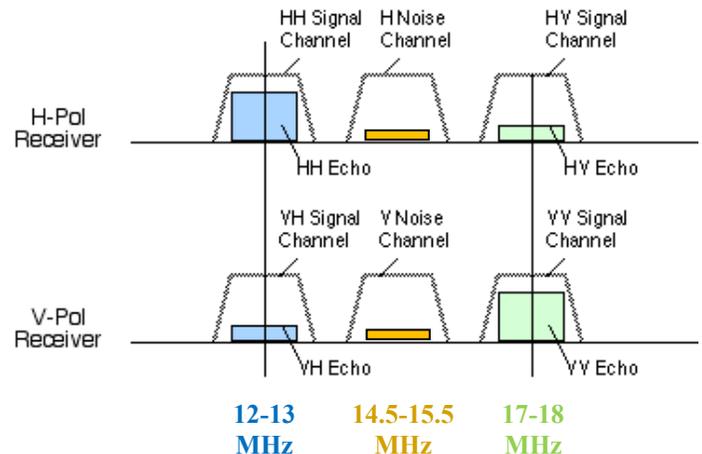


Fig. 3: Digital offset-video co-pol, noise, and x-pol signals.

The DDBC output is further processed and organized into three data categories: (a) high-rate data which undergo 12:4

BFPQ conversion; (b) low-rate data which are constructed by squaring samples, averaging over 10 range bins, integrating average range bins over 15 msec, and outputting a 16-bit sum; and (c) low-rate noise-only data which are obtained by squaring samples, averaging over 15 msec, and outputting a 16-bit sum. This process is summarized in Fig. 4.

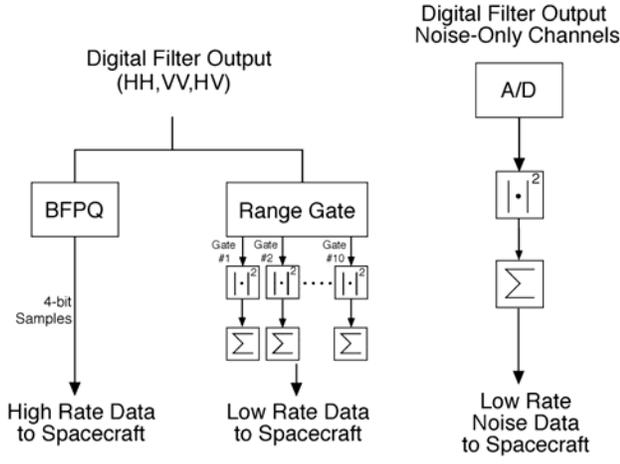


Fig. 4: Three different data modes after DDBC.

The block diagram of the DDBC is shown in Fig. 5. It consists of a quadrature modulation (QM) to move each of the subbands to baseband and a multi-stage decimation filter (DF) to reduce the sample rate from 60 MHz to 1.2 MHz. The latter composes of three decimation stages (Fig. 6) for a total decimation ratio of  $5 \times 5 \times 2 = 50$ . This is quite a substantial data rate reduction which justifies the multi-stage decimation consideration, since a single-stage design will have a long filter length which leads to numerical instability during the filter design process and large finite-wordlength error during hardware implementation [4].

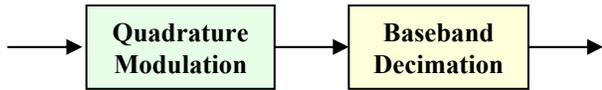


Fig. 5: Demodulating decimation bandpass channelizer.

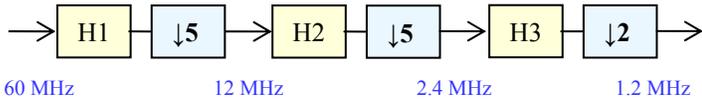


Fig. 6: Multi-stage decimation filter.

### III. FILTER DESIGN

There are many types of filters considered for decimation filtering, such as window, equiripple, maxflat, Lagrange-multiplier, cascaded-integrator-comb designs [5]. Here, the equiripple technique is chosen for illustration purpose. The optimal trade-off between different filter types and their performances will be reported in the future.

When a signal  $x[n]$  is decimated by a factor of  $M$ , its frequency spectrum is given by

$$y[n] = x[Mn]$$

$$Y(e^{j\omega}) = \frac{1}{M} \sum_{k=0}^{M-1} X(e^{j(\omega - 2\pi k)/M}) \quad (1)$$

where  $X(e^{j\omega})$  is the frequency spectrum of  $x[n]$ . Thus,  $Y(e^{j\omega})$  is the sum of  $M$  copies of  $X(e^{j\omega})$ , each stretched by  $M$  and shifted by  $2\pi k$ ,  $k = 0, 1, \dots, M-1$ . In order to avoid aliasing, a filter with normalized cutoff frequency  $\omega_s = 2\pi f_s$  around  $\pi/M$  is needed as shown in Fig. 7.

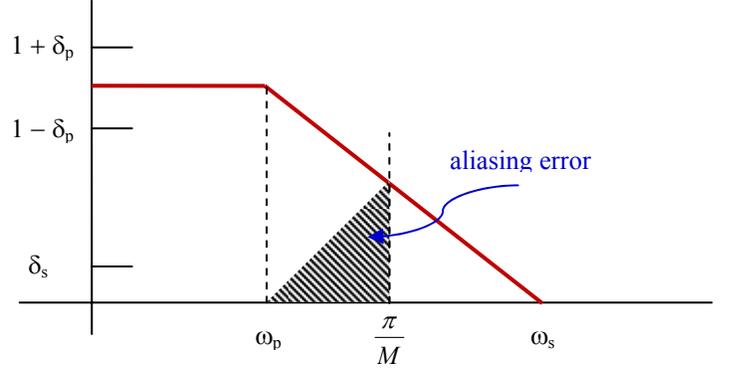


Fig. 7: Decimation filter specifications with passband  $\omega_p$ , stopband  $\omega_s$ , passband ripple  $\delta_p$ , and stopband ripple  $\delta_s$ .

The filter length is given by

$$N = \frac{-20 \log_{10}(\sqrt{\delta_p \delta_s}) - 13}{14.6(\omega_p - \omega_s)/(2\pi)} \quad (2)$$

In a multi-stage decimation design, the individual stage specifications are illustrated in Fig. 8 and related to the overall specifications  $(f_p, f_s, \delta_p, \delta_s)$  as

$$f_{pi} = f_p; \quad f_{si} = F_i - f_s$$

$$\delta_{pi} = \delta_p / M; \quad \delta_{si} = \delta_s \quad (3)$$

where  $F_{si}$  is the decimated output sampling rate of each stage.

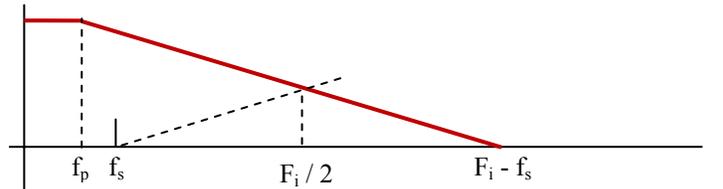


Fig. 8: Individual stage specifications in a multi-stage design.

Since SMAP's subband signals have a bandwidth of 1 MHz with a decimated sampling rate of 1.2 MHz, let  $(f_p, f_s, \delta_p, \delta_s) = (0.5 \text{ MHz}, 0.6 \text{ MHz}, 0.1 \text{ dB}, -40 \text{ dB})$  be the specifications for the overall decimation. Using the popular Remez exchange algorithm, the impulse and frequency responses of the three decimation filters H1, H2, and H3 in a

multi-stage design of Fig. 6 are shown in Fig. 9. Their lengths are (15,20,50) with a passband ripple smaller than 0.1 dB and stopband attenuation around -60 dB. Fig. 10 displays the equivalent response of the multi-stage implementation and compares with a single-stage design.

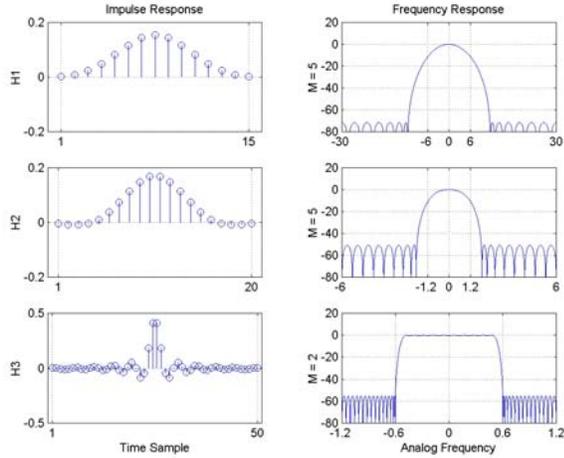


Fig. 9: Impulse (left) and frequency responses (right) of individual decimation filters.

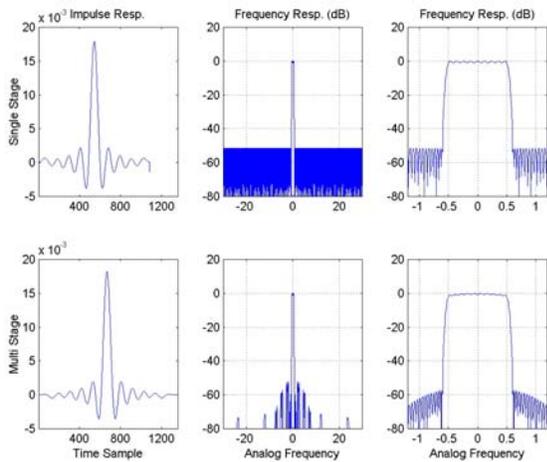


Fig. 10: Impulse (left) and frequency (right) responses of single- (top) and multi- (bottom) stage decimation designs.

#### IV. POINT TARGET SIMULATION

Fig. 11A illustrates a baseband reference chirp having a duration of 45  $\mu$ sec and a bandwidth of 1 MHz. The chirp is sampled at 1.2 MHz. Fig. 11B simulates a received echo from the transmitted chirp in Fig 11A, this time sampled at 60 MHz. There are two point targets situated at the beginning and end of a swath width having a duration of 117  $\mu$ sec. The two point targets have a magnitude difference of 6 dB. Fig. 11C shows an up-converted version of Fig. 11B with a modulation frequency of 12.5 MHz. This represents the co-pol receive channel with a gain of 0 dB. Fig. 11D displays the simulated x-pol receive channel at a modulation frequency of 17.5 MHz, and with a magnitude of -25 dB down as compared with the co-pol channel. This magnitude

attenuation represents the minimum echo expected during the mission. Random Gaussian noise with a magnitude of -35 dB is added in Fig. 11E to simulate the RF front-end thermal noise. All the signals are added and scaled to a quarter of the ADC's full-scale voltage, shown in Fig. 11F.

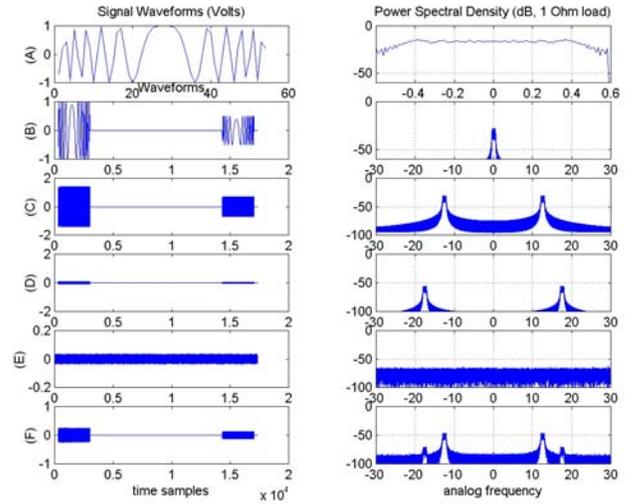


Fig. 11: Simulated signals (left) and their spectra (right): (A) baseband chirp sampled at 1.2 MHz; (B) 2 targets at beginning and end of swath, sampled at 60 MHz; (C) co-pol channel centered at 12.5 MHz; (D) x-pol channel centered at 17.5 MHz; (E) front-end thermal noise; and (F) total echo scaled to 1/4 of ADC's full-scale voltage.

#### V. FILTER OUTPUT AND PERFORMANCE VERIFICATION

Fig. 12 compares the reference chirp and the outputs of the multi-stage decimation filter for the first target in Figs. 11C and 11D. These signals are sampled at a Nyquist rate of 1.2 MHz, commensurable with the chirp bandwidth of 1 MHz. The co-pol output (Fig. 12B) is very close to the reference signal while the x-pol output (Fig. 12C) shows slight degradation due to its small signal-to-noise ratio (-25 dB).

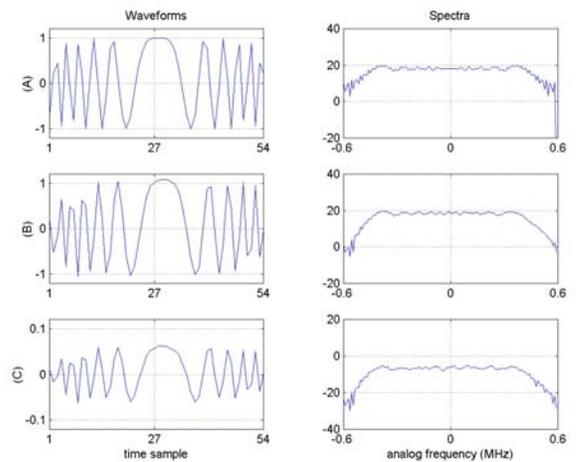


Fig. 12: Chirps (left) and their spectra (right): (A) reference; (B) co-pol channel output; (C) x-pol channel output.

Preliminary performance verification was done by applying pulse compression to the chirp signals of Fig. 12 with the result shown in Fig. 13. Three radar parameters are

considered for performance assessment: the peak sidelobe ratio (PSLR), the integrated sidelobe ratio (ISLR), and the pulse broadening factor (PBF). Their measures for the reference, co-pol and x-pol outputs of Fig. 13 are (PSLR, ISLR, PBF) = (-34 dB, -26 dB, 1.0), (-30.6 dB, -24.4 dB, 1.06), and (-27.1 dB, -22.2 dB, 1.06), respectively. These values compare favorably with the usual requirement of (-25 dB, -20 dB, 1.10).

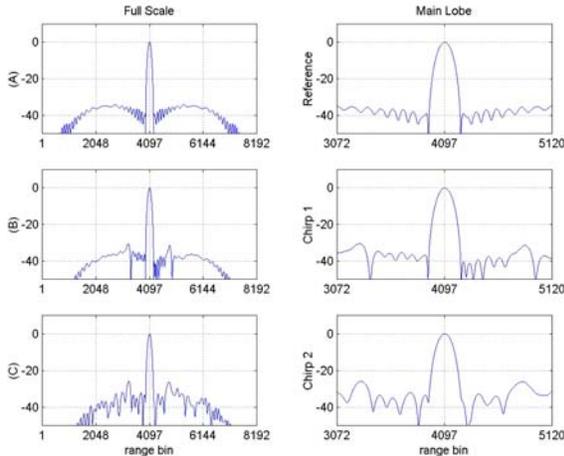


Fig. 13: Full-scale (left) and main-lobe (right) pulse compression outputs: (A) reference; (B) co-pol; (C) x-pol.

Lastly, the pulse compression output of the return echo for an entire swath of Fig. 11 is shown in Fig. 14. Note that the magnitude of the x-pol channel (Fig 14C) is -25 dB down compared to that of the co-pol channel (Fig. 14B), and that the magnitude difference between the two targets within a swath of a receive channel is 6 dB. This result validates the filter sensitivity to the expected dynamic range of input variation.

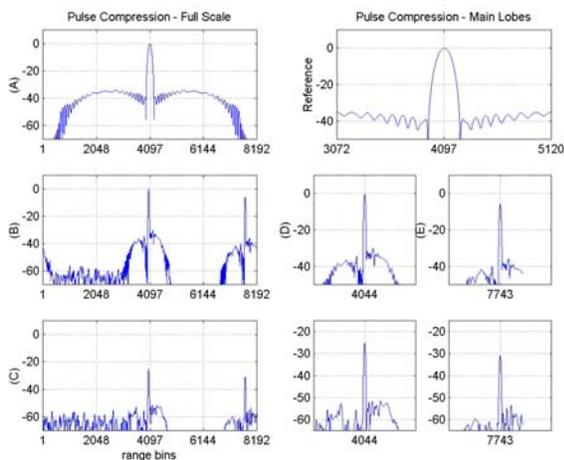


Fig. 14: Full-scale (left) and main-lobe (right) pulse compression output: (A) reference; (B) co-pol; (C) x-pol; (D) 1<sup>st</sup> target of (B); (E) 2<sup>nd</sup> target of (B).

## VI. FPGA DESIGN & IMPLEMENTATION

Preliminary FPGA design and implementation, as a HW proof-of-concept candidate, have been carried out using the ISAAC framework [6]. For each physical receive channel input producing three subband signal outputs, the QM and multi-stage filter design require 36 multipliers running at 60 MHz. The FPGA resource usages are shown in Table 1.

TABLE 1: FPGA RESOURCE USAGES

	Xilinx XQR2V3000	Xilinx XQR4VFX60
<b>Clock</b>	91.8 MHz	112.3 MHz
	Used / Total	Used / Total
<b># of Multipliers</b>	36 / 96	36 / 128
<b># of Slices</b>	10,498 / 14,336	10,533 / 25,280
<b># of Flips Flops</b>	15,753 / 28,672	15,776 / 50,560
<b># of 4-input LUTs</b>	11,910 / 28,672	11,817 / 50,560

## VII. SUMMARY AND FUTURE WORK

This paper described the algorithm specifications and development approach for SMAP's OBP which has the demodulation decimation bandpass channelizer as its first element. This is a bandpass decimation filter designed in multi stages. Point target simulation was illustrated and initial performance assessment validated the multi-stage design.

Future work includes performance with respect to different types of filter, fixed-point error analysis, FPGA design and implementation at 240 MHz, and fault-tolerance strategy.

## ACKNOWLEDGMENT

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