Delta-doped back-illuminated CMOS imaging arrays: Progress and prospects

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ABSTRACT

In this paper, we report the latest results on our development of delta-doped, thinned, back-illuminated CMOS imaging arrays. As with charge-coupled devices, thinning and back-illumination are essential to the development of high performance CMOS imaging arrays. Problems with back surface passivation have emerged as critical to the prospects for incorporating CMOS imaging arrays into high performance scientific instruments, just as they did for CCDs over twenty years ago. In the early 1990's, JPL developed delta-doped CCDs, in which low temperature molecular beam epitaxy was used to form an ideal passivation layer on the silicon back surface. Comprising only a few nanometers of highly-doped epitaxial silicon, delta-doping achieves the stability and uniformity that are essential for high performance imaging and spectroscopy. Delta-doped CCDs were shown to have high, stable, and uniform quantum efficiency across the entire spectral range from the extreme ultraviolet through the near infrared. JPL has recently bump-bonded thinned, delta-doped CMOS imaging arrays to a CMOS readout, and demonstrated imaging. Delta-doped CMOS devices exhibit the high quantum efficiency that has become the standard for scientific-grade CCDs. Together with new circuit designs for low-noise readout currently under development, delta-doping expands the potential scientific applications of CMOS imaging arrays, and brings within reach important new capabilities, such as fast, high-sensitivity imaging with parallel readout and real-time signal processing. It remains to demonstrate manufacturability of delta-doped CMOS imaging arrays. To that end, JPL has acquired a new silicon MBE and ancillary equipment for delta-doping wafers up to 200mm in diameter, and is now developing processes for high-throughput, high yield delta-doping of fully-processed wafers with CCD and CMOS imaging devices.

Keywords: CMOS, detectors, imagers, delta-doped, back-illuminated

1. INTRODUCTION

For more than two decades, scientific charge-coupled devices (CCDs) have set the standard for scientific imaging in space. Compared to CCDs, complimentary metal-oxide-semiconductor (CMOS) imaging arrays offer a faster and more flexible readout architecture. This flexibility has given rise to a growing interest in CMOS imaging arrays for scientific instruments. Despite their advantages, CMOS imaging arrays face several barriers in order to achieve scientific-grade detector performance that has become the standard for CCDs.[1] Were these barriers to be overcome, the unique advantages of CMOS imaging arrays would create new opportunities and capabilities for NASA missions. JPL developed delta-doped CCDs in the early 1990s to solve the problem of surface passivation in back-illuminated CCDs, which is one of the key challenges in achieving science-grade performance in imaging detectors. The development of delta-doped CMOS imaging arrays reported here demonstrates that delta-doping technology may be applied with equal success to CMOS imaging arrays. It remains to be shown that delta-doping is amenable to high volume, high yield production, and to demonstrate the advantages of delta-doped CMOS imaging devices for widespread use in scientific and commercial imaging applications. With the recent acquisition of a production grade MBE machine capable of processing wafers up to 8 inches in diameter, JPL is well-positioned to develop high-throughput, high-yield processes that are needed to enable the production of back-illuminated CMOS imagers on a large scale. In this paper, we report on our progress and prospects in our ongoing development of delta-doped CMOS imaging detectors.

2. THE ORIGIN AND EVOLUTION OF SCIENTIFIC CCDS

2.1 Scientific CCDs and the transformation of Astronomy

The history of scientific CCD development provides an essential background to our development of delta-doped CMOS imagers at JPL, showing both the difficulty and subtlety of finding an effective solution to the problems of back illumination. George Smith, co-inventor of the charge-coupled device, wrote in a recent paper: "In summary, CCDs were born in the Si-SiO_2 revolution and created their own revolution in widespread imaging device applications."[2] Smith's coupling of revolutions in technology and science is particularly appropriate in 2009, the international year of astronomy. Four hundred years after Galileo changed the world by developing the world's first astronomical telescope and using it to discover moons orbiting Jupiter and craters on the lunar surface, NASA is building a new generation of space telescopes to explore the universe with greater depth, precision, and coverage than ever before possible (Figure 1).

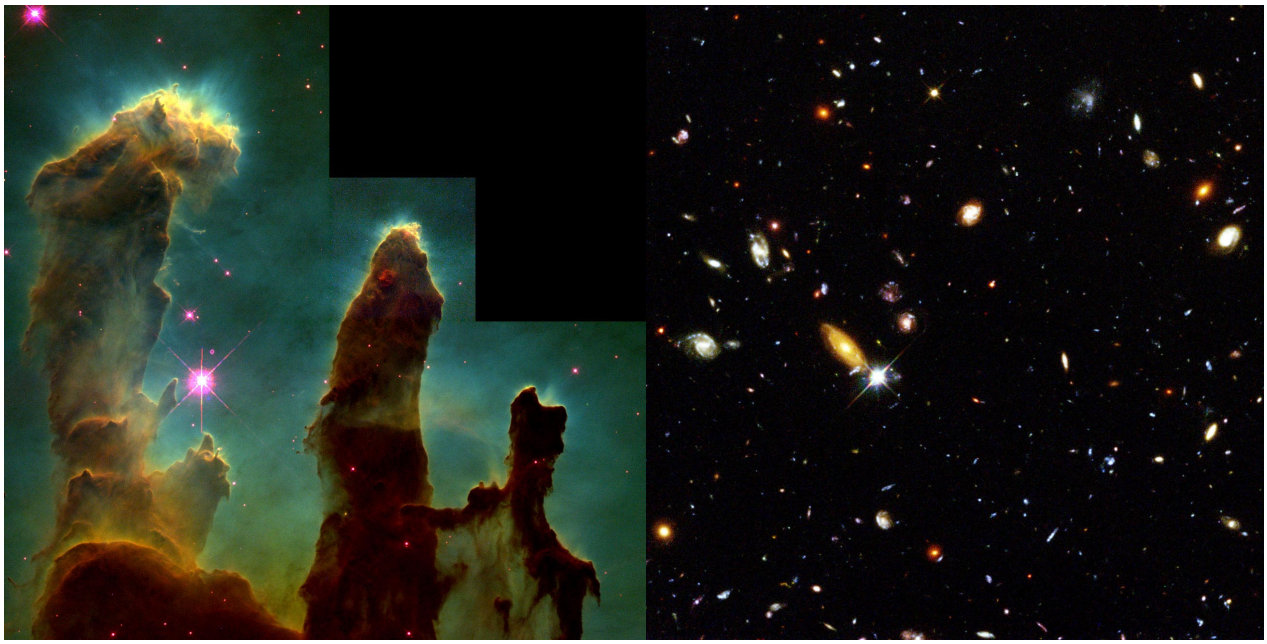

Figure 1. Two iconic images acquired by the Wide Field Planetary Camera 2 on the Hubble Space Telescope. On the left are the Pillars of Creation, which are star forming regions in the Eagle Nebula.[3] On the right is the Hubble Deep Field, in which are visible hundreds of never before seen galaxies.[4]

At the heart of these telescopes are solid state imaging detectors, which transform light into digital images with exceptional sensitivity, resolution, and dynamic range. To achieve such precision is no small task. Light incident on the solid-state imaging array is converted into charge, which is collected over the entire array and measured with sensitivity that can approach the level of single electrons, and yet maintain exceptional photometric precision over a dynamic range covering four to five orders of magnitude. At this level of precision, defects in the detector material become extremely important. From a materials science perspective, many of the challenges currently faced by developers of scientific CMOS imaging detectors come down to controlling the surfaces and interfaces comprising the solid-state imager, and many of these were first encountered with CCDs.

2.2 The origin and early evolution of scientific CCDs

Before the invention of solid state imaging detectors, NASA launched a series of unmanned spacecraft designed to take close-up pictures of the moon's surface in preparation for the moon landing. Film was not an option, because the film could not be returned to earth. The cameras onboard Ranger used vidicons, the only electronic imaging technology then available. Originally developed for television, vidicons convert light first into a beam of electrons and then into an electronic signal suitable for radio transmission. Vidicons are comprised of an evacuated tube with a photocathode at one end for conversion of incident light into electrons, electron optics for collimating and focusing the photogenerated electrons, and an electron-sensitive detector on the other end of the tube for transduction of the electron beam into an electronic signal. Massive and fragile, with poor light sensitivity, nonlinear response, and poor image quality, vidicons

are hardly ideal imaging detectors for spaceflight, let alone for scientific imaging. Compare, for example, the Earthrise photograph taken by Apollo 8 astronauts with a Hasselblad camera, and the vidicon images of the Apollo 11 moon landing. Replacing bulky and fragile vidicon tubes with wafer-thin silicon die promised to be a giant leap for scientific imaging from space.

Solid-state imaging arrays were first proposed by Eugene F. Lally of the Jet Propulsion Laboratory in a presentation to the American Rocket Society in 1961.[5] Lally envisioned the use of mosaic arrays of photodetectors as part of an electronic guidance system for interplanetary travel, but the technology for Lally's system did not yet exist. The key development to make Lally's vision a reality came in 1969, and from an entirely different direction. In that year, Willard Boyle and George E. Smith of ATT Bell Laboratories invented the charge coupled device (CCD) as an electronic alternative to magnetic bubble memory. CCDs use arrays of metal-oxide-semiconductor (MOS) capacitors for storage and serial readout of charge packets. At the same time, ATT Bell Labs was also developing the Picturephone, which would use vidicons to transmit video images over the phone line.

With two technologies being developed side-by-side at ATT Bell Labs—an electronic memory device on the one hand and an electronic camera on the other—Boyle and Smith realized immediately that CCDs could be adapted for electronic imaging, effectively coopting the charge storage and transfer capabilities of "Charge Bubble Devices" to the collection and measurement of photogenerated charge to form an image.[6] Unsurprisingly, CCDs initially suffered from very poor image quality. This was quickly traced to an interface problem, caused by the capture and rerelease of stored charge by surface states located at the $Si\text{-}SiO_2$ interface of the MOS capacitors. In 1970, Smith's team at ATT demonstrated the buried-channel CCD, in which they had modified the original CCD design by incorporating a shallow ion implant at the front surface.[7] Doping the surface alters the electron potential energy to create a buried channel that is spatially isolated from the surface traps. This design modification improved the charge transfer efficiency by several orders of magnitude, but did not eliminate all problems caused by surface states in CCDs, which are varied and subtle, and continue to present challenges to device engineers. Surface states are the bane of imaging detectors, and their presence in back-illuminated detectors played a key role in the history of scientific CCDs.

2.3 Back illuminated CCDs and the surface-interface problem

In 1973, only three years after invention of the CCD was first announced, Texas Instruments developed the first back-illuminated CCD imager, and used it to demonstrate quantum efficiencies as high as 95% at visible wavelengths, a factor of three higher than comparable front-illuminated imagers.[8] Texas Instruments' back-illuminated CCDs demonstrated the significant gains in performance enabled by thinning and back illumination. However, the new silicon surface created in the thinning process introduces a host of new problems, notably quantum efficiency hysteresis (see next section). The problems of back illumination have inspired a variety of potential solutions and intensive research efforts, some of which are still ongoing.

The motive for developing a back illumination process is apparent from the basic device structure shared by both CCDs and CMOS imagers (Figure 2). In the original front-illuminated configuration, incident light is subject to absorption and scattering by the multiple layers of oxides, polysilicon, and aluminum that make up MOS capacitors used for charge storage and manipulation. In contrast, the back-illuminated configuration inverts the imaging detector so that the backside silicon surface is directly exposed to light without any intervening barriers.

Typical CCD and CMOS imaging arrays have an active volume that is only 5-15 microns thick, with the remaining several hundred microns of silicon comprised of highly doped substrate material that is insensitive to light. Thinning achieves a partial solution by eliminating the substrate material, but at the same time the thinning process creates a surface where none existed before (Figures 2 and 3). This new surface impinges directly on the detector volume, creating a variety of new problems that would have to be solved in order to meet the requirements for scientific imaging.

Surface states are electronic states that are confined to silicon surfaces and interfaces. Dangling bonds and surface defects introduce electronic states within the semiconductor band gap that can promote thermal generation of dark current and act as traps capable of the capture and delayed release of photogenerated charge. Charge trapped at the interface and in the overlying oxide creates an electric field that extends some distance into the silicon detector. In p-type silicon, a positively charged surface biases the near surface region into depletion, creating a so-called backside potential well that traps photogenerated charge at the surface (Figure 3).

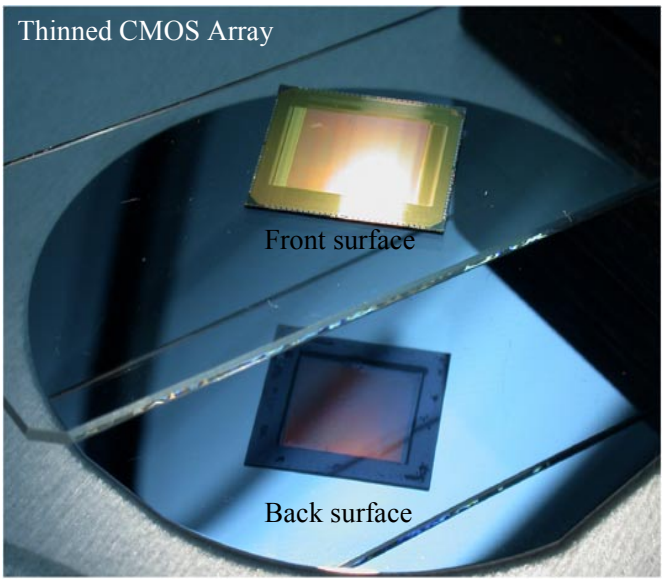

Figure 2. A thinned CMOS imaging array, with the front surface facing up, and the back surface shown in reflection. Only the central portion of the array is thinned, leaving a thick silicon frame for mechanical support.

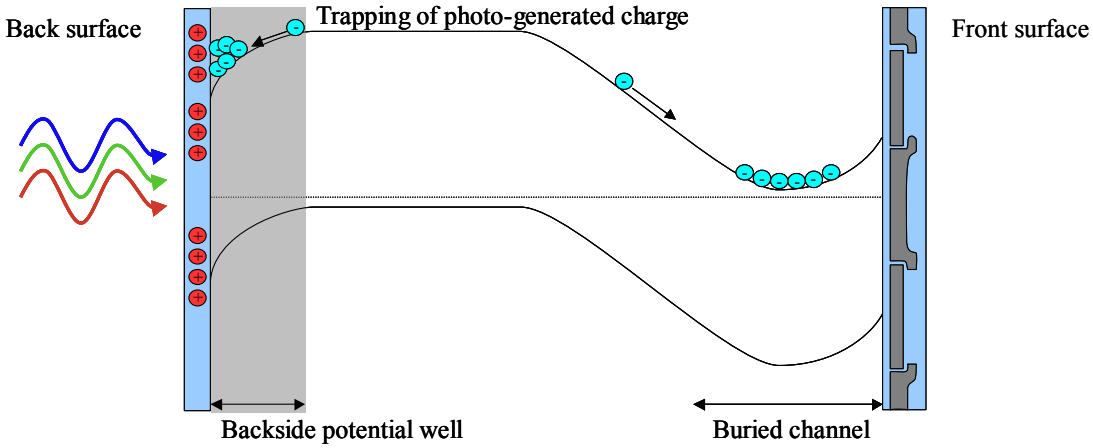

Figure 3: Schematic drawing of the electronic band structure in a back illuminated silicon imaging detector. The detector is depicted in cross section, with the back surface on the left and the front surface on the right. The front surface electrodes, consisting of multiple layers of oxide, polysilicon, and metal, are shown schematically on the right, and an oxide formed on the back surface is shown schematically on the left. Light enters the detector from the back surface, generating free electrons in the conduction band. In order to be detected, the electrons must move by drift and diffusion into the buried channel near the front surface. However, positive charge at the back surface creates a backside potential well, which can trap some of the photogenerated electrons.

2.4 Astronomical CCDs and the Hubble Space Telescope

The Hubble Space Telescope (HST) was conceived at NASA long before there was a detector that could meet its goals. The search for a detector took more than a decade, and even then a considerable detector development effort would be required. The spectacular successes of HST, still ongoing, are testament to the efforts of the early pioneers in scientific CCD technology. Jim Janesick's book on Scientific Charge-Coupled Devices documents an intensive period of development at JPL and elsewhere that led up to NASA's selection of JPL to develop CCDs for Hubble.[9] In 1972, JPL started an advanced technology program to develop CCDs for planetary missions. In 1975, JPL successfully demonstrated a 100x160 back-illuminated Texas Instruments CCD, and announced plans to develop a 400x400 CCD for planetary missions. The next year they announced the development of an 800x800 Texas Instruments CCD for a Jupiter Polar Orbiter mission, which ultimately evolved into Galileo. In 1977, JPL was selected by NASA to develop a key

instrument for the Hubble Space Telescope, the Wide Field and Planetary Camera (WF/PC). The WF/PC focal plane would be comprised of eight back-illuminated, 800x800 Texas Instruments CCDs.

Three generations of WF/PC instruments have flown on Hubble. Originally scheduled for launch in 1984, HST was delayed several times, and ultimately launched in 1990 with WF/PC 1 on board. Problems with HST's primary mirror resulted in a 1993 repair mission, during which WF/PC 1 was replaced by WF/PC 2. Many of Hubble's most spectacular discoveries came from images collected by WF/PC 2. WF/PC 2 flew on HST from 1993 until 2009, when it was replaced by the Wide Field Camera 3 (WFC 3). Throughout this period, CCDs destined for HST evolved considerably, largely in response to quantum efficiency hysteresis.

2.5 Quantum efficiency hysteresis on the Hubble Space Telescope

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Quantum efficiency hysteresis, or QEH, is the bane of scientific imaging. Referring back to Figure 3, the trapping of photogenerated charge at the surface of a back illuminated CCD causes dynamic changes in the surface charge that depend on the illumination history of the surface. Changes in the surface charge cause the depletion depth to change as well, and as a result the effective quantum efficiency of the CCD becomes unstable and hysteretic. In the decades following Texas Instruments' first demonstration of a back illuminated CCD, a variety of processes have been developed to overcome the problems created by surface and interface states at the back surface. These processes share a common goal—bias the back surface into accumulation to prevent trapping of photogenerated charge and stabilize the quantum efficiency. The history of CCD development for the Hubble Space Telescope illustrates the difficulty of this undertaking.

HST's science goals demanded that WF/PC CCDs be sensitive throughout the visible and ultraviolet spectrum, including the scientifically important Lyman-alpha line of hydrogen at 121.6 nm. Thinning and back illumination alone were insufficient to meet the requirements in the ultraviolet, because the backside potential well prevented sensitivity in the deep ultraviolet. In order to meet the science goals, the back surfaces of thinned WF/PC 1 CCDs were coated with a 120 nm coronene film to enhance and extend the UV sensitivity. Coronene is a polycyclic aromatic hydrocarbon ($C_{24}H_{12}$) that absorbs UV light at wavelengths less than 380 nm and re-emits green light with a luminescence peak near 500 nm, resulting in a quantum efficiency for WF/PC 1 CCDs that varied from 5-15% across the UV spectrum.[10,11]

While the WF/PC 1 instrument was undergoing final testing in preparation for its originally scheduled launch in 1984, system-level thermal vacuum tests revealed quantum efficiency hysteresis in the WF/PC 1 CCDs as high as 200%. HST requirements dictate that quantum efficiency must be stable to better than 1%. Further testing of thinned, coronene coated CCDs revealed a previously unknown phenomenon that had unfortunately prevented the discovery QEH earlier in the development. During laboratory testing, the WF/PC 1 CCDs had been routinely illuminated with intense UV in order to inspect the coronene layer. Only after QEH had been discovered in the flight instrument was it discovered that exposing the WF/PC 1 CCDs to intense deep UV light (~250 nm) stabilized the quantum efficiency enough to meet HST specifications. The CCDs so exposed remained stable for several weeks at room temperature, and for much longer when cooled to cryogenic temperatures for testing. Recharging with another UV flood would restabilize the CCDs; unfortunately, there was no way to access the WF/PC 1 CCDs once they had been integrated into the instrument. The only solution for WF/PC 1 was to retrofit the instrument with an external light pipe that could collect solar UV light entering through a hole in the heat shield, and transmit it to the WF/PC 1 focal plane. With this light pipe in place, HST could implement a UV flood on orbit.

Janesick's book describes in some detail the thinning, oxide formation, and UV flood process development undertaken to solve the QEH problem.[9] The substrate-epilayer interface in the TI CCDs is broadened by dopant diffusion during CCD fabrication, in which dopant atoms diffuse from the substrate into the epilayer. Because of this doping gradient, the surface doping concentration after etching, and the quantum efficiency after the UV flood, depended rather sensitively on the final thickness of the CCD. Variations in the device thickness due to nonuniform chemical thinning resulted in variations in the quantum efficiency and stability. Moreover, the effectiveness of the UV flood depended on the process by which the native oxide formed, the temperature, and on the environmental conditions.

In order to find a more permanent solution to the QEH problem, JPL began developing WF/PC 2 as a backup instrument to replace WF/PC 1 during a planned HST servicing mission. The WF/PC 2 CCDs were to be redesigned to achieve long-term QE stability without requiring a UV flood. Four modifications to the WF/PC 1 process were originally proposed: (1) select sensors with thick and uniform p+ layers after thinning; (2) use lumogen instead of coronene as the UV phosphor; (3) deposit a thin layer of platinum on the surface; (4) bias the flash gate to a fixed potential.[11] In the end, too few flight-quality CCDs remained, and new CCDs were manufactured by Loral based on the TI 800x800 format.[12] In 1993, WF/PC 2 was installed on HST with front-illuminated, lumogen-coated Loral CCDs.

In 2009, NASA replaced the spectacularly successful WF/PC 2 with its modern successor, the Wide Field Camera 3. WFC3 includes two back-illuminated 4096x2051 CCDs manufactured by e2v. The e2v back illumination process uses ion implantation with Boron followed by a laser anneal process in order to create a thin, highly doped layer of silicon at the back surface. Ion implantation with Boron introduces fixed, negative charge into the silicon lattice, which can reduce the thickness of the back surface potential well to ~10 nm or less, depending on the process parameters. Ground tests of the WFC3 CCDs prior to launch revealed anomalous behaviors, which were identified as quantum efficiency hysteresis. Mitigation of QEH on WFC3 involves an illumination process not unlike the UV flood, albeit at visible wavelengths.[13,14]

3. DELTA-DOPED CCDS

3.1 A new approach – low temperature molecule beam epitaxy

In the late 1980's, while JPL struggled with WF/PC CCDs, Mike Hecht, Frank Grunthaner, and Paula Grunthaner of JPL's Microdevices Laboratory began studying the surface-interface problem in back-illuminated CCDs from the standpoint of materials science. Experts in the chemistry and physics of Si-SiO_2 interfaces, Paula and Frank Grunthaner had recently developed processes enabling molecular beam epitaxial growth of silicon at low temperatures.[15] Mike Hecht is a physicist, who was studying the electronic band structure of semiconductor surfaces using ballistic electron emission spectroscopy. Mike Hecht's experiments showed that the UV flood process charged the surface by UV-induced adsorption of negatively charged oxygen ions on the CCD surface.[16] With this realization, they proposed exposing the surface to more highly oxidizing molecules, such as NO and N_2O, that could charge the CCD surface without requiring a UV flood. As these molecules are also corrosive, this solution proved effective but impractical. More importantly, Paula, Frank and Mike used their combined expertise to propose a radically different, permanent solution to the QEH problem—the growth by low temperature molecular beam epitaxy of a highly doped, extremely thin layer of silicon on the back surface of the CCD, an approach that ultimately evolved into delta-doping.

3.2 Ion implantation and quantum efficiency hysteresis

In principle, doping the CCD back surface offers a permanent solution to the QEH problem. Unlike the UV flood and other methods of charging the surface, the ionized dopant atoms are covalently bound in the silicon lattice, and are therefore very stable. In practice, eliminating QEH by doping the surface is difficult. Achieving high and stable quantum efficiency is particularly difficult in the ultraviolet, where most of the light is absorbed very close to the surface (Figure 4). As early as 1973, Texas Instruments doped the back surface of their first back-illuminated CCDs to 10^{18} cm^{-3}. At this dopant concentration, the back surface potential well still extends several 10s of nm into the surface, and most of the electrons generated by UV light end up trapped at the back surface. This is why the quantum efficiency of Texas Instruments' first back illuminated CCD dropped from 95% at 500 nm to barely more than 10% at 400 nm, and it is also the reason why the first generation of back-illuminated CCDs designed for the Hubble Space Telescope were coated with a UV phosphor (see last section).

Solving the problem of QEH by doping the surface is more complicated than achieving a high surface dopant concentration. Three additional factors come into play. First, the minority carrier lifetime in degenerately doped silicon is much shorter than in the high quality silicon comprising CCDs and CMOS detector arrays. Second, lattice defects and interstitial dopant atoms introduce traps into the highly doped region, further shortening the minority carrier lifetime and potentially exacerbating the QEH problem. Third, it is not enough to get the dopant atoms into the silicon—in order to be electrically active they must be incorporated into silicon lattice sites. Taken together, these requirements introduce constraints on the distribution of dopant atoms near the surface (the dopant profile) in order to create a near-surface electric field that is strong enough to drive photogenerated charge away from the surface before it is lost to recombination or trapping. A considerable amount of effort has gone into developing low energy ion implantation techniques that can simultaneously achieve a high surface dopant concentration, a very narrow dopant distribution, and a

low density of defects. This development has enabled a considerable reduction of QEH, but, as we saw with WFC3, even the best available ion implantation techniques do not completely eliminate QEH.

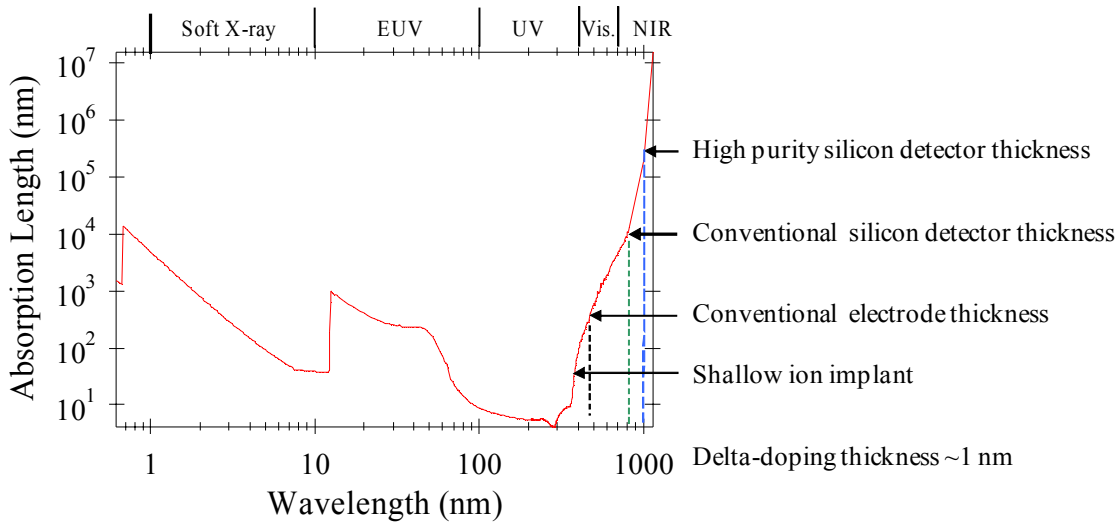

Figure 4: Logarithmic plot of the absorption length of light in silicon covering the spectral range from soft X-rays through the near infrared, illustrating the challenge of UV detection with silicon detectors. Because silicon is an indirect gap semiconductor, the near-bandgap absorption length is very long. Absorption in the ultraviolet is very strong, because at the ultraviolet energies higher energy bands come into play to allow direct-gap transitions. UV absorption in silicon is dominated by two strong absorption peaks at ~360nm and ~270nm. At 270 nm, the 1/e absorption depth in silicon is only 4 nm.

Using numerical modeling tools to calculate the band structure of doped silicon, it is possible to quantify the relationship between the dopant profile and the near surface electric field. Figure 5 shows the electric field in units of V/nm for four different simulated dopant profiles. Only delta-doping achieves a near-surface electric field that is high enough to prevent UV-generated photoelectrons from being trapped in the backside potential well.

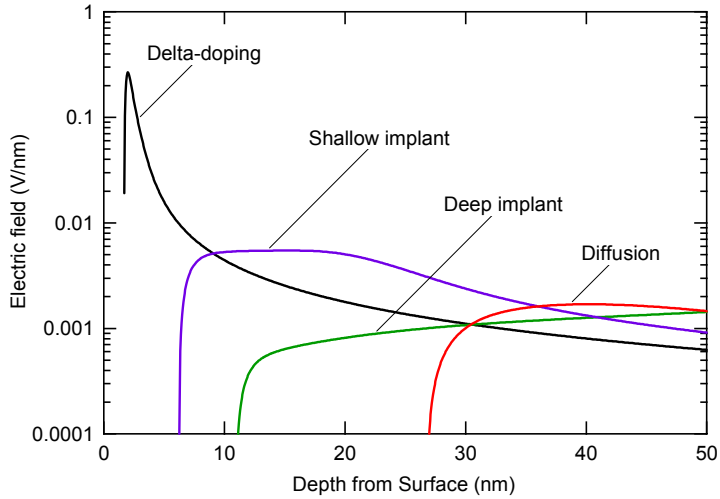

Figure 5: Near surface electric field calculated for four different dopant distributions. The electric field is given in units of Volts/nm, and depth from the surface is given in nanometers; for comparison, the minimum 1/e absorption depth in silicon is approximately 4 nm, and thermal energy is approximately 0.015 eV at –100 C. In order to prevent trapping of UV-generated photoelectrons from being trapped in the backside potential well and eliminate quantum efficiency hysteresis, a sharply peaked dopant profile is essential to creating a strong electric field within a nm of the surface. Only delta-doping can achieve this goal.

3.3 Delta-doping and the elimination of quantum efficiency hysteresis

Low-temperature molecular beam epitaxy (MBE) finally provided the ideal solution to back surface passivation and the elimination of quantum efficiency hysteresis. Whereas conventional MBE growth of silicon requires heating the silicon substrate to temperatures greater than 800 C in order to remove the native oxide, JPL's low temperature MBE growth process can be accomplished at temperatures below 450 C. The difference is significant. A fully-processed CCD cannot survive temperatures above 500 C, due to interdiffusion of silicon and aluminum on the front surface. CCDs could, in principle, survive JPL's low temperature MBE process.

Two aspects of molecular beam epitaxy make it the perfect tool for achieving the ideal dopant profile for CCDs. First, MBE is a crystal growth technique that enables the epitaxial growth of silicon one atomic layer at a time. Because the process is one of growth rather than diffusion or implantation, this control enables a level of band structure engineering that is not possible with any other technique. Second, MBE is a nonequilibrium crystal growth process. This means that MBE-grown silicon can have dopant concentrations far higher than can be achieved by conventional doping processes.

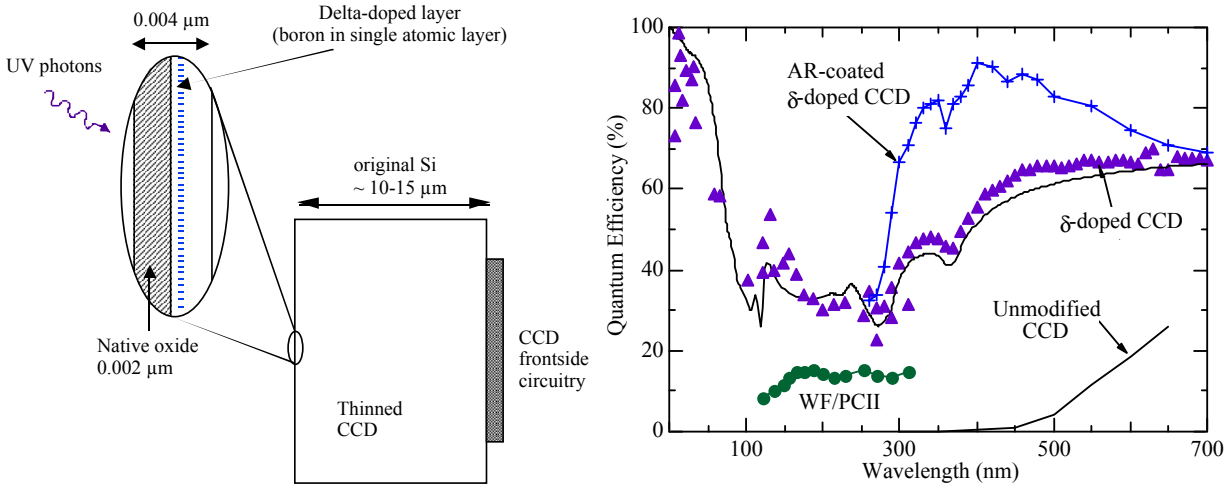

Figure 6: (a) Cross section schematic of a delta-doped CCD (left). The epitaxially-grown delta-doped layer on the back surface of a thinned CCD places a high density of boron atoms approximately 0.5 nm below the silicon surface and the native oxide. (b) Delta doped CCDs exhibit 100% internal QE from extreme UV to the visible (i.e., measured external QE is equal to the silicon transmittance, which is the detection limit for uncoated back-illuminated silicon devices). In order to extend this comparison between reflection and quantum efficiency into the deep UV and extreme UV, the quantum efficiency data have been adjusted downward to remove the effects of multiple electron-hole pair production at high photon energies. Data from an antireflection-coated, delta-doped CCD demonstrate QE optimization for particular spectral range (in this case, the AR-coating was optimized for high QE from 300-400 nm, which is a challenging range for silicon due to the two silicon absorption peaks at approximately 360nm and 270nm).

Using the compositional control afforded by the MBE growth process, dopant atoms can be incorporated into the crystal in a highly localized layer that lies approximately 1 nm beneath the silicon surface (see Figure 6a, and Hoenk92[17]). The resulting sharply-peaked dopant distribution resembles the mathematical delta function. With a surface charge density of ~2×10^{14} Boron/cm^2, delta-doping creates very high electric fields near the surface that drive photogenerated charge away from the back surface and suppress the generation of excess dark current from the exposed silicon surface. Because this layer is extremely thin, essentially all of the photogenerated charge can be detected, even when the incident light is absorbed very near the surface. Figure 6a shows the delta-doped CCD structure, and Figure 6b shows the measured QE response of thinned, delta-doped CCDs in comparison with a lumogen-coated WF/PC 2 CCD used in the Hubble Space Telescope. Delta-doped CCDs have been experimentally shown to exhibit quantum efficiency at the theoretical limit of silicon transmittance in the EUV, FUV, UV, and the visible. The exceptional stability of delta-doped detector arrays has been demonstrated by various groups as a function of time,[18] temperature [Elliott and Janesick96], illumination history[19] and ambient gases,[20] with no observed changes in the quantum efficiency under any environmental conditions and no evidence of quantum efficiency hysteresis.

4. DELTA-DOPED CMOS IMAGING ARRAYS

4.1 CMOS Imaging Arrays

CMOS active pixel sensor (APS) imaging arrays are arrays of silicon detectors in which each element of the array contains at least one transistor operating as an active device, that is, as an active amplifier rather than simply as a switch. In contrast to CCDs, which transfer collected charge serially to a small number of on-chip readout amplifiers, CMOS APS arrays operate with a parallel readout architecture similar to a Dynamic Random Access Memory (DRAM) chip (Figure 7). Within each pixel, an integrated amplifier converts the signal charge to a voltage for temporary in-pixel storage. Random access readout is enabled by an array of select switches connected in parallel to the rows and columns of CMOS APS pixels. CMOS Readout Integrated Circuits (ROICs) with a similar architecture have been used for decades in infrared sensors, but the chip area necessarily devoted to signal processing initially placed impracticable limits on pixel size for CMOS APS imagers. JPL revived interest in scientific CMOS APS visible imager technology in the early 1990's, when advances in CMOS processing techniques permitted the reduction in pixel size necessary for high-resolution imaging.

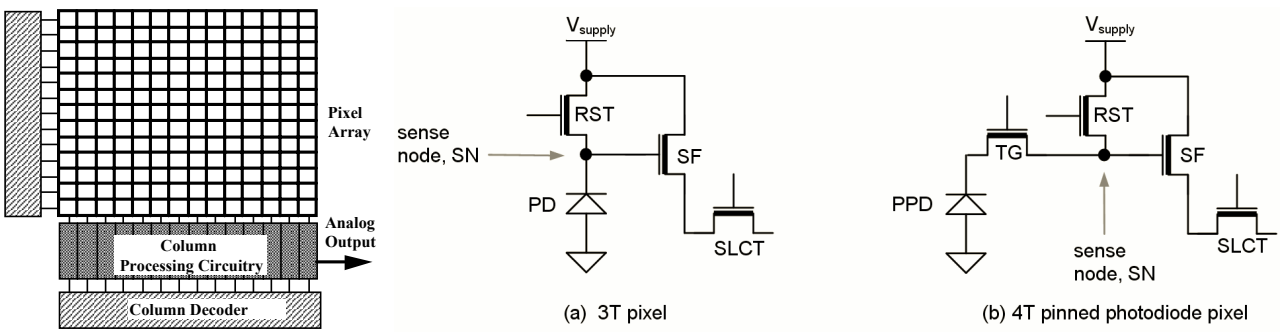

Figure 7: Schematic illustration of the layout of a CMOS APS imaging detector, and two types of in-pixel circuits. A basic 3T pixel contains three transistors to implement measurement, addressing, and reset functions essential to the operation of the detector. Additional transistors, such as the 4T pixel on the right, can improve performance and add functionality.

Because the detector is made in a standard CMOS process, all timing and control circuitry necessary for readout can be integrated on-chip. In addition, application-specific signal-processing circuits can be integrated into the design to add customized data-processing functions for particular applications. Another advantage for scientific imaging is the low power dissipation of CMOS imaging arrays, typically in the range of milliwatts or tens of milliwatts.

As with CCDs, light incident on CMOS APS arrays may be scattered or absorbed in the front surface structures that make up the array electronics. In addition, CMOS APS arrays suffer from an additional loss of efficiency because the light-sensitive photodiodes occupy only part of the surface, the remainder of the surface being devoted to the transistors necessary for detection, signal processing, and readout. While it is possible to recover part of these losses using antireflection coatings and lenses, back illumination offers far better performance for scientific CMOS imaging arrays, including higher quantum efficiency, potentially 100% fill factor, and sensitivity in the ultraviolet. Commercial manufacturers of CMOS imaging arrays have developed back illumination processes based on ion implantation, diffusion, and chemisorption; however, as we have seen, these processes can achieve the performance of delta-doped detectors.

4.2 Delta-doped CMOS Imaging Arrays

From a materials science standpoint, the back surfaces of thinned CCDs and CMOS imaging arrays are identical. The commonalities of CMOS imaging arrays and CCDs are such that the processes developed for delta-doping CCDs apply equally well to CMOS devices. Using a frame-thinning approach originally developed for CCDs, we were able to demonstrate high quantum efficiency in delta-doped CMOS arrays (Figures 2 and 8). These data show that reflection-limited quantum efficiency is attainable in CMOS imaging detectors, just as with CCDs.

There are differences between the two device architectures relevant to the thinning and back illumination. One relatively minor difference lies in the relative thicknesses of CCDs and CMOS arrays. The epilayer thickness in a standard CMOS process is only 5 microns in thickness, compared to the 10-15 micron epilayer thickness of typical CCDs. This made the thinning process slightly more difficult for CMOS devices, the tolerances for thinning uniformity are tighter for the

thinner membranes. In addition, after thinning the depletion edge of the front surface structures reaches the back surface in some areas of the device, so that prior to delta-doping, thinned CMOS arrays were found to be saturated with dark current at room temperature, and hence inoperable. Delta-doped, back-illuminated CMOS arrays did not exhibit any excess dark current, because the back surface defects are fully passivated by the delta-doping process. Finally, though it does not concern us here, it should be noted that the more complicated pixel structure of CMOS APS arrays leads to a requirement that these devices be optimized for back illumination, in order that the three dimensional electronic potential in the pixels causes all of the signal charge to be collected at the sense nodes in the array. Absent such optimization, some of the signal charge may not be detected, and the potential with back illumination for achieving 100% fill factor will not be realized.

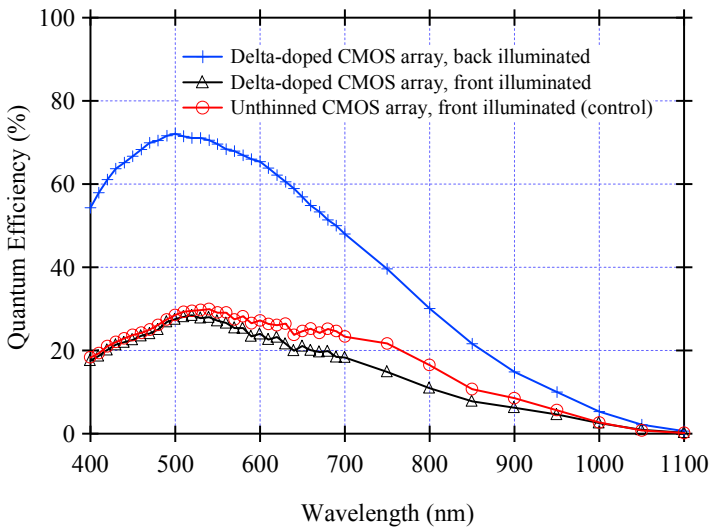

Figure 8: Quantum efficiency of a delta-doped CMOS imaging array, shown without an antireflection coating. As with delta-doped CCDs, the quantum efficiency of delta-doped CMOS arrays is limited primarily by reflection from the silicon surface. Most of the improvement in quantum efficiency achieved with back illumination results from the elimination of absorption in the front surface structures as a loss mechanism. Delta-doping passivates the silicon surface in the thinned CMOS imaging array, which is essential for the elimination of excess dark current during normal operation of the device. For comparison, both back-illuminated and front-illuminated quantum efficiencies of the delta-doped CMOS device are plotted in comparison to a normal, unthinned CMOS device. As expected, the differences in quantum efficiency between the unthinned control device and the front-illuminated delta-doped device occur primarily at longer wavelengths, where the thinned device has less material to absorb the deeper-penetrating near infrared light.

4.3 Batch processing of delta-doped CMOS imaging arrays – initial process development

One of the main challenges to enabling the widespread application of delta-doped detectors in scientific instruments and elsewhere lies in the manufacturability of the delta-doping process. Whereas NASA's new generation of space telescopes require focal planes with dozens, and eventually hundreds of large format detector arrays, we have so far been limited by the capacity of our MBE to delta-doping one detector at a time. In this section, we present the results of our initial efforts to increase the throughput with the existing 3-inch Riber MBE. In the next section, we present progress and prospects of JPL's recent investment in production scale delta-doping of CMOS and CCD imaging arrays.

All of the work previously done at JPL on delta-doped detectors has used the Riber EVA 32 silicon MBE. This MBE uses a manual sample transfer system with a maximum capacity of a single, three-inch diameter wafer. Because of this limitation, we developed processes for delta-doping a single detector die at a time. Figure 2 shows a frame-thinned CMOS APS imaging array, in which the thick silicon frame serves a dual purpose: first, providing mechanical support for holding and manipulating the fragile detector membrane; and second, providing a rigid substrate for the bond pads, enabling wire-bonding during detector packaging.

In order to increase the delta-doping process throughput, JPL modified its thinning processes to produce 9 thinned devices on a single raft (Figure 9). The corner-to-corner diagonal of the raft was kept to less than three inches, so that it could fit into the Riber MBE. Rafts were first diced from the device wafer and thinned by chemical-mechanical polishing to a thickness of approximately 200 microns. Die-sized shadow masks were placed over the detectors to be

thinned, and a silicon nitride etch mask was deposited on the raft by plasma-enhance chemical vapor deposition in order to define the shape of the thick frame. Chemical processes for thinning the CMOS detectors to remove the substrate are described elsewhere.[21] The raft containing 9 free standing membranes was delta-doped with $2x10^{14}$ Boron/cm^2 using previously described processes.[17] Optical flats were bonded to the delta-doped surface to flatten the membrane and provide a rigid structural support for subsequent bump-bonding and packaging. Using photolithography and liftoff, indium bumps were deposited on the bond pads of the detector and readout circuits. Following dicing to produce individual die, the detector and readout were bonded together using thermal compression bonding of the indium bumps. Figure 10 shows a high resolution image acquired by the thinned, delta-doped CMOS imaging array produced using this process. Process yield for these 9-die rafts is improving.

Future development will take advantage of the substantial gains in throughput and yield enabled by wafer-level processing (see next section). The first step toward wafer level processing is the development of a full wafer thinning process. Figure 11 shows a 6 inch wafer with 32 CMOS imaging arrays that has been bonded to a glass support and thinned to a final thickness of ~5 microns using chemical-mechanical polishing and HNA thinning. At this thickness, the CMOS imaging arrays are translucent, and it is actually possible to see the front surface detector structures by looking through the silicon back surface.

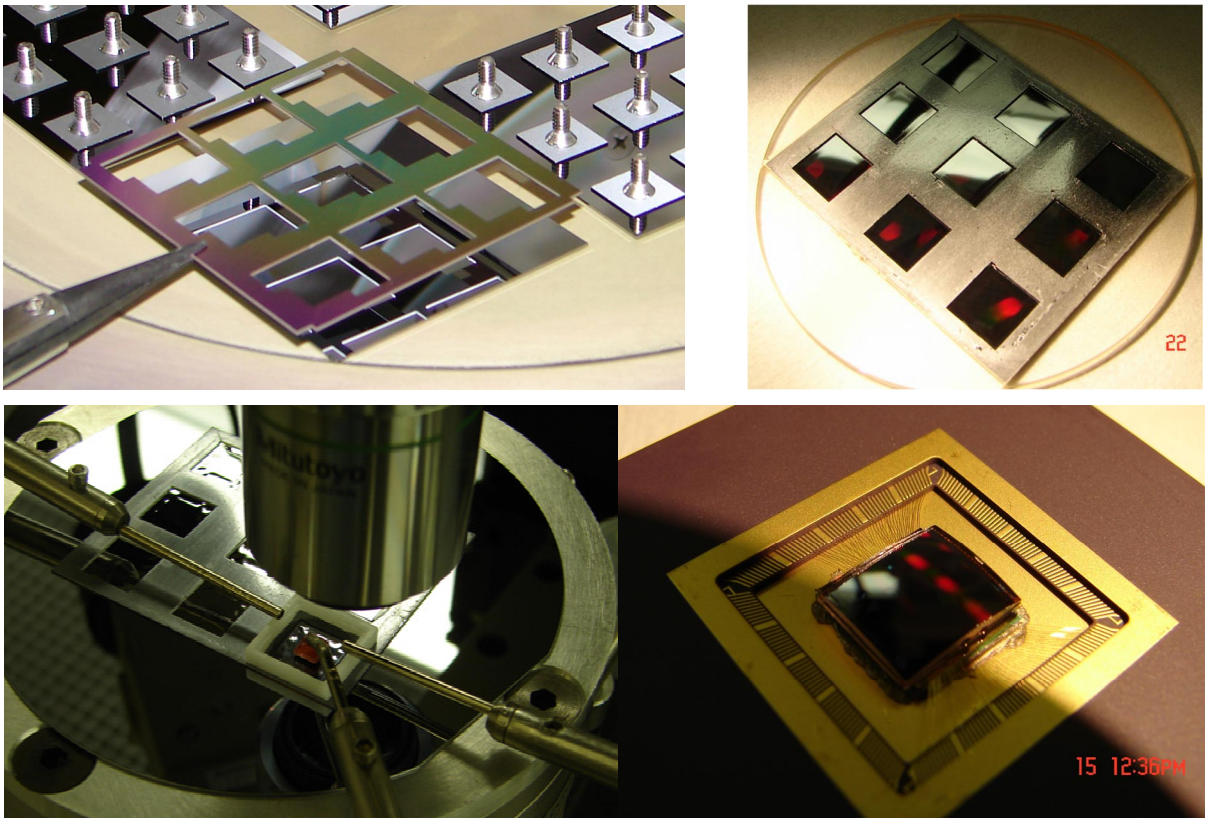

Figure 9: Photographs showing the process steps developed to implement a multi-chip delta-doping process for higher throughput (see text). The photograph on the upper left shows the placement of shadow masks on a 9-die raft, in preparation for deposition of a silicon nitride etch mask. The photograph on the upper right shows a frame-thinned, 9-die raft ready for delta-doping. The photograph on the lower left shows the placement and bonding of optical flats on the membranes in preparation for bump-bonding. The photograph on the lower right shows a thinned, delta-doped, and packaged CMOS imaging array.

Figure 10: High resolution image acquired by a thinned, delta-doped CMOS imaging array.

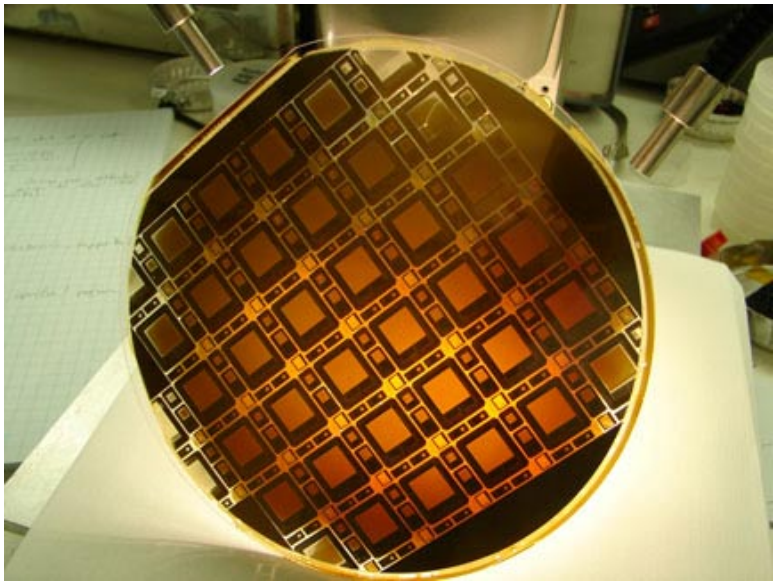

Figure 11: Six inch wafer with 32 CMOS imaging arrays thinned to a final thickness of approximately 5 microns. The thinned wafer is supported on a transparent glass substrate, making the entire structure transparent. Full wafer thinning with a bonded support is one of the processes necessary for wafer-level delta-doping, currently under development at JPL.

4.4 Wafer level delta-doping of CMOS and CCD imaging arrays – Progress and Future Prospects

State-of-the-art CCD fabrication facilities currently use six inch wafers, and state-of-the-art CMOS imager foundries use eight inch wafers. In order to enable full wafer scale production of delta-doped CCDs and CMOS detectors, JPL has recently acquired a production grade Veeco GEN200 Silicon MBE (Figure 12). The new MBE is equipped with a cluster tool with an automated sample transfer system that can move wafer cassettes between chambers under computer control. Attached to the cluster tool are a load-lock chamber and a UHV storage module with motorized elevators, enabling the loading and storage of up to eight wafer cassettes at a time. Each wafer cassette holds a 10” platen, which can be configured for single wafers up to 8” in diameter or for multiple smaller wafers. The preparation chamber is separately pumped, and equipped with a sample heater, gas inlet ports, and an rf source configured for implementing *in vacuo* surface preparation processes. The growth chamber has 12 effusion cell ports to accommodate multiple dopant materials, and dual e-beam sources enabling codeposition of silicon and up to four additional source materials. The entire system is under computer control, enabling the development of automated multi-wafer processes for high-throughput delta-doping of CMOS and CCD wafers.

Looking to the future, there are a number of opportunities and applications for delta-doped CCD and CMOS imaging arrays that will be facilitated by these developments. High throughput, high yield processes for delta-doping will make these detectors more affordable for both NASA and commercial applications. As scientific imaging detectors continue to increase in size and complexity, delta-doping the very large format imaging detectors will require wafer-level processes. The largest monolithic imaging detectors are limited by wafer size, with the record currently standing at 10,580x10,560 pixel CCD and camera manufactured by Semiconductor Technology Associates.[22] Even though the 111 megapixel detector practically fills a 5 inch wafer, CCD and CMOS manufacturers are already working with 6" and 8" wafers, so even larger devices will likely follow. Throughput becomes essential in applications requiring large numbers of detectors. Mosaic focal planes have already grown beyond gigapixel resolutions, and ever more detectors are needed to populate the largest focal planes. For example, the Star Formation Camera (SFC), currently proposed for launch in 2020, will require 540 large format CCDs to populate its two focal planes.[23] These developments impact ground-based scientific and commercial applications. For example, wafer and reticle inspection systems for the semiconductor industry are already being pushed into the deep ultraviolet, and soon will require high resolution, high speed focal planes capable of imaging in the extreme ultraviolet.[24] Delta-doping is ideal for all of these applications, and work is currently underway on several delta-doped detector technologies for planetary and astrophysics focal planes, high energy physics instrumentation, and potential commercial instruments.

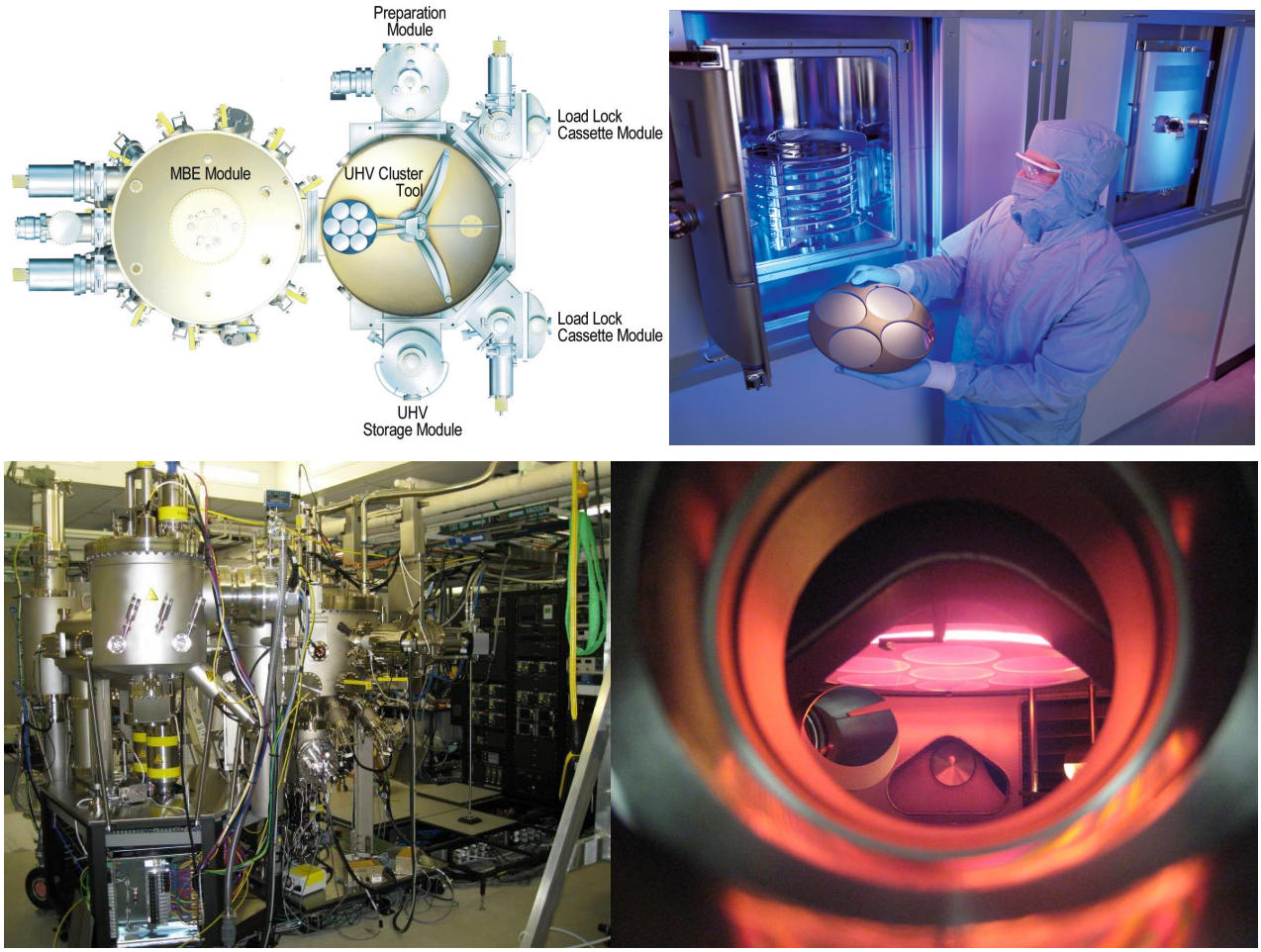

Figure 12: JPL's newly acquired Veeco GEN200 Silicon MBE. On the upper left is a schematic showing the various chambers and functionalities of the system, which is computer controlled and capable of fully automated processing (see text). On the upper right is a photograph of the load-lock chamber, showing the 8-cassette elevator for multiple-wafer processing. On the lower left is a photograph showing the Veeco GEN200 system at JPL after initial hook-up of facilities. On the lower right is a photograph of a cassette containing seven 3" wafers inside the growth chamber. (Schematic and photo of load-lock chamber courtesy of Veeco, Inc.)

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