Adaptation of the Electra Radio to Support Multiple Receive Channels

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Abstract— Proposed future Mars missions plan communication between multiple assets (rovers). This paper presents the results of a study carried out to assess the potential adaptation of the Electra radio to a multi-channel transceiver. The basic concept is a Frequency Division multiplexing (FDM) communications scheme wherein different receiver architectures are examined. Options considered include: (1) multiple IF slices, A/D and FPGAs each programmed with an Electra baseband modem; (2) common IF but multiple A/Ds and FPGAs and (3) common IF, single A/D and single or multiple FPGAs programmed to accommodate the FDM signals. These options represent the usual tradeoff between analog and digital complexity. Given the space application, a common IF is preferable; however, multiple users present dynamic range challenges (e.g., near-far constraints) that would favor multiple IF slices (Option 1). Vice versa, with a common IF and multiple A/Ds (Option 2), individual AGC control of the A/Ds would be an important consideration. Option 3 would require a common AGC control strategy and would entail multiple digital down conversion paths within the FPGA. In this paper, both FDM parameters as well as the different Electra design options will be examined. In particular, signal channel spacing as a function of user data rates and transmit powers will be evaluated. In addition, tradeoffs between the different Electra design options will be presented with the ultimate goal of defining an augmented Electra radio architecture for potential future missions.

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1. INTRODUCTION

A proposed Mars rover mission would be launched by NASA in May 2018 and would carry with it the European Space Agency's (ESA's) ExoMars rover (EXM) as well as the proposed NASA Mid-Range rover (MRR). The rovers would land together on the surface of Mars in January 2019. Both rovers would operate through an orbiter, proposed for launch in 2016. Since the orbiter would fly ELECTRA payloads [1], [2] as onboard transceivers, the implementation of Prox-1 protocol would be in accordance with [3].

Given this projected multiple-rover scenario, communications would typically comprise the following elements: (i) an orbiter which establishes communication with a rover via a "hailing" operation in combination with relay/forward commands sent from Earth and received by the orbiter usually before the overflight and (ii) each rover present in the area responds separately to the hail by sending telemetry data to the orbiter to be relayed/returned to Earth when a direct-to-Earth link becomes available.

The preliminary requirement for average data volume return is 250Mb/sol for the proposed MRR and 150Mb/sol for the EXM rover [4]. Since both rovers would share the landing site and the same orbiter, they would be available for communications during the same time windows. Consequently, techniques for simultaneous communications between the rovers and orbiter must be examined. Two options have been considered: (i) time-division multiplexing

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(TDM) and (ii) frequency-division multiplexing (FDM). In either case, modifications to the basic Electra transceiver on the orbiter would be required. These are first discussed in Section 2 followed by a discussion of automatic gain control (AGC) considerations for the transceiver are presented in Section 3. Tradeoffs between the TDM and FDM communication options are then presented in Section 4 and a summary is given in Section 5.

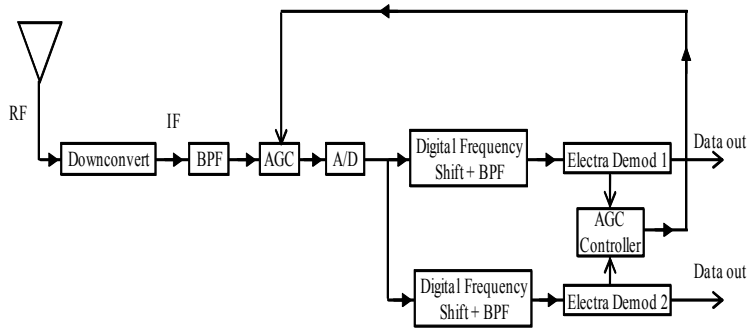
2. Electra Transceiver Architecture

First of all, we note that TDM would require the fewest modifications to the Electra transceiver architecture. These would mainly entail software changes to accommodate the multiple, time-multiplexed data streams. Consequently, we focus here on the more substantial (firmware) modifications required to accommodate FDM which, as shown in Section 4, provides significant data volume improvements over TDM. Of course in general, a combination of TDM and FDM would be desired.

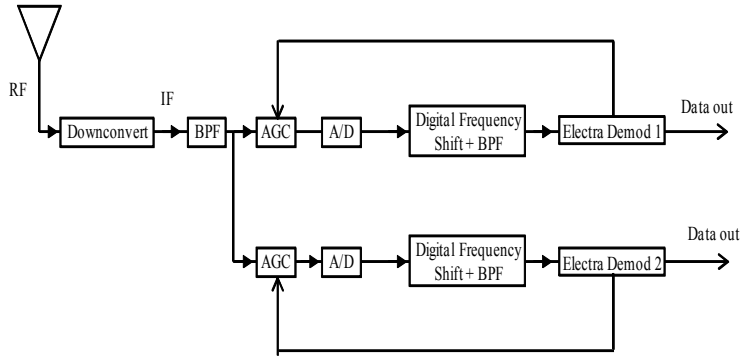
There are several potential options for modifying the basic, single-channel Electra transceiver architecture to accommodate multiple FDM signals from the proposed rovers. However, to provide a practical architectural constraint, we assume that a common RF down conversion to IF (nominally 70 MHz) is used thereby eliminating changes to the existing Electra front end RF electronics. This leaves two basic options utilizing either a single A/D (typically operating in the 16-19 MHz range) and AGC control or dual A/Ds (16-19 MHz) and AGC controls. These architectural options are presented in Figure 1 corresponding to dual FDM signals.

It is presumed that the IF bandwidth (typically 7 MHz) encompasses both of the input signal channels and that additional, digital tuning is required to center the signals at complex basedband and provide sufficient digital filtering to minimize adjacent channel interference (ACI) in the two digital demodulators (which will be addressed further in Section 4). From an implementation standpoint, Figure 1a is preferable since it requires only a single A/D and AGC. However, a limitation with this option is that a strong signal can cause the AGC to attenuate a weak signal to such an extent that it is substantially degraded by the A/D quantization noise. However, within the Mars 2018 dual rover scenario, this would not be significant issue since the EIRP of both rovers are within 3 dB of each other (EXM has 3 dB less EIRP than the proposed MRR). Thus the received power differential at the orbiter would be within approximately 3 dB [4]. As such it is not anticipated that the strong-weak signal scenario would be an issue with the single A/D-AGC architecture and thus we will focus on this architecture in the remainder of this paper.

There are two keys to the operation of the single A/D-AGC architecture in Figure 1a: (i) the AGC controller and (ii) the digital down converter (labeled "Digital Frequency Shift + BPF" in Figure 1). The former will be discussed in Section 3 and the latter would be implemented as depicted in Figure 2. Also in Figure 2, f_0 represents the digital down conversion frequency. Typically, we express $f_0 = 0.25 \pm \Delta f$, where $0 <$



a. Single A/D and AGC



b. Dual A/Ds and AGCs

Figure 1. Electra Transceiver Architectural Options to Accommodate FDM Signaling.

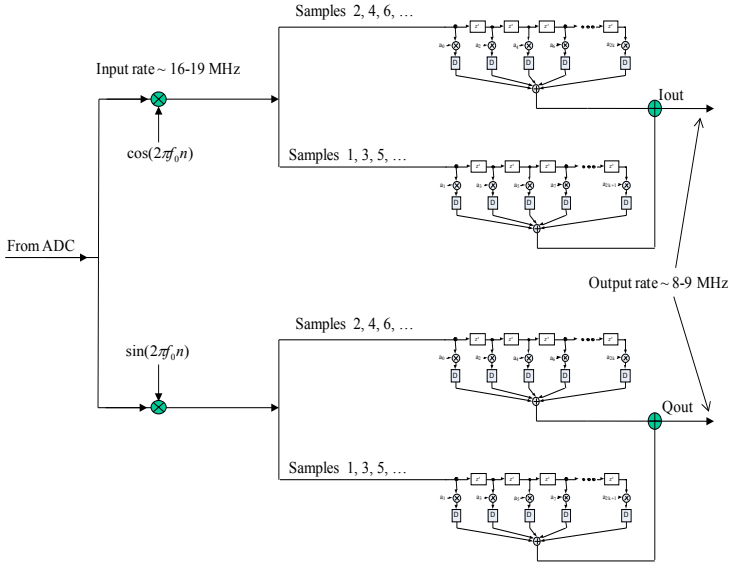


Figure 2. Digital Down Converter.

$\Delta f < 0.25$ is the frequency offset from the digital IF frequency. In the standard Electra transceiver configuration with single input signal, the digital IF frequency is in the middle of the Nyquist band, i.e., Fs/4 (Fs denotes the input sample frequency), in which case $f_0 = 0.25$ and the cos/sin multipliers in Figure 2 simplify.

Note that the digital filtering is implemented as finite impulse response (FIR) filters in a dual-channel polyphase configuration. This allows the FIR filters to run at half the input sample rate which implies that the input signal bandwidth must be Fs/4 ~ 2 MHz or less to avoid aliasing after decimation by 2. As discussed in Section 4, this is consistent with the Electra transceiver given its input IF bandwidth ~ 7 MHz.

As an example of dual signal separation, consider the following scenario corresponding to an IF at 69.632 MHz and an A/D sample rate of 16.384 MHz: a 256 kbps BPSK strong signal centered at IF (and translated down to 4.096 MHz after bandpass sampling) and a 256 BPSK weak signal (10 dB lower) centered at IF + 1.8 MHz (and translated down to 5.896 MHz after bandpass sampling). The resulting input signal spectrum, after bandpass sampling, is depicted in Figure 3a. For purposes of illustration, no additive noise has been included in this example. The spectrum of the weak signal channel, after digital decimation to 8 samples per symbol (2.048 MHz decimated sampling rate), is depicted in Figure 3b in the case of no digital band select filtering. This corresponds to utilizing the existing Electra unit, without modification. As is seen, weak signal demodulation would be severely compromised in this case. Application of digital band select filtering, prior to decimation, is required to reduce strong signal aliasing into the weak signal channel as illustrated in Figure 3c.

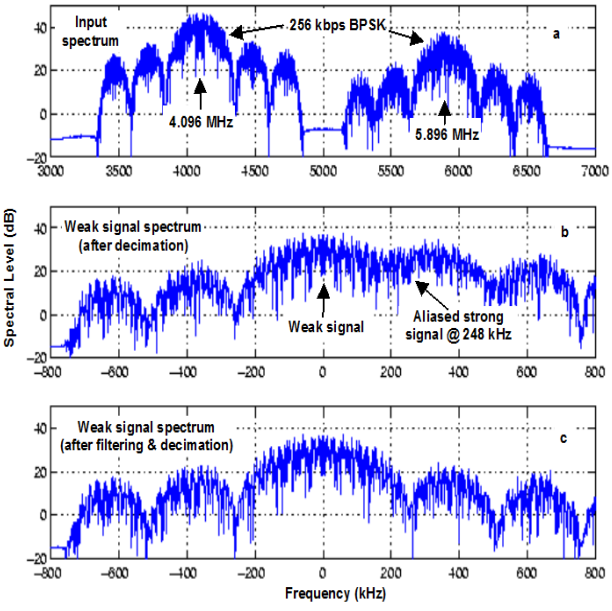


Figure 3. Effects of strong signal aliasing into the weak signal channel.

3. Automatic Gain Control Strategies

First we briefly review the AGC control circuit for the single channel Electra transceiver. It is a single loop, all digital control design as depicted in Figure 4 (R_s denotes the symbol rate). The AGC control extends from the Costas[2] arm filter outputs back to the ADC input and is designed to maintain a constant power level at the output of the Costas arm filters, where the bandwidth is generally much narrower than the IF filter bandwidth. In addition two static gains, K_{cic} and K_{arm}, are inserted before the internal cascaded integrator-comb (CIC) quantizer and after the arm filters, respectively. These gains are programmable, dependent upon the data rate and decimation factor M (chosen such that there are approximately 16 samples per data symbol), and are used for purposes of minimizing the effects of quantization noise and saturation.

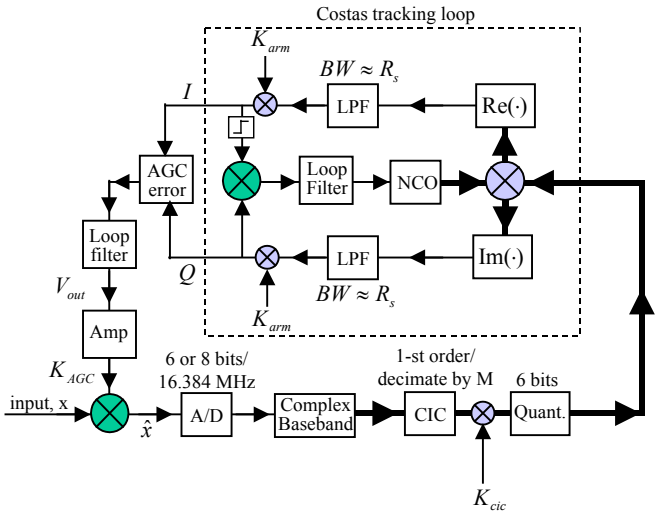


Figure 4. Single-loop AGC design. (The heavy dark lines denote complex data paths.).

As seen in Figure 4, the digital AGC error signal, E_{AGC}, is generated from the Costas arm filter outputs, I and Q, via:

$$E_{AGC} = K_{gain} \cdot (\sqrt{I^2 + Q^2} - 1) \ ,$$

where K_{gain} controls the time constant of the AGC as well as the variance of the resulting amplitude gain estimate. The AGC error signal E_{AGC} is integrated in the AGC loop filter to form the AGC control voltage V_{out}, i.e.,

[2]This configuration corresponds to suppressed carrier signaling. It can be easily modified to accommodate residual carrier signaling.

$$V_{out} = V_{out} + E_{AGC} \ ,$$

and the magnitude of the result, $|V_{out}|$, is used to generate the AGC gain, K_{AGC}, via an analog gain control amplifier (GCA) with nonlinear transfer curve, $f(\cdot)$, i.e.,

$$K_{AGC}(dB) = f\left(|V_{out}|\right).$$

This gain is then used to scale the A/D input.

Returning to the dual channel FDM architecture in Figure 1a, it is seen that since there is only one AGC then its input must be some combination of the AGC control voltages available from the individual Electra demodulators. Here we consider two options:

$$\text{Option 1: } V_{out} = \max\left\{V_{out}^1, V_{out}^2\right\},$$

$$\text{Option 2: } V_{out} = \min\left\{V_{out}^1, V_{out}^2\right\},$$

where V_{out}^1 and V_{out}^2 denote the AGC control voltages available from the individual Electra demodulators. The first option results in the smallest possible AGC gain (largest AGC attenuation). In this case, V_{out} will coincide with the AGC control voltage produced by the Electra demodulator unit operating on the largest input signal. This option practically eliminates A/D saturation but can result in significant A/D quantization noise degradation whereas the second option, $\min\left\{V_{out}^1, V_{out}^2\right\}$, minimizes quantization noise effects but can result in A/D saturation.

A modification to the Electra demodulator required for dual-channel operation is the implementation of additional digital AGCs. Since the AGC at the input to the A/D is being controlled either by the strong or weak signal power level, only one of the Costas arm filter outputs will maintain a unity RMS level. Thus additional digital AGCs are required to equalize the Costas arm signals, i.e., so that the RMS arm levels in each Costas loop is approximately the same. This maintains approximately constant loop bandwidth for both carrier recovery loops. In the simulations carried out to date, digital feedforward digital AGCs are introduced in each Electra demodulator just after the Costas arm filters to maintain unity RMS arm levels.

As an example of simulated performance with the dual-channel architecture depicted in Figure 1a, we consider the case of two, suppressed carrier BPSK signals, one (strong) centered at IF (256 kbps) and the second (32 kbps) offset by 1.024 MHz. It is assumed that the A/D sample rate is set at 16.384 MHz for this example. The strong signal E_s / N_o is set at 3 dB and the weak signal E_s / N_o = 3 - 10 + 9 = 2 dB. Furthermore, the Costas loop tracking bandwidth for the strong signal was set at approximately 1 kHz whereas that for the weak was set at 500 Hz and both Costas loops were operating at 8 samples per symbol decimated sampling rate (M = 2 in Figure 4). In addition, the input power level was scaled to approximately –30 dB relative to the input noise level and the AGC gain, K_{AGC}, was initialized to 23 dB. Also, the fixed gains were set at: $K_{cic}^1 = K_{cic}^2 = 2$ and $K_{arm}^1 = K_{arm}^2 = 10$.

Based on these parameters, the strong-signal Costas loop SNR is ideally approximately 27 dB (less squaring losses) and the weak-signal Costas loop SNR is approximately 20 dB (less squaring losses). The actual measured values from the simulation experiments are as follows:

(a) Strong/weak signal channel loop SNR: 26.2 dB/19.5 dB using Option 1 ($V_{out} = \max\left\{V_{out}^1, V_{out}^2\right\}$) without digital band select filtering to reduce adjacent channel aliasing and an 8 bit A/D.

(b) Strong/weak signal channel loop SNR: 26.2 dB/19.5 dB using Option 2 without digital band select filtering and an 8 bit A/D.

(c) Strong/weak signal channel loop SNR: 24.3 dB/16.7 dB using a 1 bit front-end A/D (no AGC required) and with digital band select filtering.

As is seen, the dual-channel architecture performs close to ideal using either Option 1 or 2. Furthermore, either option with an 8 bit A/D performs about 2 dB better than 1 bit quantization and is certainly worth the extra implementation cost.

A more dramatic example of this behavior is based on the following scenario: 2 BPSK signals, but in this example the weak signal (256 kbps) is centered at IF and the strong signal (32 kbps) offset by 1.024 MHz. The weak signal E_s / N_o is set at 10 dB and is attenuated by 20 dB relative to the strong signal. Thus, the strong signal E_s / N_o = 10 + 20 + 9 = 39 dB. Furthermore, the Costas loop tracking bandwidth for the strong signal was set at approximately 1 kHz whereas that for the weak was set at approximately 500 Hz and both Costas loops were operating at 8 samples per symbol decimated sampling rate.

For this example, the fixed gains are set at: $K_{cic}^1 = 2.7; K_{cic}^2 = 7.6; K_{arm}^1 = 5.8$ and $K_{arm}^2 = 5.8$, where unit 1 is assigned to the 256 kbps channel and unit 2 is assigned to the 32 kbps channel. Based on these parameters, the strong-signal Costas loop SNR is ideally approximately 57 dB and the weak-signal Costas loop SNR

is approximately 34 dB. The actual measured values from the simulation experiments are:

(a) Strong/weak signal channel loop SNR: 51.9 dB/7.4 dB using AGC control Option 1 with digital band select filtering; a 6 bit A/D and K_{AGC} initialized to 0 dB.

(b) Strong/weak signal channel loop SNR: 88.1 dB/5.9 dB using Option 2 with digital band select filtering and a 6 bit A/D and K_{AGC} initialized to 0 dB.

(c) Strong/weak signal channel loop SNR: 86.0 dB/5.5 dB using a 1 bit front-end A/D and with digital band select filtering.

Thus for either the 6 bit or 1 bit A/D, the weak signal channel carrier recovery essentially breaks down (almost 30 dB below ideal) whereas the strong signal channel carrier recovery continues to function in both cases. In fact for the 1 bit A/D, evidence of noise suppression is seen from the extremely large strong signal channel loop SNR (exceeding the ideal by almost 30 dB). Similarly for the dual channel system using AGC gain option $V_{out} = \min\{V_{out}^1, V_{out}^2\}$. In this latter case, K_{AGC} increases until the A/D saturates in which case it reduces to the 1 bit A/D performance limit as evident from the above simulation results.

Although both signals are strong (E_s / N_o > 10 dB) in this example, it is the strongest which captures the A/D dynamic range. For the 6 bit A/D, calculations of A/D SNR degradation reveals that the quantization noise exceeds the input noise due to AGC limiting on the strong signal. This can be alleviated simply by reducing the fixed gains.

Specifically, by reducing the fixed gain on the strong signal channel, K_{arm}^2, from 5.8 to 2.7 and keeping all the other fixed gains at their original values specified above, we force K_{AGC} to converge to a higher gain (by approximately a factor of 2) thereby limiting quantization noise to less than the input noise. The measured strong/weak signal channel loop SNR values for the dual-channel system with the 6 bit A/D are now: 53.5 dB/32.1 dB. Thus the carrier recovery loops on both channels now function successfully.

The above examples, clearly illustrate the advantages of the dual-channel architecture relative to a 1 bit A/D solution and also illustrates the advantages of strong signal AGC limiting (Option 1) versus weak signal limiting (2). To demonstrate the tracking capability of the dual-channel system, we again consider the previous scenario: two suppresses carrier BPSK signals, with the 256 kbps signal (E_s / N_o = 10 dB) again centered at IF (tracked by Electra demodulator unit 1) and the 32 kbps offset by 1.024 MHz (tracked by unit 2).

However, in this example the 32 kbps signal is initially 20 dB smaller than the 256 kbps signal but increases over the course of the simulation (corresponding to only 62 msecs duration) to being 20 dB larger. Keeping the fixed gains at the values specified above (with $K_{arm}^2 = 2.7$) and again utilizing a 6 bit A/D, we find that the dual-channel system can easily maintain carrier recovery over the 40 dB variation in the 32 kbps signal power level.

Plots of the resulting AGC gain (using AGC control Option 1) as well as the individual AGC gains resulting from using the individual Electra AGC control voltages (V_{out}^1, V_{out}^2) are plotted in Figure 5a along with the 32 kbps signal gain profile. As is seen, initially the system AGC gain coincides with the unit 1 AGC gain (Option 1) when the 256 kbps signal power is largest. However, as the 32 kbps signal power increases, the system AGC gain switches to the unit 2 AGC gain.

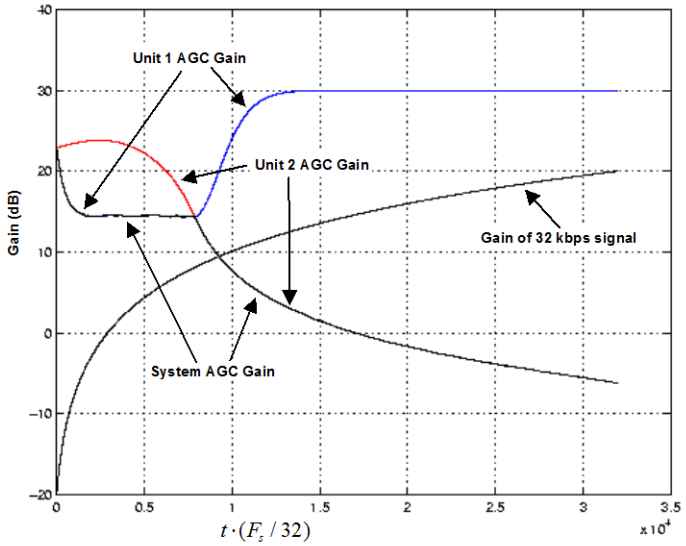


Figure 5a Dual-channel AGC tracking performance for a time-varying scenario.

Corresponding plots of the loop SNR for both demodulators are presented in Figure 5b. Note that the unit 1 loop SNR remains approximately constant near 32 dB (within 2 dB of ideal), which is the desired behavior inasmuch as the 256 kbps signal power remains constant over the duration of the simulation. This is accomplished via the auxiliary feedforward AGC assigned to this channel which maintains the arm outputs from the unit 1 Costas loop at a constant RMS level as discussed above. Note also in Figure 5b that the unit 2 loop SNR increases with increasing 32 kbps signal power.

4. TDM/FDM TRADEOFFS

In assessing data throughput capability, we have considered a realistic scenario wherein the EIRP of the EXM rover is 3

dB less than that of the proposed MRR. In addition, we assume suppressed carrier BPSK signaling from each rover with a target uncoded BER = 10^{-3} at the orbiter receiver. Furthermore we assume the nominal Electra IF bandwidth of 7 MHz. As such, to maximize total data throughput while simultaneously minimizing ACI, we assume that the EXM rover transmits at a maximum rate R_{EX} = 1 Mbps and the maximum rate for the proposed MRR is R_{MR} = 2 Mbps with a separation of 4 MHz between carriers. Thus both signals will fill up the 7 MHz IF receiver bandwidth if transmitting at maximum rate and assuming that mainlobe bandlimiting is applied by both rover transmitters.

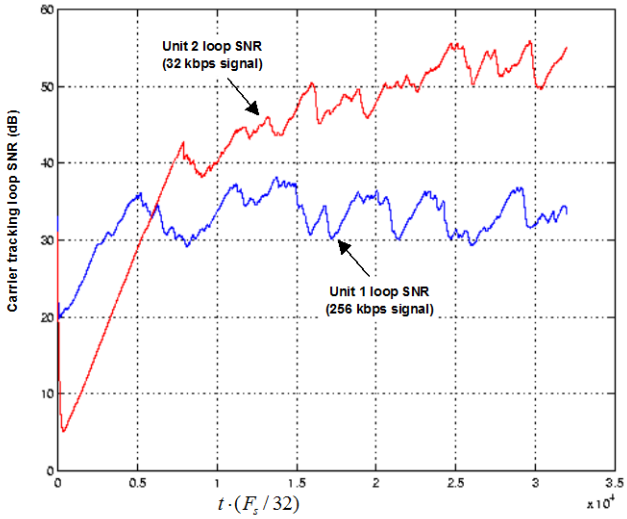


Figure 5b Dual-channel loop SNR performance for the time-varying scenario.

Assuming the rovers transmit simultaneously on a non-interfering basis, the maximum throughput is:

$$T_{MAX} = R_{EX} + R_{MR} = 3 \text{ Mbps},$$

whereas if the rovers transmit on alternate orbit passes (TDM) on a non-interfering basis at max rate then the throughput is:

$$T_{TDM} = (R_{EX} + R_{MR})/2 = 1.5 \text{ Mbps}.$$

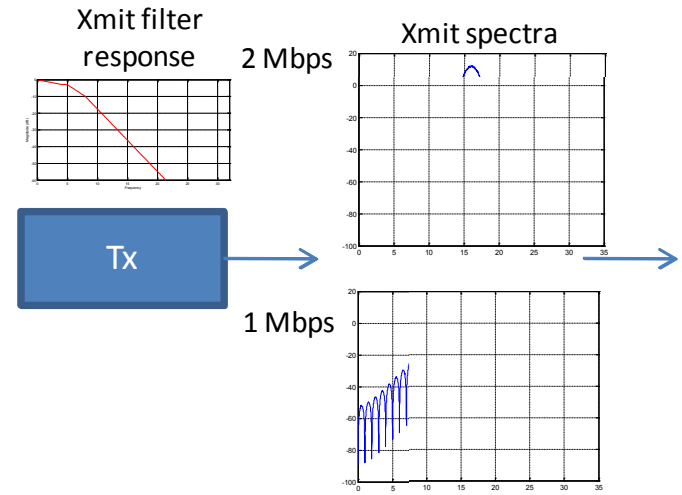
Assuming FDM is used, the achievable throughput, taking into account ACI[3], is:

$$T_{FDM} = \alpha R_{EX} + \beta R_{MR},$$

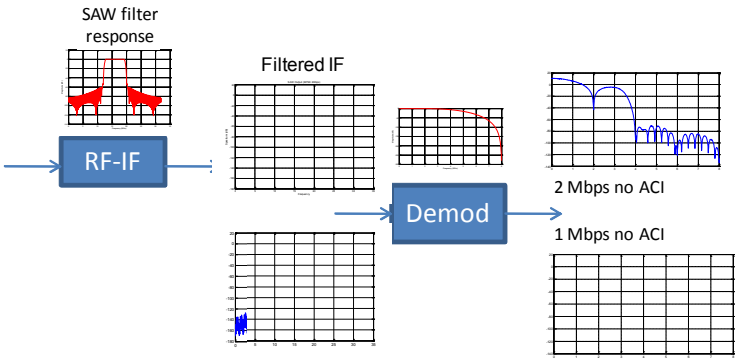
where $0 \leq \alpha,\beta < 1$ represent data rate reduction factors needed to recover ACI losses. The goal of our data throughput study is to determine α,β to achieve the target uncoded BER (10^{-3}).

[3] Here we are ignoring other modem losses including AGC losses, carrier and symbol tracking losses, finite precision effects, etc.

We start by considering single channel performance. In particular, transmit/receive signal spectra for both 1 and 2 Mbps transmit BPSK signals are presented in Figure 6 corresponding to the current Electra transceiver configuration.



a. Transmit spectra



b. Receive spectra

Figure 6 Transmit/receive signal spectra for a single transmit channel.

For both 1 and 2 Mbps, the same transmit, receive SAW and receive digital filtering is assumed. The modeled SAW IF filter bandwidth is 7 MHz and the digital receive filters are set to approximately 4 MHz. The net lowpass filtering bandwidth as indicated in Figure 6b is approximately 4 MHz.

Given this single channel system model, simulated BER performance is presented in Figure 7. As seen, assuming the nominal filtering parameters (transmit, receive SAW, receive digital), the performance loss at 10^{-3} uncoded BER is approximately 0.5 dB at 1 Mbps and 1 dB at 2 Mbps. In our study, it is assumed that these losses are recovered by adjusting the rover transmit powers – not data rates. In particular, to achieve a factor of two increase in data rate with comparable BER performance, the proposed MRR

would have to actually transmit 3.5 dB more power than the EM rover to overcome the extra filtering losses at 2 Mbps. Equivalently, the ratio of transmit powers is: $P_{MR}/ P_{EX} \sim 2.24$. This ratio is assumed in the dual channel (FDM) analysis presented below.

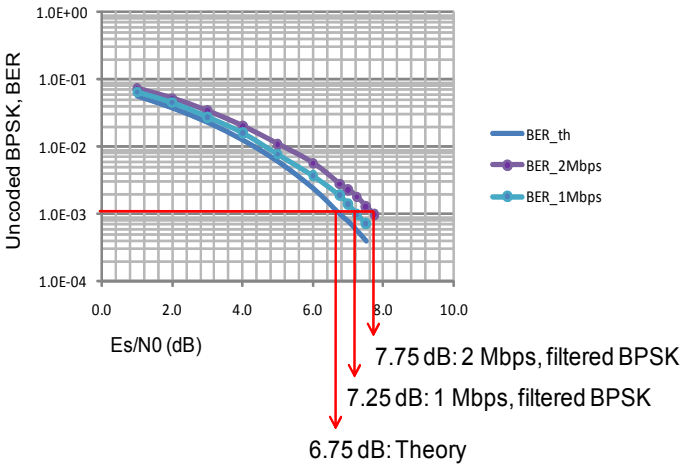


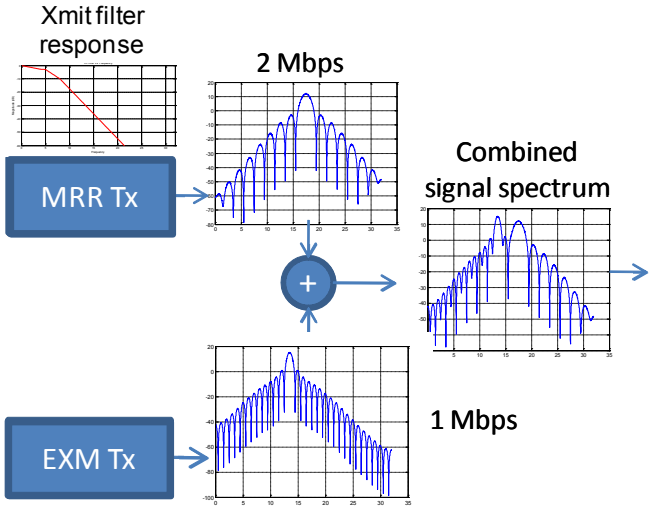
Figure 7 Single-channel BER performance for 1/2 Mbps.

Transmit and receive spectra are presented in Figure 8 corresponding to dual channel, FDM signaling with a 4 MHz separation between carriers. For the FDM analysis, it is assumed that the SAW receive filter response corresponds to the nominal, single-channel response (7 MHz bandwidth). However, we have modified the digital lowpass receive filter to have a much tighter response resulting in a 2 MHz bandwidth and a 60 dB stopband attenuation. This significantly reduces ACI loss. Residual ACI loss can be recovered by appropriate choice of the data rate reduction factors α,β.

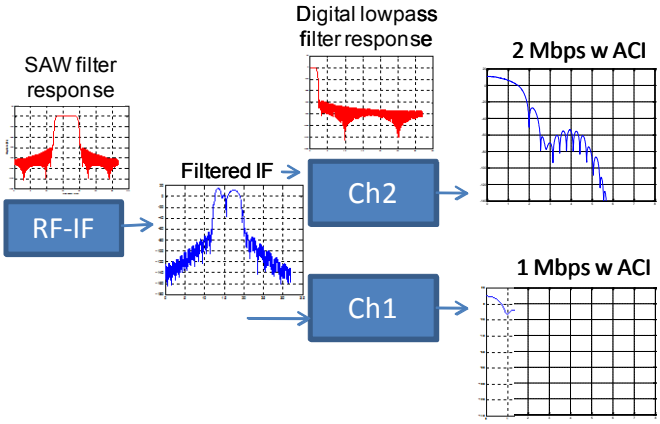
Given this dual channel system model, simulated BER performance is presented in Figure 9. The BER plots include both the single channel BER results (from Figure 7) as well as the dual channel BER results corresponding to EXM data rate: $\alpha\ R_{EX} = 0.9\ R_{EX} = 0.9$ Mbps and MRR data rate: $\beta\ R_{MR} = 0.925\ R_{MR} = 1.85$ Mbps. This slight reduction in the rover transmit rates from their maximum essentially recovers all of the residual ACI loss and still results in a substantial enhancement in data throughput rate over TDM.

5. Summary

In this paper we have presented the results of a study addressing performance and implementation issues in transmitting dual channel, FDM signals for the proposed 2018 Mars rover mission. As discussed in Section 3, a transceiver architecture incorporating dual Electra demodulators fed by a common IF/AGC/A/D path is feasible provided a common AGC control could be implemented (in firmware). This would entail a modification to the Electra demodulator to include additional digital AGCs that are required to equalize the Costas arm signals, i.e., so that the RMS arm levels.in each



a. Transmit spectra



b. Receive spectra

Figure 8 Transmit/receive signal spectra for dual FDM transmit channels.

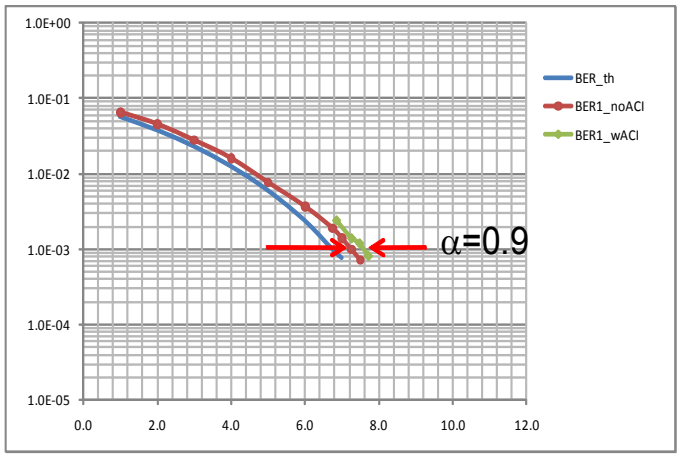
Costas loop is approximately the same. Given this modification, then the dual channel receiver would perform close to ideal with either a min or max common AGC control.

A data throughput analysis was also carried out (Section 4) to determine data throughput rates achievable with FDM signaling from both the EXM and proposed MRR rovers. This study indicates that the existing Electra transmit filter and SAW receive filter can accommodate two channels operating near 1 and 2 Mbps provided their carriers are separated by 4 MHz. Furthermore, FDM has the potential to substantially increase the total data throughput which could be achieved with TDM. In particular, constraining the maximum transmit rates to $R_{EX} = 1$ Mbps (EXM) and $R_{MR} = 2$ Mbps (MRR), the maximum data throughput assuming the rovers would transmit simultaneously on a non-interfering basis is 3 Mbps. With TDM the maximum throughput which

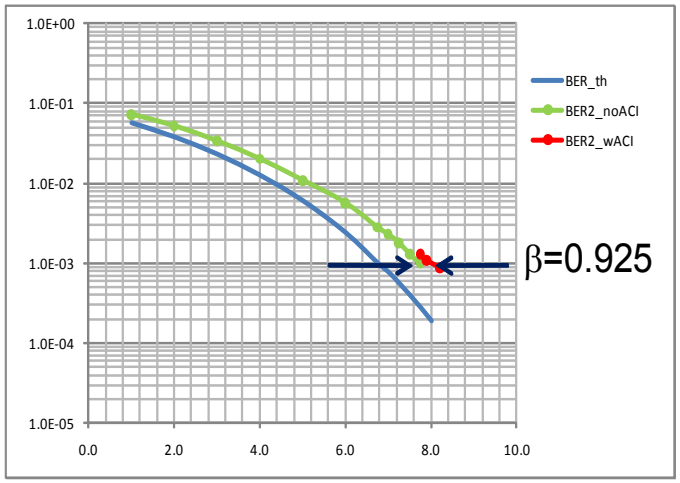
could be achieved is 1.5 Mbps. By modifying the existing Electra transceiver firmware to incorporate tighter digital lowpass receive filters, a maximum data throughput of:

$$T_{FDM} = \alpha R_{EX} + \beta R_{MR} = 0.9 + 0.925X2 = 2.75 \text{ Mbps}$$

could be achieved assuming the rovers transmit simultaneously. Note that these results also tacitly assume that the Electra firmware can be modified to operate at data rates that are not restricted to powers of 2, i.e., to accommodate the data rate reduction factors α,β. Alternatively $\alpha = \beta = 1$ can be used if a slight increase in uncoded BER for the two FDM channels is deemed acceptable.



a. Received EXM BER



b. Received MRR BER

Figure 9 Dual-channel BER performance.

6. Acknowledgements

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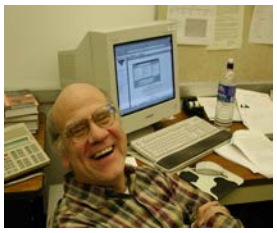

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